DIFFERENTIAL-TO-0.7V DIFFERENTIAL PCI EXPRESS™ JITTER ATTENUATOR

ICS871002I-02

General Description

The ICS871002I-02 is a high performance Jitter Attenuator designed for use in PCI Express™ systems. In some PCI Express systems, such as those found in desktop PCs, the PCI Express clocks are generated from a low bandwidth, high phase noise PLL frequency synthesizer. In these systems, a jitter attenuator may be required to attenuate high frequency random and deterministic jitter components from the PLL synthesizer and from the system board. The ICS871002I-02 has two PLL bandwidth modes: 350kHz and 2000kHz. The 350kHz mode will provide maximum jitter attenuation, but with higher PLL tracking skew and spread spectrum modulation from the motherboard synthesizer may be attenuated. The 2000kHz bandwidth provides the best tracking skew and will pass most spread profiles, but the jitter attenuation will not be as good as the lower bandwidth modes. The ICS871002I-02 can be set for different modes using the F_SELx pins as shown in Table 3C.

The ICS871002I-02 uses IDT 3rd Generation FemtoClock™ PLL technology to achieve the lowest possible phase noise. The device is packaged in a small 20 Lead TSSOP package, making it ideal for use in space constrained applications such as PCI Express add-in cards.

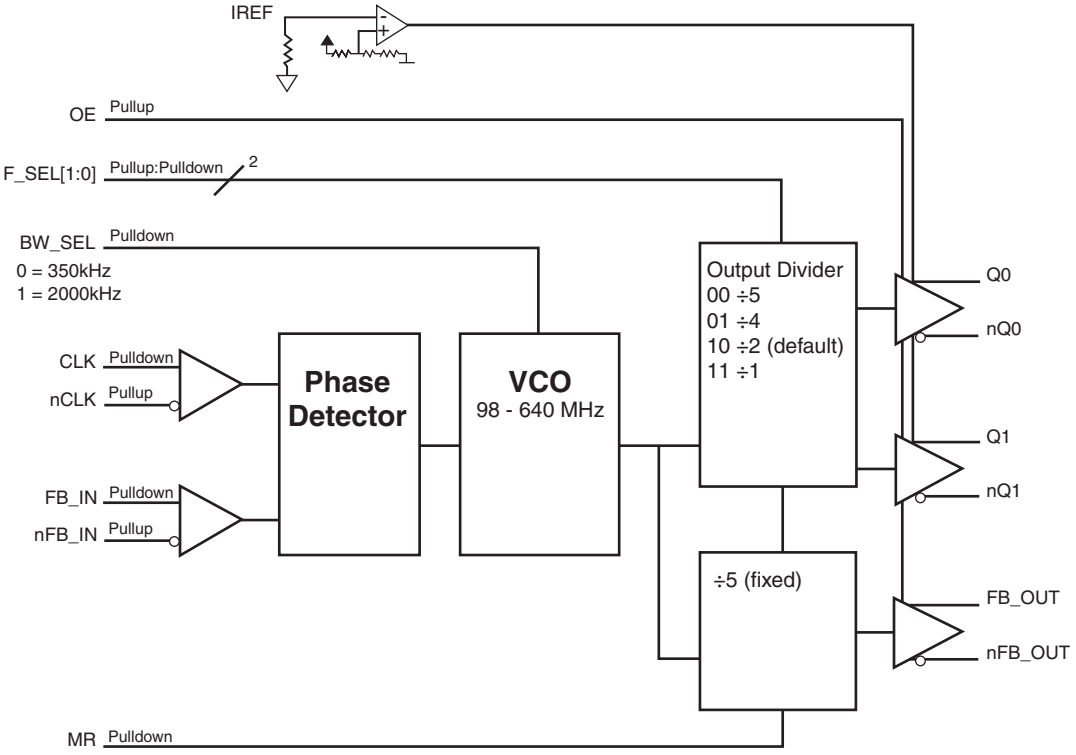
Features

- Two 0.7V differential output pairs
- One differential clock input
- CLK and nCLK supports the following input types: LVPECL, LVDS, LVHSTL, SSTL, HCSL
- Output frequency range: 98MHz - 640MHz
- Input frequency range: 98MHz - 128MHz
- VCO range: 490MHz - 640MHz
- Cycle-to-cycle jitter: 20ps (typical)
- 3.3V operating supply
- Two bandwidth modes allow the system designer to make jitter attenuation/tracking skew design trade-offs
- -40°C to 85°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

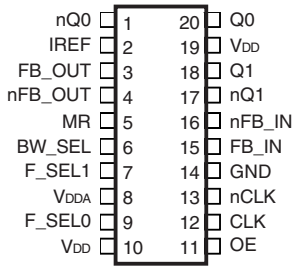
PLL Bandwidth

BW_SEL
0 = PLL Bandwidth: ~350kHz (default)
1 = PLL Bandwidth: ~2000kHz

Block Diagram



Pin Assignment



ICS871002I-02
20-Lead TSSOP
6.5mm x 4.4mm x 0.92mm package body
G Package
Top View

The Preliminary Information presented herein represents a product in pre-production. The noted characteristics are based on initial product characterization and/or qualification. Integrated Device Technology, Incorporated (IDT) reserves the right to change any circuitry or specifications without notice.

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 20	nQ0, Q0	Output		Differential output pair. HCSL interface levels.
2	IREF	Input		A fixed precision resistor (475Ω) from this pin to ground provides a reference current used for differential current-mode Qx/nQx clock outputs.
3, 4	FB_OUT, nFB_OUT	Output		Differential feedback output pair. HCSL interface levels.
5	MR	Input	Pulldown	Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs (Qx, FB_OUT) to go low and the inverted outputs (nQx, nFB_OUT) to go high. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS/LVTTL interface levels.
6	BW_SEL	Input	Pulldown	PLL Bandwidth select input. 0 = 350kHz, 1 = 2000kHz. See Table 3B.
7, 9	F_SEL1, F_SEL0	Input	Pullup, Pulldown	Frequency select pins. LVCMOS/LVTTL interface levels. See Table 3C.
8	V_{DDA}	Power		Analog supply pin.
10, 19	V_{DD}	Power		Core supply pin.
11	OE	Input	Pullup	Output enable pin. When HIGH, the outputs are active. When LOW, the outputs are in a high impedance state. LVCMOS/LVTTL interface levels. See Table 3A.
12	CLK	Input	Pulldown	Non-inverting differential clock input.
13	nCLK	Input	Pullup	Inverting differential clock input.
14	GND	Power		Power supply ground.
15	FB_IN	Input	Pulldown	Non-inverting differential feedback input.
16	nFB_IN	Input	Pullup	Inverting differential feedback input.
17, 18	nQ1, Q1	Output		Differential output pair. HCSL interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

TABLE 3A. OUTPUT ENABLE FUNCTION TABLE

Input	Outputs	
OE	Q[1:0]/nQ[1:0]	FB_OUT/nFB_OUT
0	HiZ	Enabled
1	Enabled	Enabled

TABLE 3B. PLL BANDWIDTH CONTROL TABLE

Input	
BW_SEL	PLL Bandwidth
0	350kHz (default)
1	2000kHz

TABLE 3C. F_SELX FUNCTION TABLE

Input Frequency (MHz)	Inputs			Output Frequency (MHz)
	F_SEL1	F_SEL0	Divider	
100	0	0	5	100
100	0	1	4	125
100	1	0	2	250 (default)
100	1	1	1	500

Absolute Maximum Ratings

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, V_O	-0.5V to V_{DD} + 0.5V
Package Thermal Impedance, θ_{JA}	86.7°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4A. Power Supply DC Characteristics, V_{DD} = 3.3V±10%, TA = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		2.97	3.3	3.63	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.13	3.3	V_{DD}	V
I_{DD}	Power Supply Current			75		mA
I_{DDA}	Analog Supply Current			13		mA

Table 4B. LVCMOS/LVTTL DC Characteristics, V_{DD} = 3.3V±10%, TA = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{DD} = 3.63V	2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		V_{DD} = 3.63V	-0.3		0.8	V
I_{IH}	Input High Current	F_SEL1, OE	V_{DD} = V_{IN} = 3.63V			5	µA
		F_SEL0, MR, BW_SEL	V_{DD} = V_{IN} = 3.63			150	µA
I_{IL}	Input Low Current	F_SEL1, OE	V_{DD} = 3.63V, V_{IN} = 0V	-150			µA
		F_SEL0, MR, BW_SEL	V_{DD} = 3.63V, V_{IN} = 0V	-5			µA

Table 4C. Differential DC Characteristics, V_{DD} = 3.3V±10%, TA = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK, FB_IN	V_{DD} = V_{IN} = 3.63V			150	µA
		nCLK, nFB_IN	V_{DD} = V_{IN} = 3.63V	5			µA
I_{IL}	Input Low Current	CLK, FB_IN	V_{DD} = V_{IN} = 63V			150	µA
		nCLK, nFB_IN	V_{DD} = V_{IN} = 3.63V	-150			µA
V_{PP}	Peak-to-Peak Input Voltage			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			GND + 0.5		V_{DD} - 0.85	V

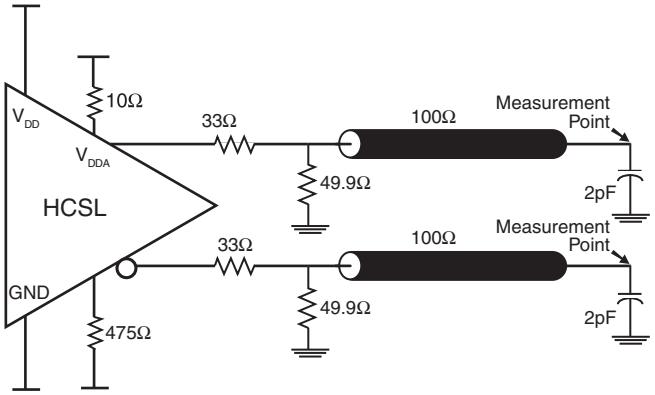
NOTE 1: Common mode voltage is defined as V_{IH}.
NOTE 2: For single ended applications, the maximum input voltage for CLK, nCLK is V_{DD} + 0.3V.

TABLE 5. AC CHARACTERISTICS, V_{DD} = 3.3V±10%, T_A = -40°C TO 85°C

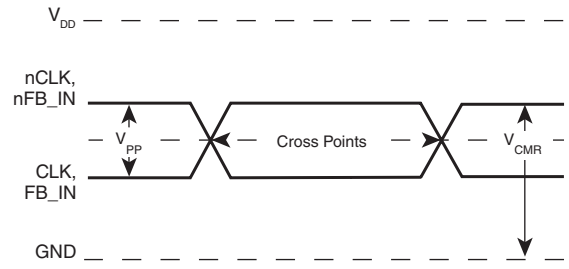
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency		98		640	MHz
*t*jit(cc)	Cycle-to-Cycle Jitter; NOTE 1	PLL Mode		20		ps
V_{HIGH}	Voltage High		660		850	mV
V_{LOW}	Voltage Low		-150			mV
V_{OVS}	Max. Voltage, Overshoot				V_{HIGH} + 0.3	V
V_{UDS}	Min. Voltage, Undershoot		-0.3			V
V_{rb}	Ringback Voltage				0.2	V
V_{CROSS}	Absolute Crossing Voltage		250		550	mV
ΔV_{CROSS}	Total Variation of V_{CROSS} over all edges				140	mV
t_R / t_F	Output Rise/Fall Time	measured between 0.175V to 0.525V	175		700	ps
$\Delta t_R / \Delta t_F$	Rise/Fall Time Variation				125	ps
t_{RFM}	Rise/Fall Matching				125	ps
odc	Output Duty Cycle		45		55	%

NOTE 1: This parameter is defined in accordance with JEDEC Standard 65.

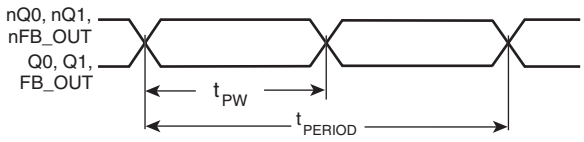
PARAMETER MEASUREMENT INFORMATION



3.3V HCSL OUTPUT LOAD AC TEST CIRCUIT

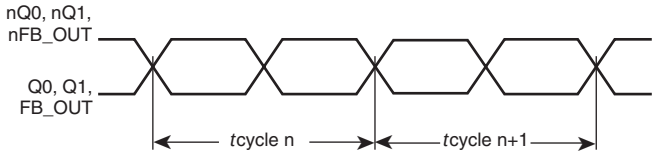


DIFFERENTIAL INPUT LEVEL



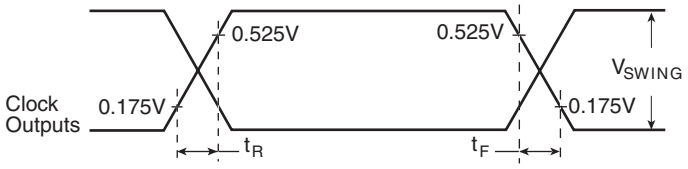
$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



$tjit(cc) = tcycle\ n - tcycle\ n+1$
1000 Cycles

CYCLE-TO-CYCLE JITTER



OUTPUT RISE/FALL TIME

APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS871002I-02 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD} and V_{DDA} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 10Ω resistor along with a 10μF and a 0.01μF bypass capacitor should be connected to each V_{DDA} pin.

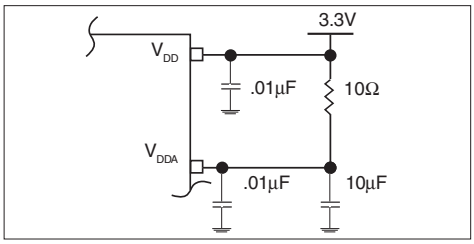


FIGURE 1. POWER SUPPLY FILTERING

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 2 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = V_{DD}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

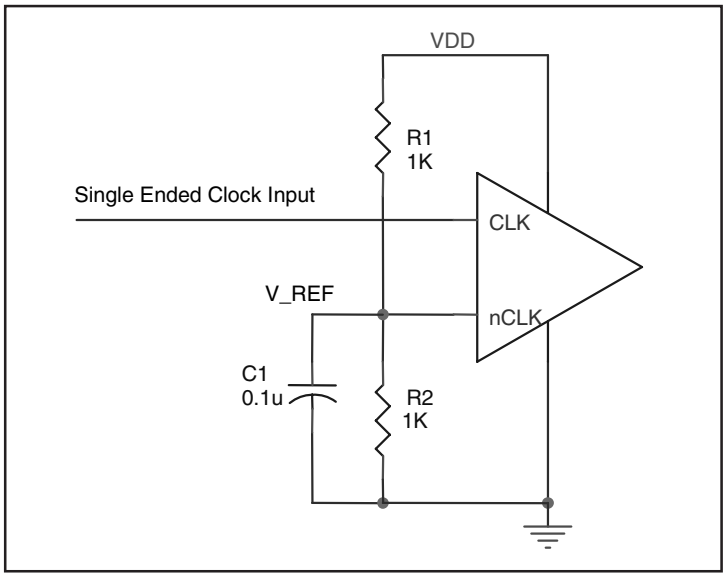


FIGURE 2. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

INPUTS:

LVCMOS CONTROL PINS

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

OUTPUTS:

DIFFERENTIAL OUTPUTS

All unused differential outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

DIFFERENTIAL CLOCK INPUT INTERFACE

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 3A to 3F* show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in Figure 3A, the input termination applies for IDT HiPerClockS open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

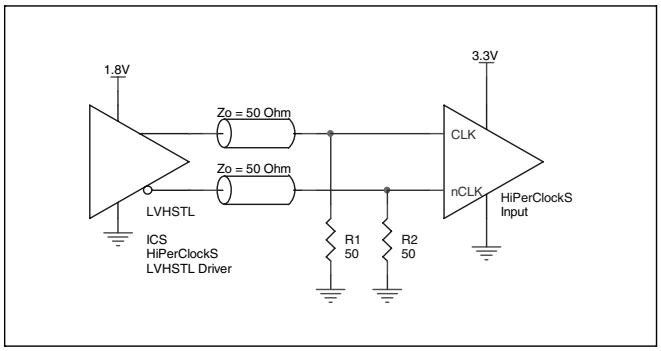


FIGURE 3A. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY AN IDT OPEN EMITTER HIPERCLOCKS LVHSTL DRIVER

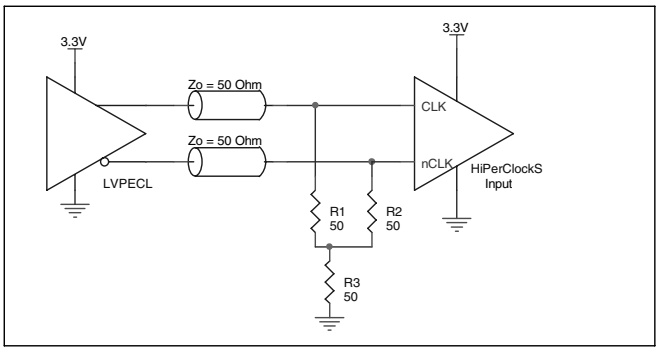


FIGURE 3B. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY A 3.3V LVPECL DRIVER

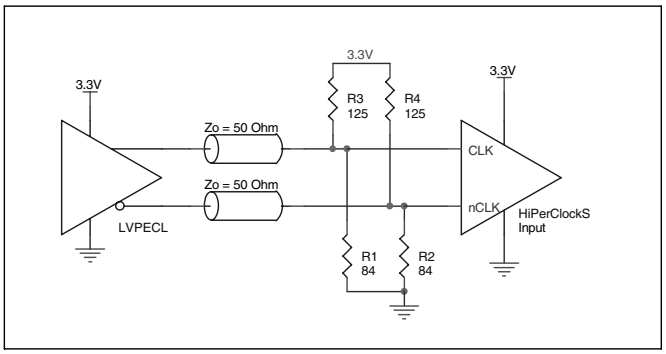


FIGURE 3C. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY A 3.3V LVPECL DRIVER

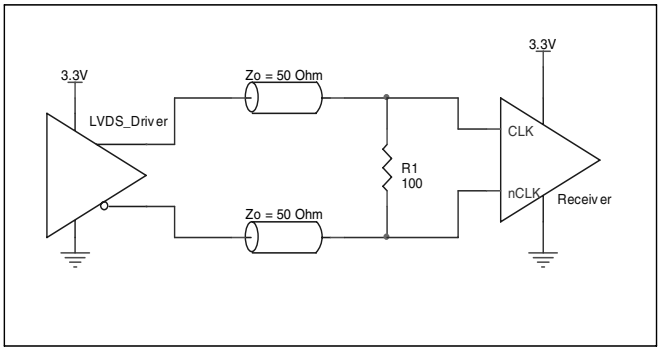


FIGURE 3D. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY A 3.3V LVDS DRIVER

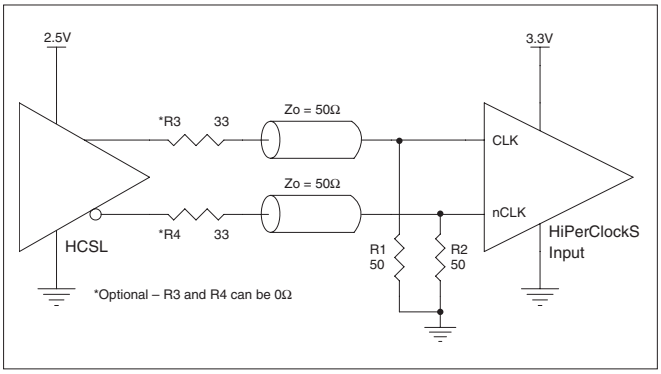


FIGURE 3E. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY A 3.3V HCSL DRIVER

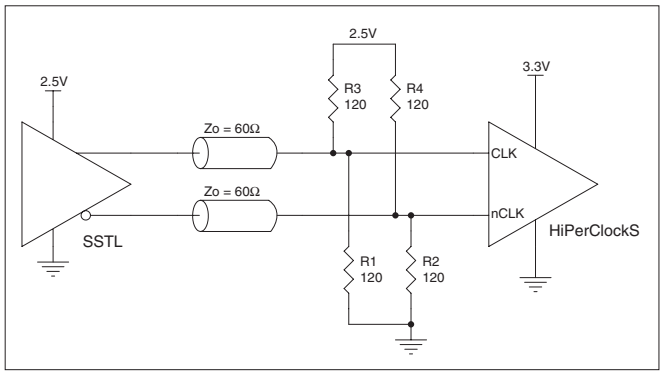


FIGURE 3F. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY A 2.5V SSTL DRIVER

Recommended Termination

Figure 4A is the recommended termination for applications which require the receiver and driver to be on a separate PCB. All traces should be 50Ù impedance.

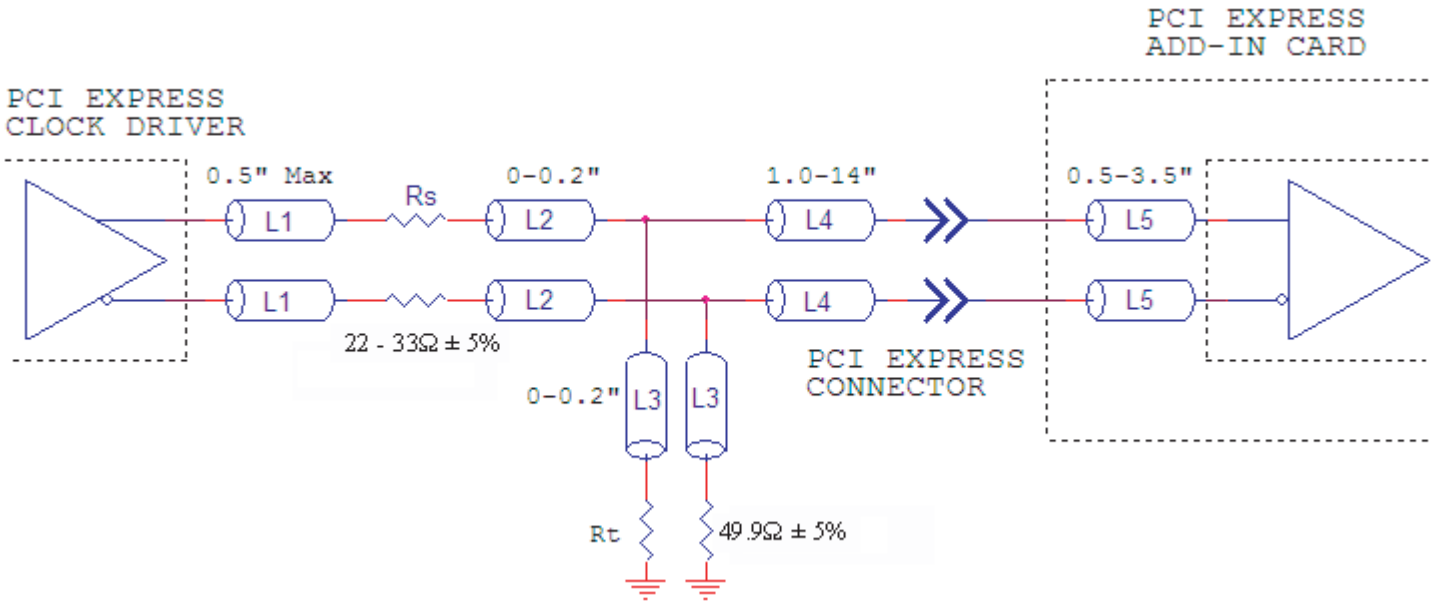


Figure 4A. Recommended Termination

Figure 4B is the recommended termination for applications which require a point to point connection and contain the driver and receiver on the same PCB. All traces should all be 50Ù impedance.

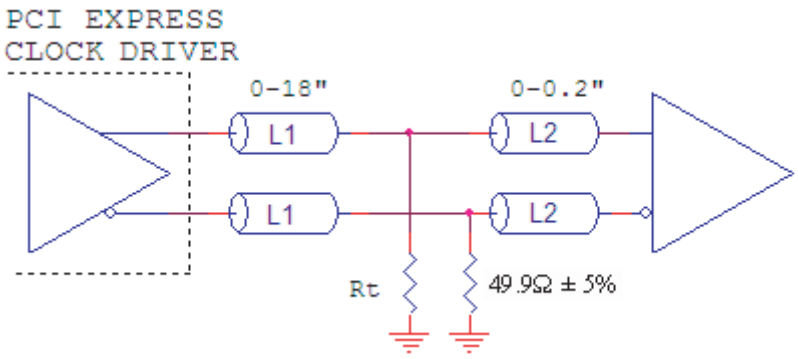


Figure 4B. Recommended Termination

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS871002I-02.
Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the ICS871002I-02 is the sum of the core power plus the analog power plus the power dissipated in the load(s).
The following is the power dissipation for V_{DD} = 3.3V + 10% = 3.63V, which gives worst case results.
NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX} = V_{DD\_MAX} * (I_{DD\_MAX} + I_{DDA\_MAX})$ = 3.63V * (75mA + 15mA) = **326.7mW**
- Power $(outputs)_{MAX}$ = **47.75mW/Loaded Output pair**
  If all outputs are loaded, the total power is 2 * 47.75mW = **95.5mW**

Total Power$_{\_MAX}$ (3.63V, with all outputs switching) = 326.7mW + 95.5mW = **422.2mW**

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in Section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 86.7°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:
85°C + 0.422W * 86.7°C/W = 121°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 6. THERMAL RESISTANCE θ_{JA} FOR 20-PIN TSSOP, FORCED CONVECTION

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	86.7°C/W	82.4°C/W	80.2°C/W

3. Calculations and Equations.

The purpose of this section is to calculate power dissipation on the IC per HCSL output pair.

HCSL output driver circuit and termination are shown in *Figure 5.*

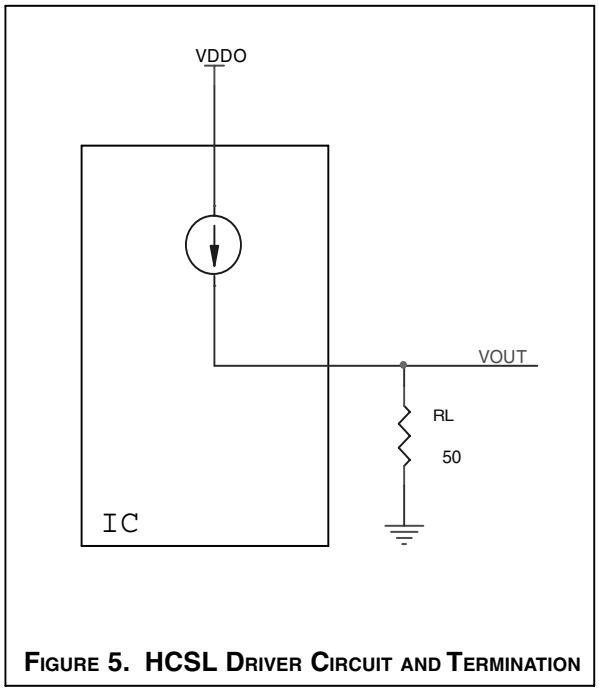


FIGURE 5. HCSL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{DD} – 2V.

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

$Pd\_H = (V_{OH\_MAX}/R_L) * (V_{DD\_MAX} - V_{OH\_MAX})$

$Pd\_L = (V_{OL\_MIN}/R_L) * V_{OL\_MIN}$

Pd_H = (0.85V/50Ω) * (3.63V – 0.85V) = **47.3mW**
Pd_L = (0.15V/50Ω) * 0.15V = **0.45mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **47.75mW**

RELIABILITY INFORMATION

TABLE 7. θ_{JA} VS. AIR FLOW TABLE FOR 20 LEAD TSSOP

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	86.7°C/W	82.4°C/W	80.2°C/W

TRANSISTOR COUNT

The transistor count for ICS871002I-02 is: 1704

PACKAGE OUTLINE - G SUFFIX FOR 20 LEAD TSSOP

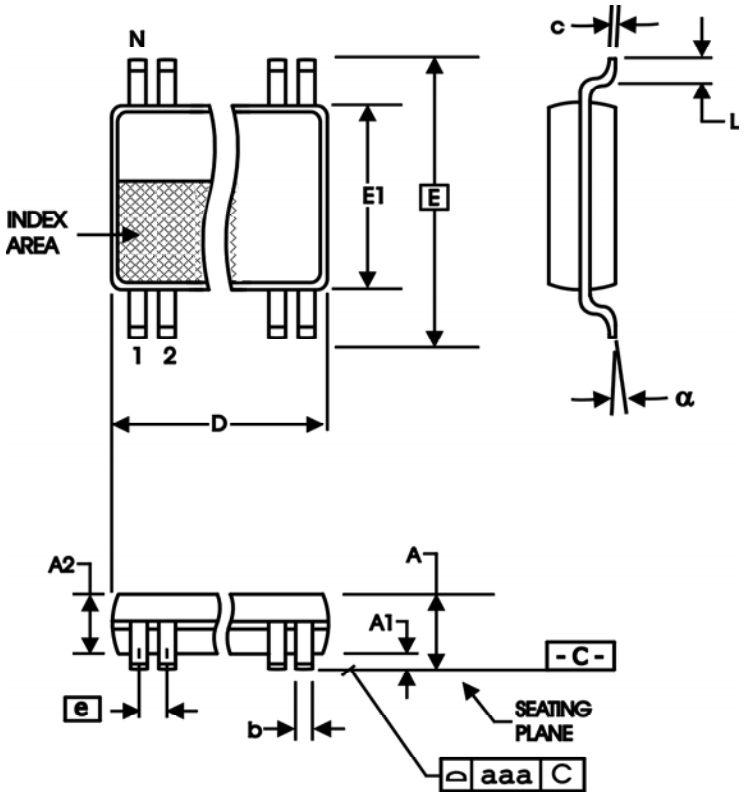


TABLE 8. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	MIN	MAX
N	20	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	6.40	6.60
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS871002AGI-02	ICS71001I-02	20 Lead TSSOP	tube	-40°C to 85°C
ICS871002AGI-02T	ICS71001I-02	20 Lead TSSOP	2500 tape & reel	-40°C to 85°C
ICS871002AGI-02LF	TBD	20 Lead "Lead-Free" TSSOP	Tray	-40°C to 85°C
ICS871002AGI-02LFT	TBD	20 Lead "Lead-Free" TSSOP	2500 tape & reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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