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- Over Voltage Protection and Lock Out for 12 V, 5 V, 3.3 V
- Under Voltage Protection and Lock Out for 5 V and 3.3 V
- Fault Protection Output With Open-Drain Output Stage
- Open-Drain Power Good Output Signal for Power Good Input, 3.3 V and 5 V
- 300-ms Power Good Delay
- 75-ms Delay for 5-V and 3.3-V Power Supply Short-Circuit Turnon Protection
- 2.3-ms PSON Control to FPO Turnoff Delay
- 38-ms PSON Control Debounce
- 73-μs Width Noise Deglitches
- Wide Supply Voltage Range From 4 V to 15 V

description

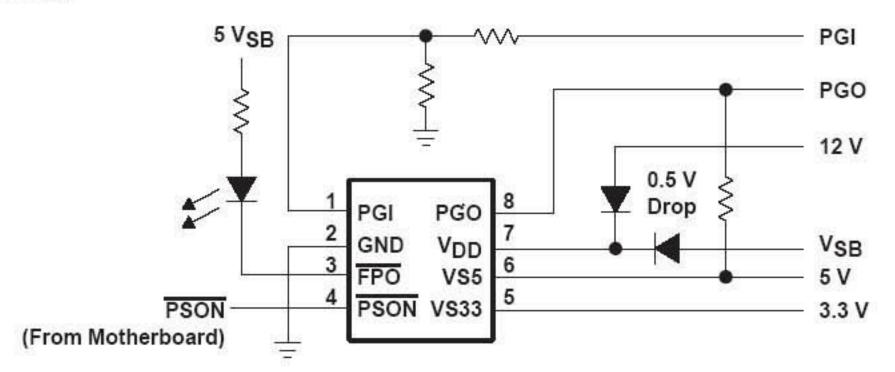
The TPS3510 is designed to minimize external components of personal-computer switching power supply systems. It provides protection circuits, power good indicator, fault protection output (FPO) and PSON control.

Over voltage protection (OVP) monitors 3.3 V, 5 V, and 12 V (12-V signal detects via V_{DD} pin). Under voltage protection (UVP) monitors 3.3 V and 5 V. When an OV or UV condition is detected, the power good output (PGO) is set to low and FPO is latched high. PSON from low to high resets the protection latch. UVP function is enabled 75 ms after PSON is set low and debounced. Furthermore, there is a 2.3-ms delay (and an additional 38-ms debounce) at turnoff. There is no delay during turnon.

Power good feature monitors PGI, 3.3 V and 5 V and issues a power good signal when the output is ready.

The TPS3510 is characterized for operation from -40°C to 85°C.

typical application



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Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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FUNCTION TABLE

PGI	PSON	UV CONDITION (3.3 V OR 5 V)	OV CONDITION (3.3 V, 5 V, OR 12 V)	FPO	PGO
<0.95 V	L	no	no	L	L
<0.95 V	L	no	yes	Н	L
<0.95 V	L	yes	no	Ĺ	L
0.95 V <pgi<1.15 td="" v<=""><td>L</td><td>no</td><td>no</td><td>L</td><td>L</td></pgi<1.15>	L	no	no	L	L
0.95 V <pgi<1.15 td="" v<=""><td>L</td><td>no</td><td>yes</td><td>Н</td><td>L</td></pgi<1.15>	L	no	yes	Н	L
0.95 V <pgi<1.15 td="" v<=""><td>L</td><td>yes</td><td>no</td><td>Н</td><td>L</td></pgi<1.15>	L	yes	no	Н	L
PGI > 1.15 V	L	no	no	L	Н
PGI > 1.15 V	L	no	yes	Н	L
PGI > 1.15 V	L	yes	no	Н	L
х	Н	х	х	Н	L

x = don't care

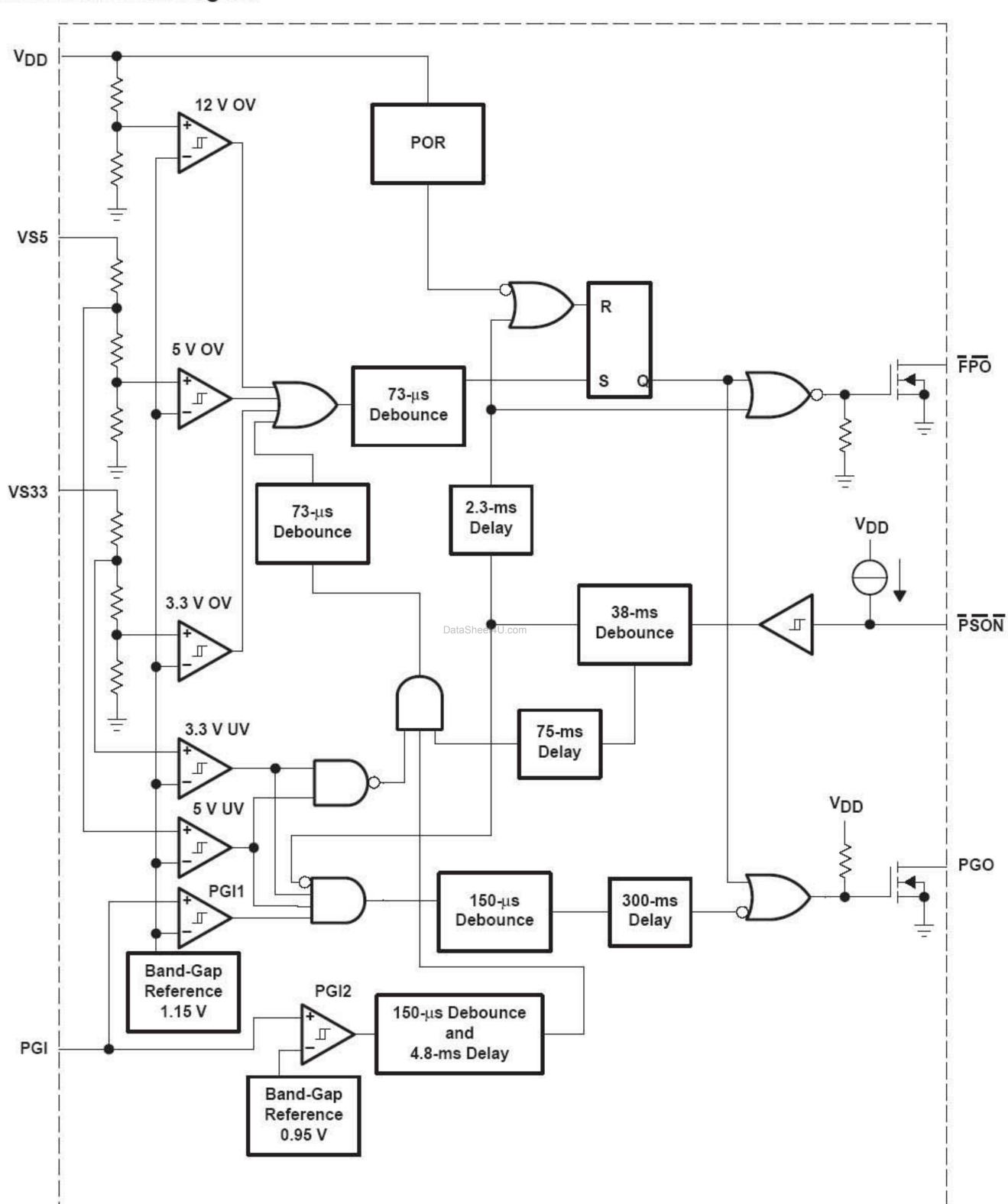
FPO = L means: fault IS NOT latched FPO = H means: fault IS latched

PGO = L means: fault PGO = H means: NO fault

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functional block diagram

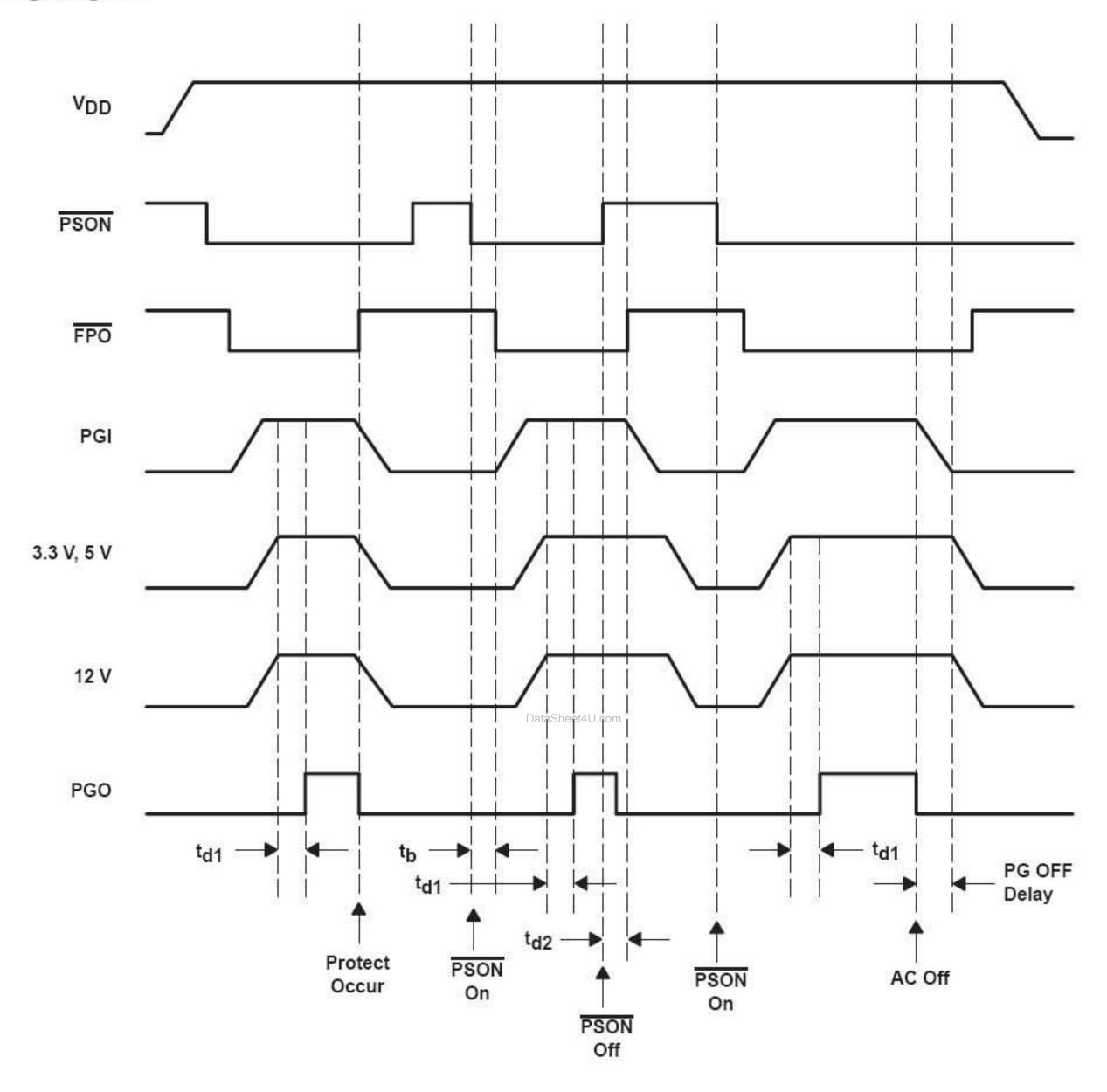


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timing diagram



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Terminal Functions

TERMIN	RMINAL		DECORIDATION	
NAME	NO.	1/0	DESCRIPTION	
FPO	3	0	Inverted fault protection output, open drain output stage	
GND	2		Ground	
PGI	1	I	Power good input	
PGO	8	0	Power good output, open drain output stage	
PSON	4	1	/OFF control	
V_{DD}	7	E	Supply voltage/12 V over-voltage protection input pin	
VS33	5	1	3.3 V over/under-voltage protection	
VS5	6	Į,	5 V over/under-voltage protection	

detailed description

power good and power good delay

A PC power supply is commonly designed to provide a power-good signal, which is defined by the computer manufacturers. PGO is a power-good signal and should be asserted high by the PC power supply to indicate that the 5-V and 3.3-V outputs are above the under-voltage threshold limit. At this time the converter should be able to provide enough power to ensure continuous operation within the specification. Conversely, when either the 5-V or the 3.3-V output voltages fall below the under-voltage threshold, or when ac power has been removed for a time sufficiently long so that power supply operation is no longer ensured, PGO should be de-asserted to a low state.

Figure 1 represents the timing characteristics of the power good (PGO), dc enable (PSON), and the 5 V/3.3 V supply rails.

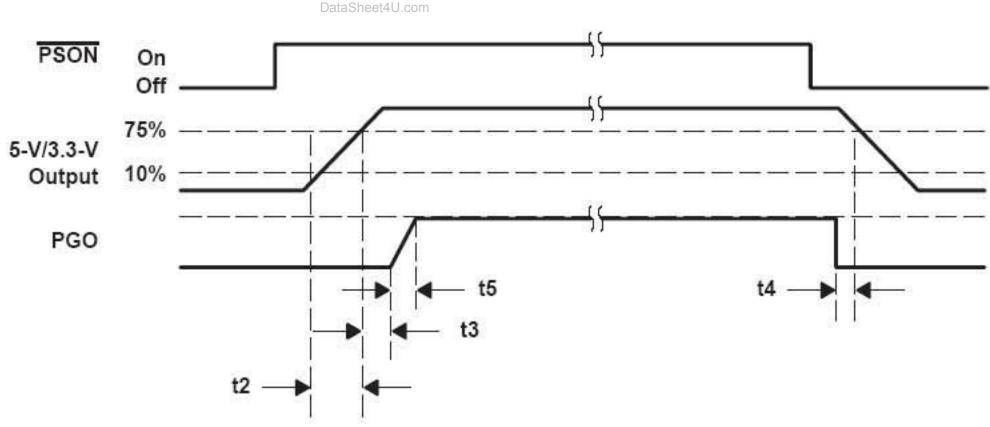


Figure 1. Timing of PSON and PGO

Although there is no requirement to meet specific timing parameters, the following signal timings are recommended:

 $2ms \le t2 \le 20 \text{ ms}, 100 \text{ ms} < t3 < 2000 \text{ ms}, t4 > 1 \text{ ms}, t5 \le 10 \text{ ms}$

Furthermore motherboards should be designed to comply with the previously recommended timing. If timings other than these are implemented or required, this information should be clearly specified.

The TPS3510 family of power-supply supervisors provides a power-good output (PGO) for the 3.3-V and 5-V supply voltage rails and a separate power-good input (PGI). An internal timer is used to generate a 300-ms power-good delay. If the voltage signals at PGI, VS33, and VS5 rise above the under-voltage threshold, the

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open-drain power-good output (PGO) goes high after a delay of 300 ms. When the PGI voltage or either the 3.3-V and 5-V power rails drops below the under-voltage threshold, PGO is disabled immediately (after 150-μs debounce).

power supply remote on/off (PSON) and fault protect output (FPO)

Since the latest personal computer generation focuses on easy turnon and power saving functions, the PC power supply requires two characteristics. One is a dc power supply remote on/off function, the other is standby voltage to achieve very low power consumption of the PC system. Thus the main power needs to be shut down.

The power supply remote on/off (PSON) is an active low signal that turns on all of the main power rails including 3.3 V, 5 V, –5 V, 12 V, and –12 V power rails. When this signal is held high by the PC motherboard or left open circuited, the signal of the fault protect output (FPO) also goes high. Thus, the main power rails should not deliver current and should be held at 0 V.

When the FPO signal is held high due to an occurring fault condition, the fault status is latched and the outputs of the main power rails should not deliver current but are held at 0 V. Toggling the power supply remote on/off (PSON) from low to high resets the fault-protection latch. During this fault condition only the standby power is not affected.

When PSON goes from high to low or low to high, the 38-ms debounce block is active to avoid a glitch on the input that disables/enables the FPO output. During this period the under-voltage function is disabled for 75 ms to prevent turnon failure. At turnoff, there is an additional delay of 2.3 ms from PSON to FPO.

Power should be delivered to the rails only if the PSON signal is held at ground potential, thus FPO is active-low. The FPO pin can be connected to 5 V (or up to 15 V) through a pullup resistor.

under-voltage protection

The TPS3510 provides under-voltage protection (UVP) for the 3.3-V and 5-V rails. When an under voltage condition appears at either one of the 3.3-V (VS33) or 5-V (VS5) input pins for more than 146 μ s, the FPO output goes high and PGO goes low. Also, this fault condition is latched until PSON is toggled from low to high or V_{DD} is removed.

The need for under voltage protection is often overlooked in off-line switching power supply system design. But it is very important in battery-powered or hand-held equipment since the TTL or CMOS logic often results in malfunction.

In flyback or forward-type off-line switching power supplies, usually designed for low power, the over-load protection design is very simple. Most of these types of power supplies are only sensing the input current for an overload condition. The trigger point needs to be set much higher than the maximum load in order to prevent false turnon.

However, this causes one critical problem. If the connected load is larger than the maximum allowable load but smaller than the trigger point, the system always becomes overheated with failure and damage occurring.

over-voltage protection

The over voltage protection (OVP) of TPS3510 monitors 3.3 V, 5 V, and 12 V (12 V is sensed via the V_{DD} pin). When an over-voltage condition appears at one of the 3.3-V, 5-V, or 12-V input pins for more than 73 μ s, the FPO output goes high and PGO goes low. Also, this fault condition is latched until PSON is toggled from low to high or V_{DD} is removed. During fault conditions, most power supplies have the potential to deliver higher output voltages than those normally specified or required. In unprotected equipment, it is possible for output voltages to be high enough to cause internal or external damage of the system. To protect the system under these abnormal conditions, it is common practice to provide over-voltage protection within the power supply.

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Because TTL and CMOS circuits are very vulnerable to over-voltages, it is becoming industry standard to provide overvoltage protection on all 3.3-V and 5-V outputs. However, not only the 3.3-V and 5-V rails for the logic circuits on the motherboard need to be protected, but also the 12-V peripheral devices such as the hard disk, floppy disk, and CD-ROM players etc., need to be protected.

short-circuit power supply turnon

During safety testing the power supply might have tied the output voltage direct to ground. If this happens during the normal operating, this is called a short-circuit or over-current condition. When it happens before the power supply turns on, this is called a short-circuit power supply turn on. It can happen during the design period, in the production line, at quality control inspection or at the end user. The TPS3510 provides an under-voltage protection function with a 75-ms delay after PSON is set low.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V _{DD} (see Note1)	
Output voltage Vo: FPO	
PGO	
All other pins (see Note 1)	
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, TA	
Storage temperature range, T _{stq}	
e receige recordens and a second of the seco	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute—maximum—rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

DISSIPATION RATING TABLE

PACKAGE	T _A ≤ 25°C POWER RATING	DERATING FACTOR ABOVE T _A = 25°C	T _A = 70°C POWER RATING	T _A = 85°C POWER RATING
Р	1092 mW	8.74 mW/°C	699 mW	568 mW
D	730 mW	5.84 mW/°C	467 mW	379 mW

recommended operating conditions at specified temperature range

	4	15	3.7
Supply voltage, V _{DD}		10	V
PSON, VS5, VS33		7	
PGI	V _{DI}	D + 0.3 V ax = 7 V)	٧
FPO	89		V
PGO		15 7 V _{DD} + 0.3 V (max = 7 V) 15 7 20 10	V
FPO		20	
PGO		10	mA
See Note 2	1		ms
	-40	85	°C
	FPO PGO PGO	FPO PGO PGO PGO See Note 2 (m	FPO (max = 7 V) FPO 15 PGO 7 FPO 20 PGO 10 See Note 2 1

NOTE 2: VDD rising and falling slew rate must be less than 14 V/ms.

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electrical characteristics over recommended operating conditions (unless otherwise noted)

over-voltage protection

	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
		VS33		3.7	3.9	4.1	
	Over-voltage threshold	VS5		5.7	6.1	6.5	V
		V_{DD}		13.2	13.8	14.4	
ILKG	Leakage current (FPO)	•	V(FPO) = 5 V			5	μΑ
Vol	Low-level output voltage (FPO)		$V_{DD} = 5 \text{ V}$, $I_{sink} = 20 \text{ mA}$	5		0.7	٧
	Noise deglitch time OVP		V _{DD} = 5 V	35	73	110	μs

PGI and PGO

	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
\ <i>I</i>	Input threehold voltage (DCI)	PGI1		1.1	1.15	1.2	٧
VPGI	Input threshold voltage (PGI)	PGI2		0.9	0.95	1	V
VIT	Linder voltage threshold	VS33		2	2.2	2.4	V
	Under-voltage threshold	VS5		3.3	3.5	3.7	٧
ILKG	Leakage current (PGO)		PGO = 5 V			5	μΑ
Vol	Low-level output voltage (PGO)	90	$V_{DD} = 4 \text{ V}$, $I_{sink} = 10 \text{ mA}$			0.4	V
	Short-circuit protection delay	3.3 V, 5 V		49	75	114	ms
÷	Dolov timo	PGI to PGO	V _{DD} = 5 V	200	300	450	ms
^t d1	Delay time	PGI to FPO		3.2	4.8	7.2	
		PGI to PGO		88	150	225	
	Noise deglitch time	PGI to FPO	V _{DD} = 5 V	180	296	445	μS
		UVP to FPO eet	4 U .com	82	146	220	

PSON control

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
lį:	Input pullup current	PSON = 0 V		120	The state of the s	μΑ
VIH	High-level input voltage		2.4			V
VIL	Low-level input voltage				1.2	٧
t _b	Debounce time (PSON)	V _{DD} = 5 V	24	38	57	ms
t _{d2}	Delay time (PSON to FPO)	V _{DD} = 5 V	t _b +1.1	t _b +2.3	t _b +4	ms

total device

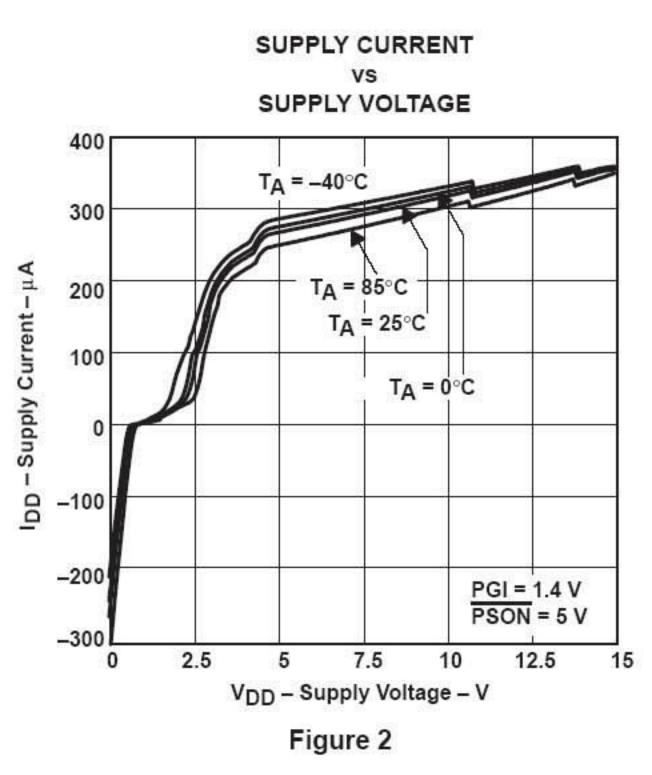
	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
IDD	Supply current	PSON = 5 V	S		1	mA

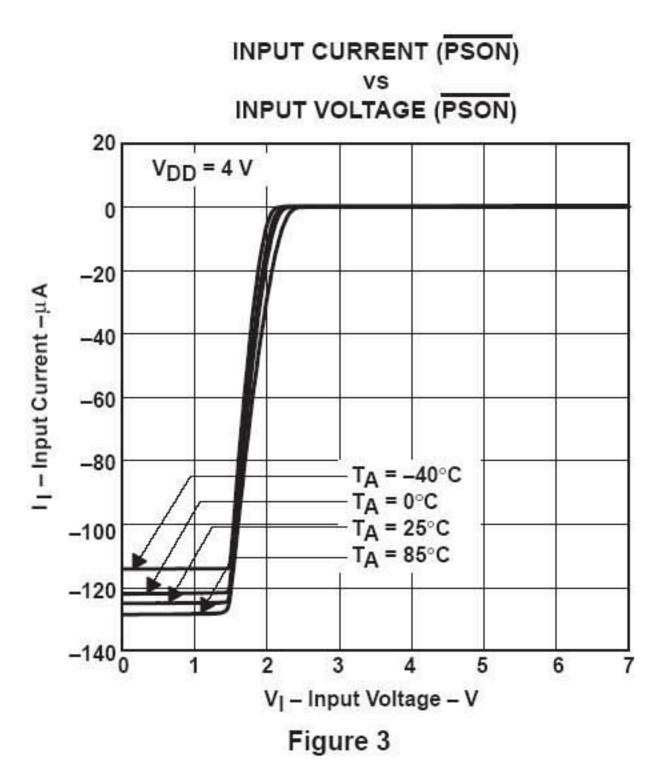
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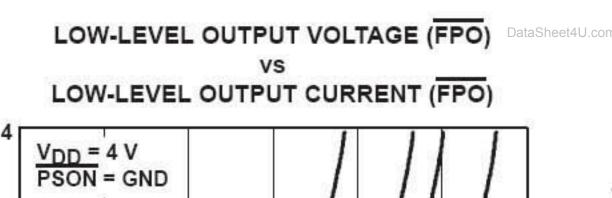
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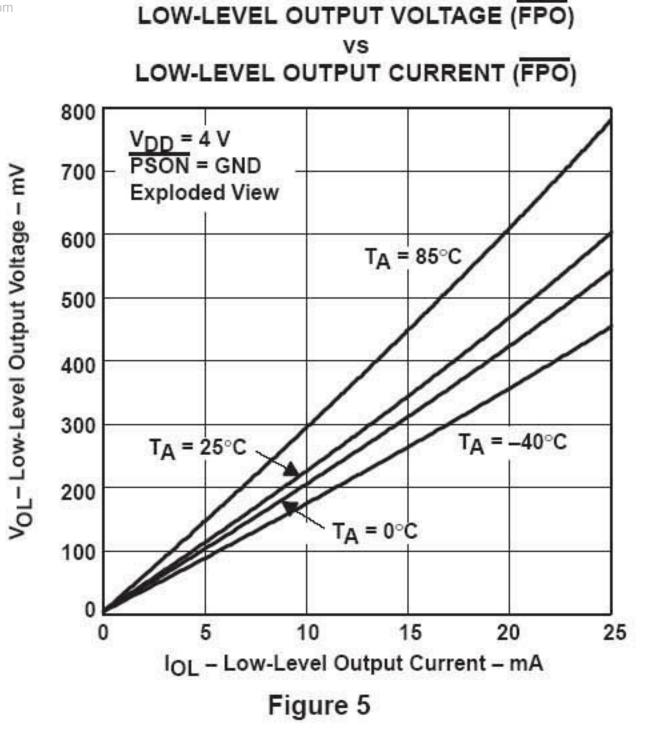
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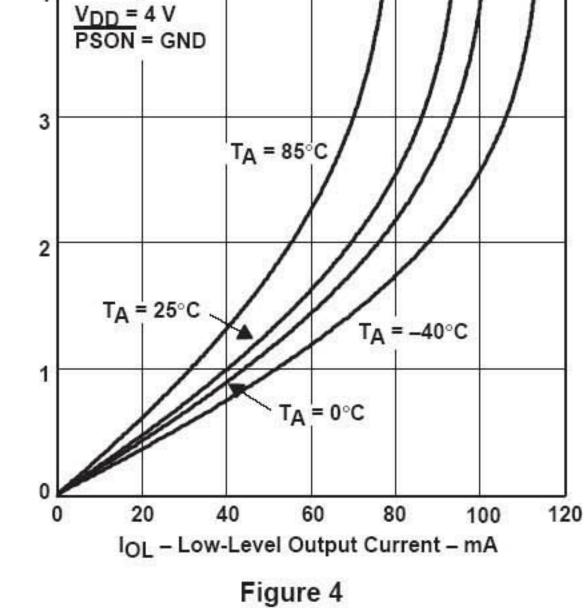
TYPICAL CHARACTERISTICS











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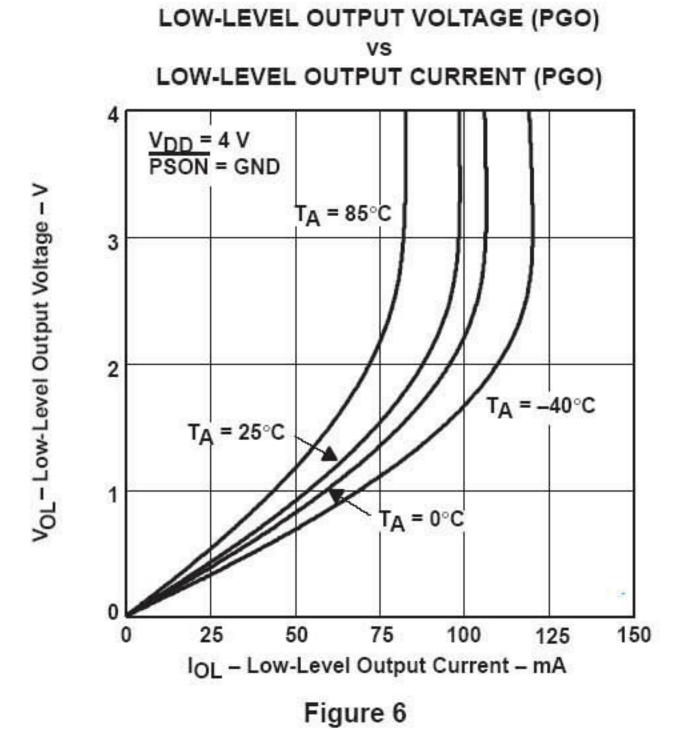
Vol- Low-Level Output Voltage - V

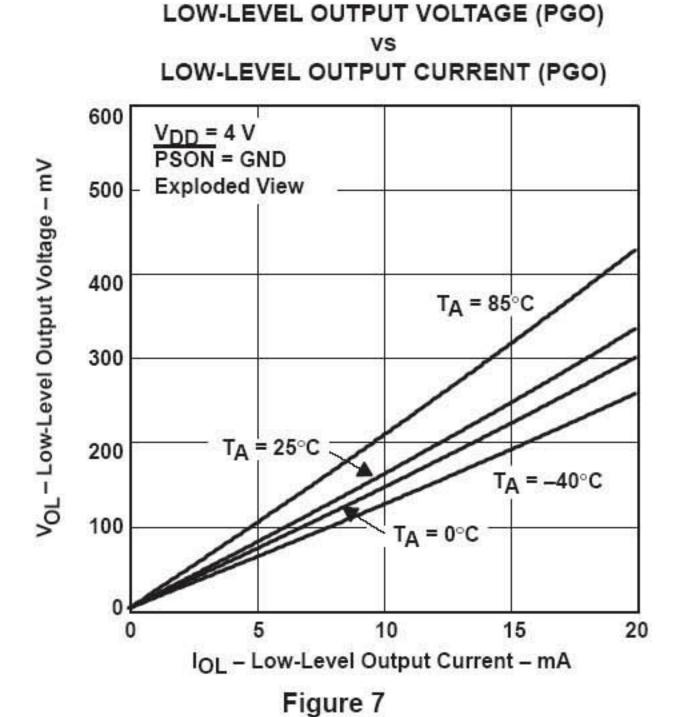
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TYPICAL CHARACTERISTICS





NORMALIZED SENSE THRESHOLD VOLTAGE

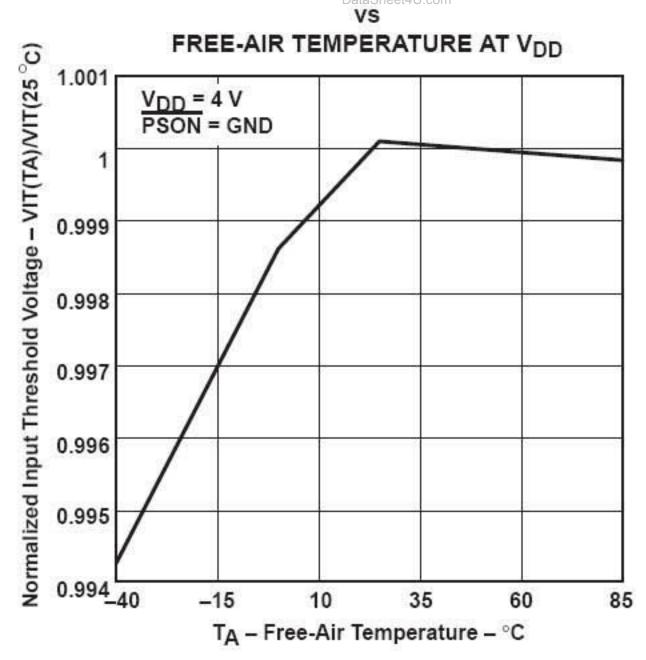


Figure 8

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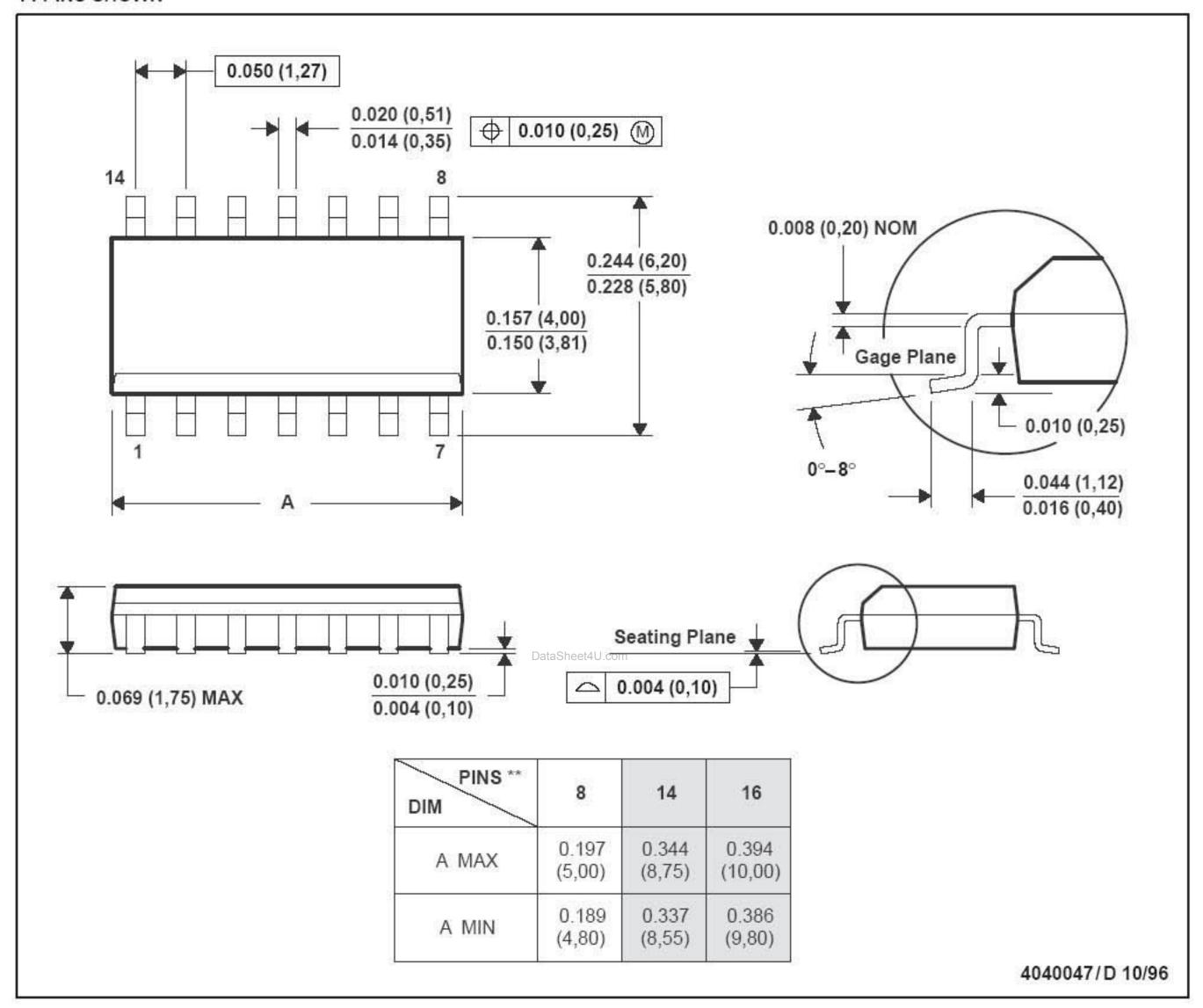
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MECHANICAL DATA

D (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-012

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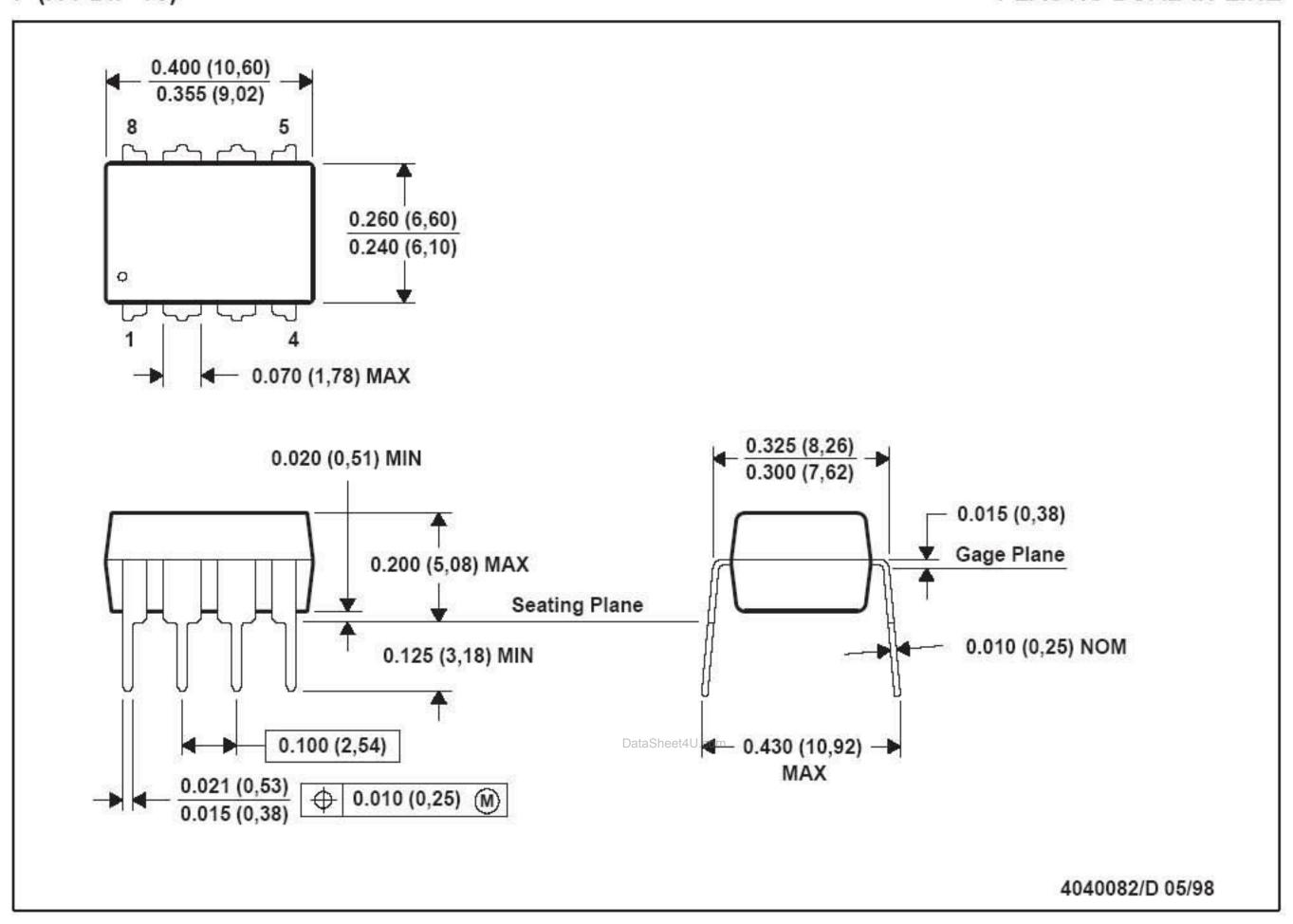
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MECHANICAL DATA

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS-001

For the latest package information, go to http://www.ti.com/sc/docs/package/pkg_info.htm

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