54F/74F841

10-Bit Transparent Latch

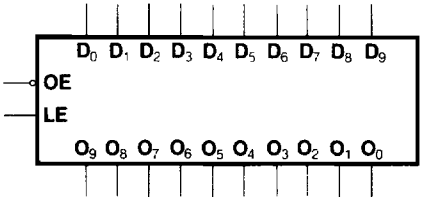
Description

The 'F841 bus interface latch is designed to eliminate the extra packages required to buffer existing latches and provide extra data width for wider address/data paths or buses carrying parity. The 'F841 is a 10-bit transparent latch, a 10-bit version of the 'F373.

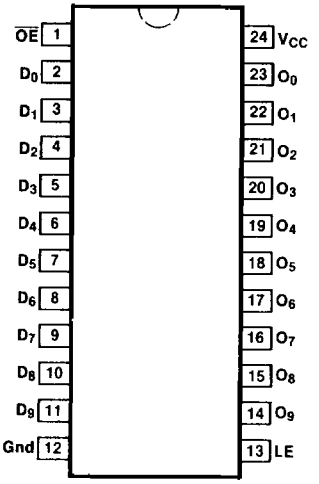
The 'F841 is functionally and pin compatible to AMD's AM29841.

Ordering Code: See Section 5

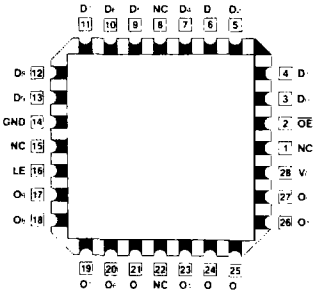
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
D_0-D_9	Data Inputs	0.5/0.375
O_0-O_9	Data Outputs	75/15 (12.5)
$\overline{OE}$	Output Enable	0.5/0.375
LE	Latch Enable	0.5/0.375

Functional Description

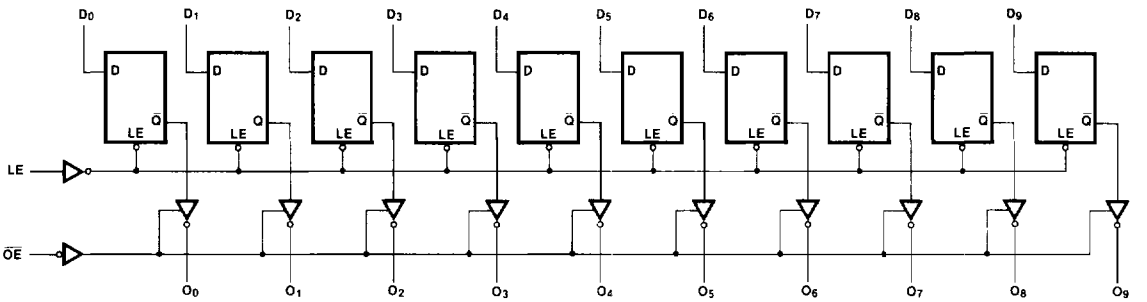
The 'F841 device consists of ten D-type latches with 3-state outputs. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. This allows asynchronous operation, as the output transition follows the data in transition. On the LE HIGH-to-LOW transition, the data that meets the setup and hold time is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH the bus output is in the high impedance state.

Function Table

Inputs			Internal	Output	Function
$\overline{OE}$	LE	D	Q	O	
X	X	X	X	Z	High Z
H	H	L	L	Z	High Z
H	H	H	H	Z	High Z
H	L	X	NC	Z	Latched
L	H	L	L	L	Transparent
L	H	H	H	H	Transparent
L	L	X	NC	NC	Latched
L	X	X	H	H	Preset
L	X	X	L	L	Clear
L	X	X	H	H	Preset
H	L	X	L	Z	Latched
H	L	X	H	Z	Latched

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = HIGH Impedance
NC = No Change

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		50	75	mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF			54F T_A, V_{CC} = Mil C_L = 50 pF		74F T_A, V_{CC} = Com C_L = 50 pF		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay D_n to O_n		8.0 6.0						ns	3-1 3-4
t_{PLH} t_{PHL}	Propagation Delay LE to O_n		13.0 8.0						ns	3-1 3-7
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to O_n		11.0 8.0						ns	3-1 3-12 3-13
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to O_n		7.0 5.0							

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F T_A = +25°C V_{CC} = +5.0 V			54F T_A, V_{CC} = Mil		74F T_A, V_{CC} = Com		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
t_s(H) t_s(L)	Setup Time, HIGH or LOW D_n to LE	3.0 3.0							ns	3-15
t_h(H) t_h(L)	Hold Time, HIGH or LOW D_n to LE	3.0 3.0								
t_w(H)	LE Pulse Width, HIGH	4.0							ns	3-7