Dual 12-/10-/8-Bit SPI V_{OUT} DACs with 10ppm/°C Reference

FEATURES

- **Integrated Precision Reference**
  2.5V Full-Scale 10ppm/°C (LTC2632-L)
  4.096V Full-Scale 10ppm/°C (LTC2632-H)
- **Maximum INL Error: ±1LSB (LTC2632A-12)**
- Low Noise: 0.75mV$_{P-P}$ 0.1Hz to 200kHz
- Guaranteed Monotonic –40°C to 125°C Automotive Temperature Range
- Selectable Internal or External Reference
- 2.7V to 5.5V Supply Range (LTC2632-L)
- Low Power Operation 0.4mA at 3V
- Power-On-Reset to Zero-Scale/Mid-Scale
- Double-Buffered Data Latches
- 8-Lead ThinSOT™ Package

APPLICATIONS

- Mobile Communications
- Process Control and Industrial Automation
- Automatic Test Equipment
- Portable Equipment
- Automotive

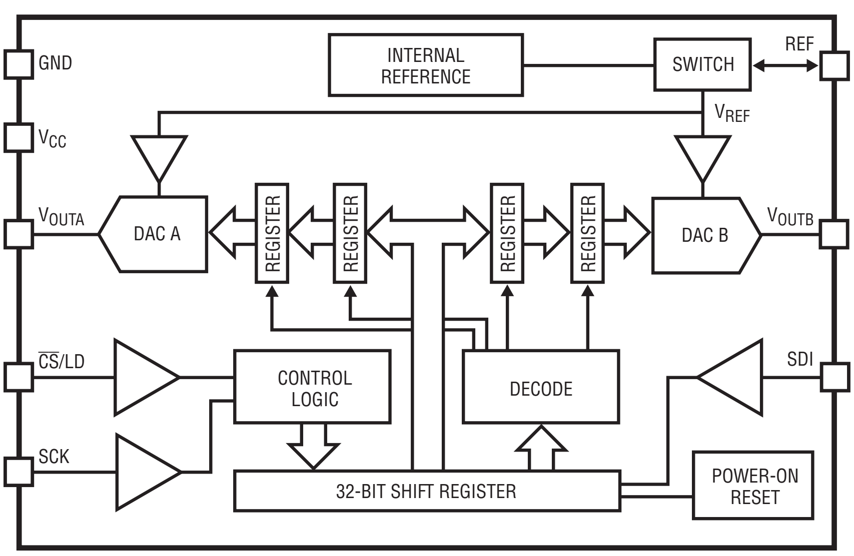
DESCRIPTION

The LTC®2632 is a family of dual 12-, 10-, and 8-bit voltage-output DACs with an integrated, high-accuracy, low-drift reference in an 8-lead TSOT-23 package. It has rail-to-rail output buffers and is guaranteed monotonic.

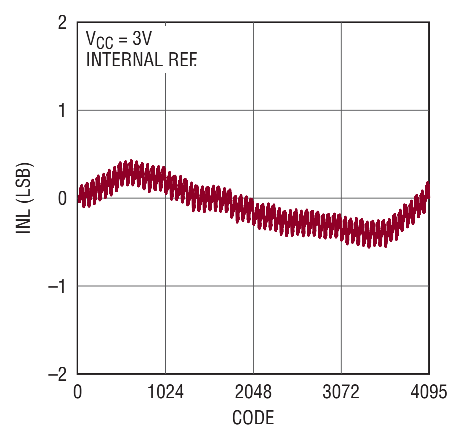
The LTC2632-L has a full-scale output of 2.5V, and operates from a single 2.7V to 5.5V supply. The LTC2632-H has a full-scale output of 4.096V, and operates from a 4.5V to 5.5V supply. Each DAC can also operate with an external reference, which sets the full-scale output to the external reference voltage.

These DACs communicate via a simple SPI/MICROWIRE compatible 3-wire serial interface which operates at clock rates up to 50MHz. The LTC2632 incorporates a power-on reset circuit. Options are available for reset to zero-scale or reset to mid-scale in internal reference mode, or reset to mid-scale in external reference mode after power-up.

BLOCK DIAGRAM



Integral Nonlinearity (LTC2632A-LZ12)



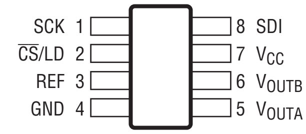
ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltage (V_{CC}) .... –0.3V to 6V
SCK, SDI .... –0.3V to 6V
$\overline{CS}$/LD (Note 11) ....–0.3V to Min (V_{CC} + 0.3V, 6V)
V_{OUTA}, V_{OUTB} ....–0.3V to Min (V_{CC} + 0.3V, 6V)
REF ....–0.3V to Min (V_{CC} + 0.3V, 6V)
Operating Temperature Range
  LTC2632C .... 0°C to 70°C
  LTC2632H (Note 3) .... –40°C to 125°C
Maximum Junction Temperature .... 150°C
Storage Temperature Range .... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)................... 300°C

PIN CONFIGURATION

TOP VIEW



TS8 PACKAGE
8-LEAD PLASTIC TSOT-23
T_{JMAX} = 150°C (NOTE 6), θ_{JA} = 195°C/W

ORDER INFORMATION

LTC2632 A C TS8 –L Z 12 #TRM PBF

- **LEAD FREE DESIGNATOR** (PBF)
- **TAPE AND REEL** (#TRM)
  TR = 2,500-Piece Tape and Reel
  TRM = 500-Piece Tape and Reel
- **RESOLUTION** (12)
  12 = 12-Bit
  10 = 10-Bit
  8 = 8-Bit
- **POWER-ON RESET** (Z)
  MI = Reset to Mid-Scale in Internal Reference Mode
  MX = Reset to Mid-Scale in External Reference Mode (2632-L Only)
  Z = Reset to Zero-Scale in Internal Reference Mode
- **FULL-SCALE VOLTAGE, INTERNAL REFERENCE MODE** (–L)
  L = 2.5V
  H = 4.096V
- **PACKAGE TYPE** (TS8)
  TS8 = 8-Lead Plastic TSOT-23
- **TEMPERATURE GRADE** (C)
  C = Commercial Temperature Range (0°C to 70°C)
  H = Automotive Temperature Range (–40°C to 125°C)
- **ELECTRICAL GRADE (OPTIONAL)** (A)
  A = ±1LSB Maximum INL (12-Bit)
- **PRODUCT PART NUMBER** (LTC2632)

Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

PRODUCT SELECTION GUIDE

PART NUMBER	PART MARKING*	V_{FS} WITH INTERNAL REFERENCE	POWER-ON RESET TO CODE	POWER-ON REFERENCE MODE	RESOLUTION	V_{CC}	MAXIMUM INL
LTC2632A-LMI12	LTFSJ	2.5V • (4095/4096)	Mid-Scale	Internal	12-Bit	2.7V to 5.5V	±1LSB
LTC2632A-LMX12	LTFSH	2.5V • (4095/4096)	Mid-Scale	External	12-Bit	2.7V to 5.5V	±1LSB
LTC2632A-LZ12	LTFSG	2.5V • (4095/4096)	Zero	Internal	12-Bit	2.7V to 5.5V	±1LSB
LTC2632A-HMI12	LTFSM	4.096V • (4095/4096)	Mid-Scale	Internal	12-Bit	4.5V to 5.5V	±1LSB
LTC2632A-HZ12	LTFSK	4.096V • (4095/4096)	Zero	Internal	12-Bit	4.5V to 5.5V	±1LSB
LTC2632-LMI12	LTFSJ	2.5V • (4095/4096)	Mid-Scale	Internal	12-Bit	2.7V to 5.5V	±2.5LSB
LTC2632-LMI10	LTFSQ	2.5V • (1023/1024)	Mid-Scale	Internal	10-Bit	2.7V to 5.5V	±1LSB
LTC2632-LMI8	LTFSW	2.5V • (255/256)	Mid-Scale	Internal	8-Bit	2.7V to 5.5V	±0.5LSB
LTC2632-LMX12	LTFSH	2.5V • (4095/4096)	Mid-Scale	External	12-Bit	2.7V to 5.5V	±2.5LSB
LTC2632-LMX10	LTFSP	2.5V • (1023/1024)	Mid-Scale	External	10-Bit	2.7V to 5.5V	±1LSB
LTC2632-LMX8	LTFSV	2.5V • (255/256)	Mid-Scale	External	8-Bit	2.7V to 5.5V	±0.5LSB
LTC2632-LZ12	LTFSG	2.5V • (4095/4096)	Zero	Internal	12-Bit	2.7V to 5.5V	±2.5LSB
LTC2632-LZ10	LTFSN	2.5V • (1023/1024)	Zero	Internal	10-Bit	2.7V to 5.5V	±1LSB
LTC2632-LZ8	LTFST	2.5V • (255/256)	Zero	Internal	8-Bit	2.7V to 5.5V	±0.5LSB
LTC2632-HMI12	LTFSM	4.096V • (4095/4096)	Mid-Scale	Internal	12-Bit	4.5V to 5.5V	±2.5LSB
LTC2632-HMI10	LTFSS	4.096V • (1023/1024)	Mid-Scale	Internal	10-Bit	4.5V to 5.5V	±1LSB
LTC2632-HMI8	LTFSY	4.096V • (255/256)	Mid-Scale	Internal	8-Bit	4.5V to 5.5V	±0.5LSB
LTC2632-HZ12	LTFSK	4.096V • (4095/4096)	Zero	Internal	12-Bit	4.5V to 5.5V	±2.5LSB
LTC2632-HZ10	LTFSR	4.096V • (1023/1024)	Zero	Internal	10-Bit	4.5V to 5.5V	±1LSB
LTC2632-HZ8	LTFSX	4.096V • (255/256)	Zero	Internal	8-Bit	4.5V to 5.5V	±0.5LSB

* The temperature grade is identified by a label on the shipping container.
Above options are available in an 8-lead TSOT package (LTC2632xTS8).

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 2.7V to 5.5V, V_{OUT} unloaded unless otherwise specified.

LTC2632-LMI12/-LMI10/-LMI8/-LMX12/-LMX10/-LMX8/-LZ12/-LZ10/-LZ8, LTC2632A-LMI12/-LMX12/-LZ12 (V_{FS} = 2.5V)

SYMBOL	PARAMETER	CONDITIONS		LTC2632-8			LTC2632-10			LTC2632-12			LTC2632A-12			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
DC Performance																
	Resolution		●	8			10			12			12			Bits
	Monotonicity	V_{CC} = 3V, Internal Ref. (Note 4)	●	8			10			12			12			Bits
DNL	Differential Nonlinearity	V_{CC} = 3V, Internal Ref. (Note 4)	●			±0.5			±0.5			±1			±1	LSB
INL	Integral Nonlinearity	V_{CC} = 3V, Internal Ref. (Note 4)	●		±0.05	±0.5		±0.2	±1		±1	±2.5		±0.5	±1	LSB
ZSE	Zero-Scale Error	V_{CC} = 3V, Internal Ref., Code = 0	●		0.5	5		0.5	5		0.5	5		0.5	5	mV
V_{OS}	Offset Error	V_{CC} = 3V, Internal Ref. (Note 5)	●		±0.5	±5		±0.5	±5		±0.5	±5		±0.5	±5	mV
V_{OSTC}	V_{OS} Temperature Coefficient	V_{CC} = 3V, Internal Ref.			±10			±10			±10			±10		μV/°C
GE	Gain Error	V_{CC} = 3V, Internal Ref.	●		0.2	0.8		0.2	0.8		0.2	0.8		0.2	0.8	%FSR
GE_{TC}	Gain Temperature Coefficient	V_{CC} = 3V, Internal Ref. (Note 10) C-Grade H-Grade			 10 10			 10 10			 10 10			 10 10		 ppm/°C ppm/°C
	Load Regulation	Internal Ref., Mid-Scale, V_{CC} = 3V±10%, –5mA ≤ I_{OUT} ≤ 5mA V_{CC} = 5V±10%, –10mA ≤ I_{OUT} ≤ 10mA	● ●		0.009 0.009	0.016 0.016		0.035 0.035	0.064 0.064		0.14 0.14	0.256 0.256		0.14 0.14	0.256 0.256	LSB/mA LSB/mA
R_{OUT}	DC Output Impedance	Internal Ref., Mid-Scale, V_{CC} = 3V±10%, –5mA ≤ I_{OUT} ≤ 5mA V_{CC} = 5V±10%, –10mA ≤ I_{OUT} ≤ 10mA	● ●		0.09 0.09	0.156 0.156		0.09 0.09	0.156 0.156		0.09 0.09	0.156 0.156		0.09 0.09	0.156 0.156	Ω Ω

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OUT}	DAC Output Span	External Reference Internal Reference			0 to V_{REF} 0 to 2.5		V V
PSR	Power Supply Rejection	V_{CC} = 3V±10% or 5V±10%			–80		dB
I_{SC}	Short-Circuit Output Current (Note 6) Sinking Sourcing	V_{FS} = V_{CC} = 5.5V Zero-Scale; V_{OUT} Shorted to V_{CC} Full-Scale; V_{OUT} Shorted to GND	 ● ●		 27 –28	 48 –48	 mA mA
Power Supply							
V_{CC}	Positive Supply Voltage	For Specified Performance	●	2.7		5.5	V
I_{CC}	Supply Current (Note 7)	V_{CC} = 3V, V_{REF} = 2.5V, External Reference V_{CC} = 3V, Internal Reference V_{CC} = 5V V_{REF} = 2.5V, External Reference V_{CC} = 5V, Internal Reference	● ● ● ●		0.3 0.4 0.3 0.4	0.5 0.6 0.5 0.6	mA mA mA mA
I_{SD}	Supply Current in Power-Down Mode (Note 7)	V_{CC} = 5V	●		0.5	2	μA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 2.7V to 5.5V, V_{OUT} unloaded unless otherwise specified.

LTC2632-LMI12/-LMI10/-LMI8/-LMX12/-LMX10/-LMX8/-LZ12/-LZ10/-LZ8, LTC2632A-LMI12/-LMX12/-LZ12 (V_{FS} = 2.5V)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Reference Input							
	Input Voltage Range		●	1		V_{CC}	V
	Resistance		●	120	160	200	kΩ
	Capacitance				12		pF
I_{REF}	Reference Current, Power-Down Mode	DAC Powered Down	●		0.005	5.0	µA
Reference Output							
	Output Voltage		●	1.24	1.25	1.26	V
	Reference Temperature Coefficient				±10		ppm/°C
	Output Impedance				0.5		kΩ
	Capacitive Load Driving				10		µF
	Short-Circuit Current	V_{CC} = 5.5V, REF Shorted to GND			2.5		mA
Digital I/O							
V_{IH}	Digital Input High Voltage	V_{CC} = 3.6V to 5.5V V_{CC} = 2.7V to 3.6V	● ●	2.4 2.0			V V
V_{IL}	Digital Input Low Voltage	V_{CC} = 4.5V to 5.5V V_{CC} = 2.7V to 4.5V	● ●			0.8 0.6	V V
I_{LK}	Digital Input Leakage	V_{IN} = GND to V_{CC}	●			±1	µA
C_{IN}	Digital Input Capacitance	(Note 8)	●			8	pF
AC Performance							
t_S	Settling Time	V_{CC} = 3V (Note 9) ±0.39% (±1LSB at 8 Bits) ±0.098% (±1LSB at 10 Bits) ±0.024% (±1LSB at 12 Bits)			 3.5 3.9 4.4		 µs µs µs
	Voltage Output Slew Rate				1.0		V/µs
	Capacitive Load Driving				500		pF
	Glitch Impulse	At Mid-Scale Transition			2.8		nV•s
	DAC-to-DAC Crosstalk	1 DAC Held at FS, 1 DAC Switch 0 to FS			4.5		nV•s
	Multiplying Bandwidth	External Reference			320		kHz
e_n	Output Voltage Noise Density	At f = 1kHz, External Reference At f = 10kHz, External Reference At f = 1kHz, Internal Reference At f = 10kHz, Internal Reference			180 160 200 180		$nV/\sqrt{Hz}$ $nV/\sqrt{Hz}$ $nV/\sqrt{Hz}$ $nV/\sqrt{Hz}$
	Output Voltage Noise	0.1Hz to 10Hz, External Reference 0.1Hz to 10Hz, Internal Reference 0.1Hz to 200kHz, External Reference 0.1Hz to 200kHz, Internal Reference C_{REF} = 0.1µF			30 35 680 730		$µV_{P-P}$ $µV_{P-P}$ $µV_{P-P}$ $µV_{P-P}$

TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 2.7V to 5.5V, V_{OUT} unloaded unless otherwise specified.

LTC2632-LMI12/-LMI10/-LMI8/-LMX12/-LMX10/-LMX8/-LZ12/-LZ10/-LZ8, LTC2632A-LMI12/-LMX12/-LZ12 (V_{FS} = 2.5V)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_1	SDI Valid to SCK Setup	(Figure 1)	●	4			ns
t_2	SDI Valid to SCK Hold	(Figure 1)	●	4			ns
t_3	SCK High Time	(Figure 1)	●	9			ns
t_4	SCK Low Time	(Figure 1)	●	9			ns
t_5	$\overline{CS}$/LD Pulse Width	(Figure 1)	●	10			ns
t_6	LSB SCK High to $\overline{CS}$/LD High	(Figure 1)	●	7			ns
t_7	$\overline{CS}$/LD Low to SCK High	(Figure 1)	●	7			ns
t_{10}	$\overline{CS}$/LD High to SCK Positive Edge	(Figure 1)	●	7			ns
	SCK Frequency	50% Duty Cycle	●			50	MHz

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 4.5V to 5.5V, V_{OUT} unloaded unless otherwise specified.

LTC2632-HMI12/-HMI10/-HMI8/-HZ12/-HZ10/-HZ8, LTC2632A-HMI12/-HZ12 (V_{FS} = 4.096V)

SYMBOL	PARAMETER	CONDITIONS		LTC2632-8			LTC2632-10			LTC2632-12			LTC2632A-12			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
DC Performance																
	Resolution		●	8			10			12			12			Bits
	Monotonicity	V_{CC} = 5V, Internal Ref. (Note 4)	●	8			10			12			12			Bits
DNL	Differential Nonlinearity	V_{CC} = 5V, Internal Ref. (Note 4)	●			±0.5			±0.5			±1			±1	LSB
INL	Integral Nonlinearity	V_{CC} = 5V, Internal Ref. (Note 4)	●		±0.05	±0.5		±0.2	±1		±1	±2.5		±0.5	±1	LSB
ZSE	Zero-Scale Error	V_{CC} = 5V, Internal Ref., Code = 0	●		0.5	5		0.5	5		0.5	5		0.5	5	mV
V_{OS}	Offset Error	V_{CC} = 5V, Internal Ref. (Note 5)	●		±0.5	±5		±0.5	±5		±0.5	±5		±0.5	±5	mV
V_{OSTC}	V_{OS} Temperature Coefficient	V_{CC} = 5V, Internal Ref.			±10			±10			±10			±10		μV/°C
GE	Gain Error	V_{CC} = 5V, Internal Ref.	●		0.2	0.8		0.2	0.8		0.2	0.8		0.2	0.8	%FSR
GE_{TC}	Gain Temperature Coefficient	V_{CC} = 5V, Internal Ref. (Note 10) C-Grade H-Grade			 10 10			 10 10			 10 10			 10 10		 ppm/°C ppm/°C
	Load Regulation	V_{CC} = 5V±10%, Internal Ref. Mid-Scale, –10mA ≤ I_{OUT} ≤ 10mA	●		0.006	0.01		0.022	0.04		0.09	0.16		0.09	0.16	LSB/mA
R_{OUT}	DC Output Impedance	V_{CC} = 5V±10%, Internal Ref. Mid-Scale, –10mA ≤ I_{OUT} ≤ 10mA	●		0.09	0.156		0.09	0.156		0.09	0.156		0.09	0.156	Ω

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OUT}	DAC Output Span	External Reference Internal Reference			0 to V_{REF} 0 to 4.096		V V
PSR	Power Supply Rejection	V_{CC} = 5V±10%			–80		dB
I_{SC}	Short-Circuit Output Current (Note 6) Sinking Sourcing	V_{FS} = V_{CC} = 5.5V Zero-Scale; V_{OUT} Shorted to V_{CC} Full-Scale; V_{OUT} Shorted to GND	 ● ●		 27 –28	 48 –48	 mA mA
Power Supply							
V_{CC}	Positive Supply Voltage	For Specified Performance	●	4.5		5.5	V
I_{CC}	Supply Current (Note 7)	V_{CC} = 5V, V_{REF} = 4.096V, External Reference V_{CC} = 5V, Internal Reference	● ●		0.4 0.5	0.6 0.7	mA mA
I_{SD}	Supply Current in Power-Down Mode (Note 7)	V_{CC} = 5V	●		0.5	2	μA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 4.5V to 5.5V, V_{OUT} unloaded unless otherwise specified.

LTC2632-HMI12/-HMI10/-HMI8/-HZ12/-HZ10/-HZ8, LTC2632A-HMI12/-HZ12 (V_{FS} = 4.096V)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Reference Input							
	Input Voltage Range		●	1		V_{CC}	V
	Resistance		●	120	160	200	kΩ
	Capacitance				12		pF
I_{REF}	Reference Current, Power-Down Mode	DAC Powered Down	●		0.005	5.0	µA
Reference Output							
	Output Voltage		●	2.032	2.048	2.064	V
	Reference Temperature Coefficient				±10		ppm/°C
	Output Impedance				0.5		kΩ
	Capacitive Load Driving				10		µF
	Short-Circuit Current	V_{CC} = 5.5V; REF Shorted to GND			4		mA
Digital I/O							
V_{IH}	Digital Input High Voltage		●	2.4			V
V_{IL}	Digital Input Low Voltage		●			0.8	V
I_{LK}	Digital Input Leakage	V_{IN} = GND to V_{CC}	●			±1	µA
C_{IN}	Digital Input Capacitance	(Note 8)	●			8	pF
AC Performance							
t_S	Settling Time	V_{CC} = 5V (Note 9) ±0.39% (±1LSB at 8 Bits) ±0.098% (±1LSB at 10 Bits) ±0.024% (±1LSB at 12 Bits)			 3.9 4.1 4.9		 µs µs µs
	Voltage Output Slew Rate				1.0		V/µs
	Capacitive Load Driving				500		pF
	Glitch Impulse	At Mid-Scale Transition			3.0		nV•s
	DAC-to-DAC Crosstalk	1 DAC Held at FS, 1 DAC Switch 0 to FS			6.7		nV•s
	Multiplying Bandwidth	External Reference			320		kHz
e_n	Output Voltage Noise Density	At f = 1kHz, External Reference At f = 10kHz, External Reference At f = 1kHz, Internal Reference At f = 10kHz, Internal Reference			180 160 250 230		$nV/\sqrt{Hz}$ $nV/\sqrt{Hz}$ $nV/\sqrt{Hz}$ $nV/\sqrt{Hz}$
	Output Voltage Noise	0.1Hz to 10Hz, External Reference 0.1Hz to 10Hz, Internal Reference 0.1Hz to 200kHz, External Reference 0.1Hz to 200kHz, Internal Reference C_{REF} = 0.1µF			30 40 680 750		$µV_{P-P}$ $µV_{P-P}$ $µV_{P-P}$ $µV_{P-P}$

LINEAR TECHNOLOGY

TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 4.5V to 5.5V, V_{OUT} unloaded unless otherwise specified.

LTC2632-HMI12/-HMI10/-HMI8/-HZ12/-HZ10/-HZ8, LTC2632A-HMI12/-HZ12 (V_{FS} = 4.096V)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_1	SDI Valid to SCK Setup	(Figure 1)	●	4			ns
t_2	SDI Valid to SCK Hold	(Figure 1)	●	4			ns
t_3	SCK High Time	(Figure 1)	●	9			ns
t_4	SCK Low Time	(Figure 1)	●	9			ns
t_5	$\overline{CS}$/LD Pulse Width	(Figure 1)	●	10			ns
t_6	LSB SCK High to $\overline{CS}$/LD High	(Figure 1)	●	7			ns
t_7	$\overline{CS}$/LD Low to SCK High	(Figure 1)	●	7			ns
t_{10}	$\overline{CS}$/LD High to SCK Positive Edge	(Figure 1)	●	7			ns
	SCK Frequency	50% Duty Cycle	●			50	MHz

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltages are with respect to GND

Note 3: High temperatures degrade operating lifetimes. Operating lifetime is derated at temperatures greater than 105°C.

Note 4: Linearity and monotonicity are defined from code k_L to code 2^N–1, where N is the resolution and k_L is given by $k_L = 0.016•(2^N/V_{FS})$, rounded to the nearest whole code. For V_{FS} = 2.5V and N = 12, k_L = 26 and linearity is defined from code 26 to code 4,095. For V_{FS} = 4.096V and N = 12, k_L = 16 and linearity is defined from code 16 to code 4,095.

Note 5: Inferred from measurement at code 16 (LTC2632-12), code 4 (LTC2632-10) or code 1 (LTC2632-8), and at full-scale.

Note 6: This IC includes current limiting that is intended to protect the device during momentary overload conditions. Junction temperature can exceed the rated maximum during current limiting. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 7: Digital inputs at 0V or V_{CC}.

Note 8: Guaranteed by design and not production tested.

Note 9: Internal Reference mode. DAC is stepped 1/4 scale to 3/4 scale and 3/4 scale to 1/4 scale. Load is 2kΩ in parallel with 100pF to GND.

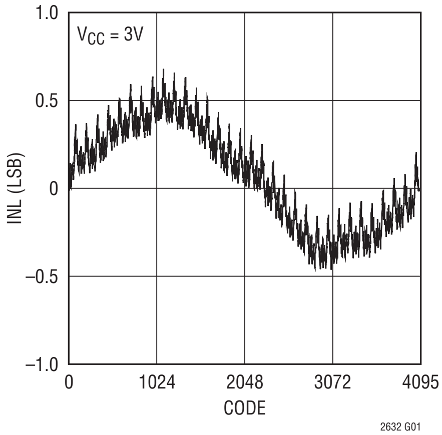
Note 10: Temperature coefficient is calculated by dividing the maximum change in output voltage by the specified temperature range.

Note 11: $\overline{CS}$/LD can be held at high voltage as V_{CC} ramps upon power-up.

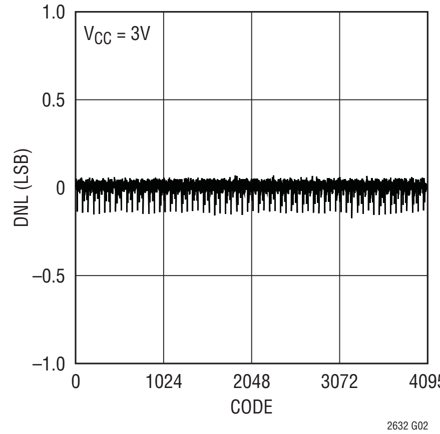
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted. LTC2632-L12 (Internal Reference, V_{FS} = 2.5V)

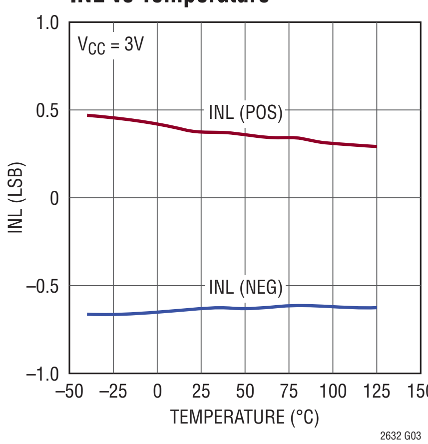
Integral Nonlinearity (INL)



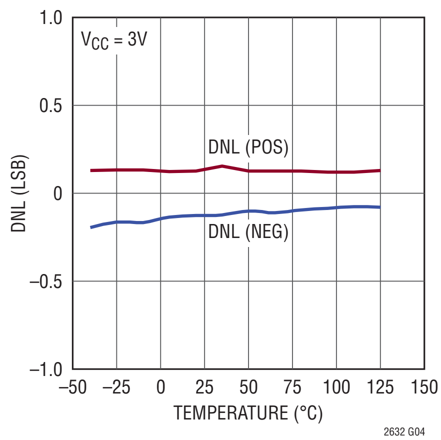
Differential Nonlinearity (DNL)



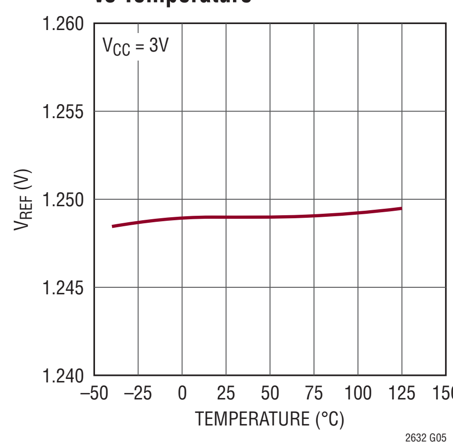
INL vs Temperature



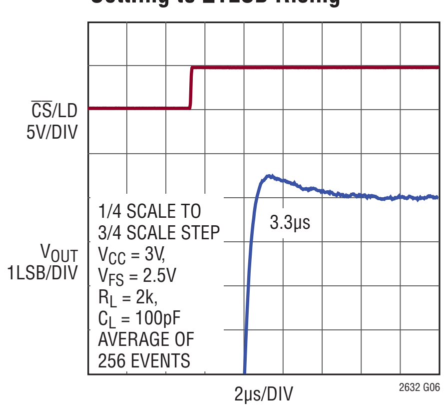
DNL vs Temperature



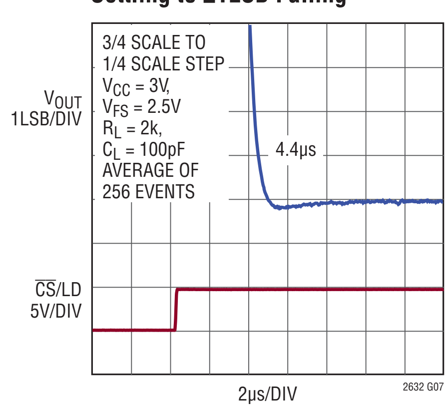
Reference Output Voltage vs Temperature



Settling to ±1LSB Rising



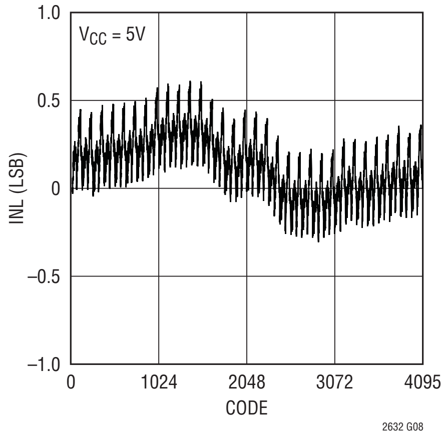
Settling to ±1LSB Falling



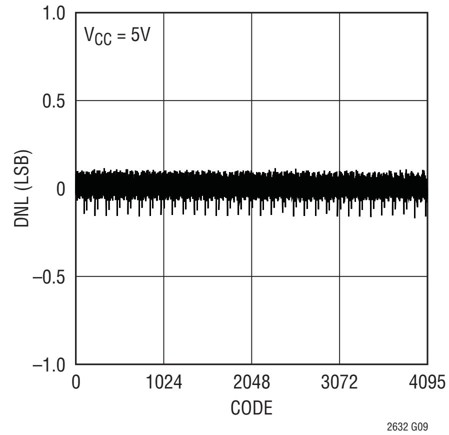
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted. LTC2632-H12 (Internal Reference, V_{FS} = 4.096V)

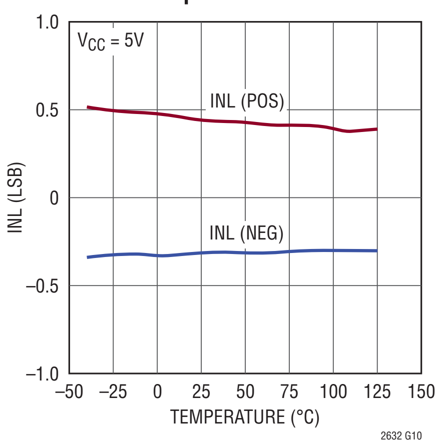
Integral Nonlinearity (INL)



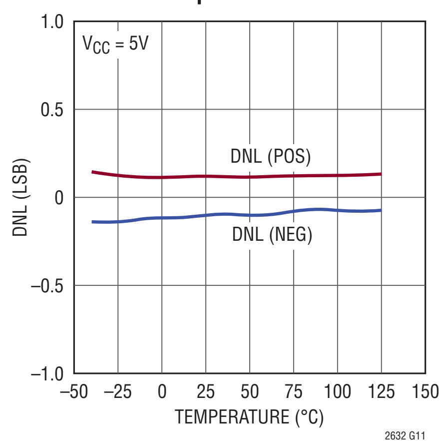
Differential Nonlinearity (DNL)



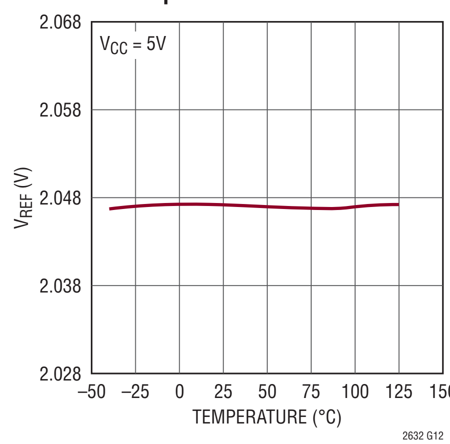
INL vs Temperature



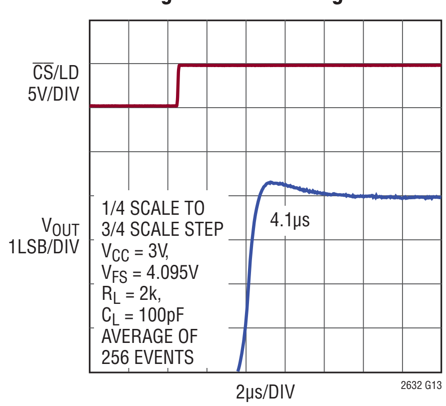
DNL vs Temperature



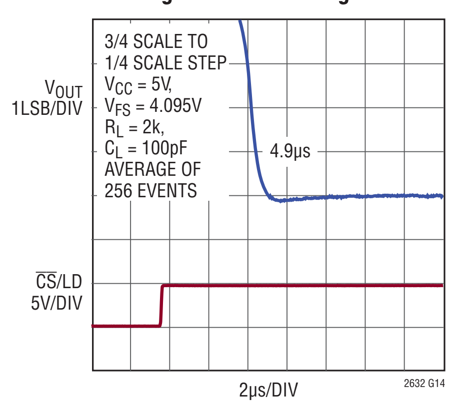
Reference Output Voltage vs Temperature



Settling to ±1LSB Rising



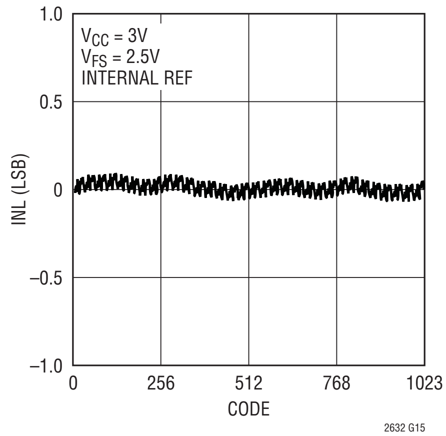
Settling to ±1LSB Falling



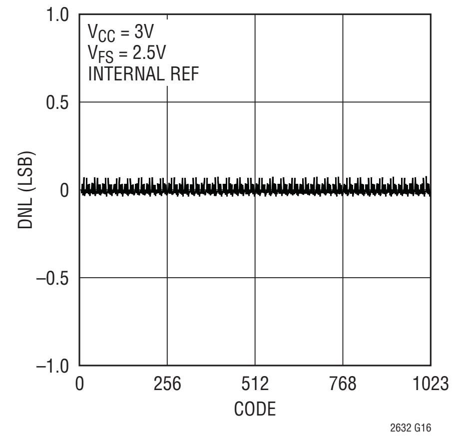
TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25°C$, unless otherwise noted.

LTC2632-10

Integral Nonlinearity (INL)

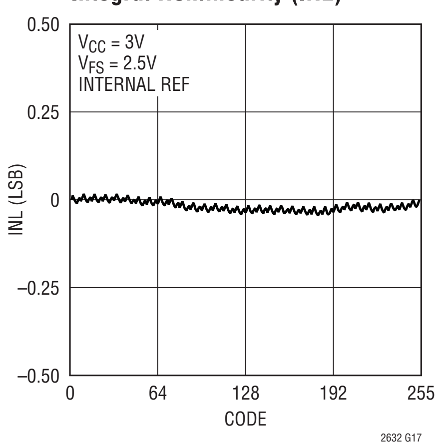


Differential Nonlinearity (DNL)

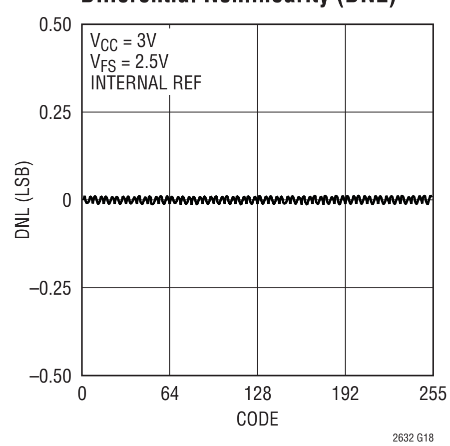


LTC2632-8

Integral Nonlinearity (INL)

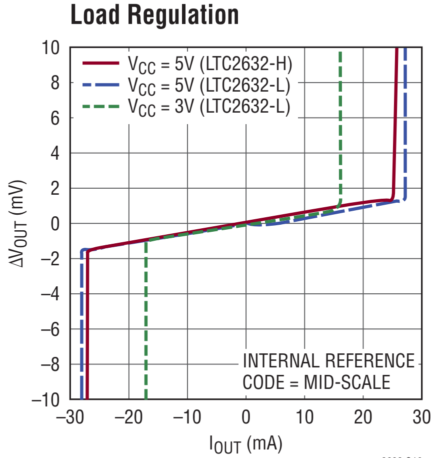


Differential Nonlinearity (DNL)

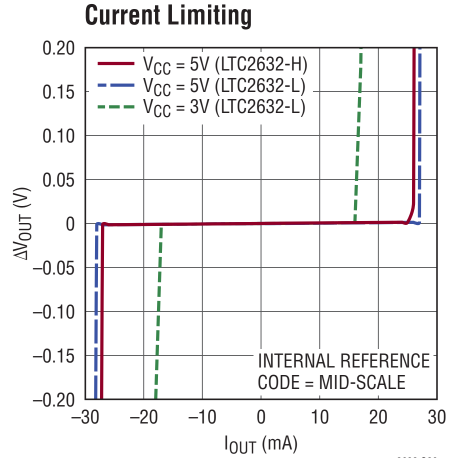


LTC2632

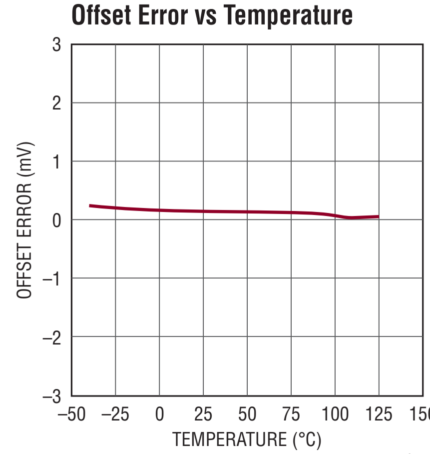
Load Regulation



Current Limiting



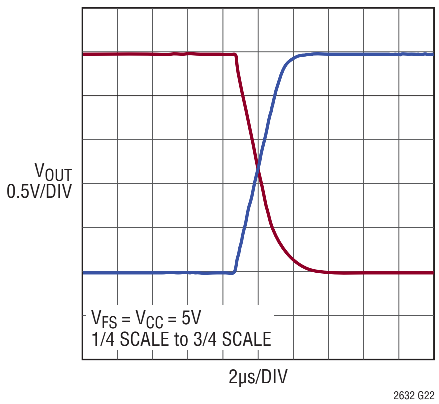
Offset Error vs Temperature



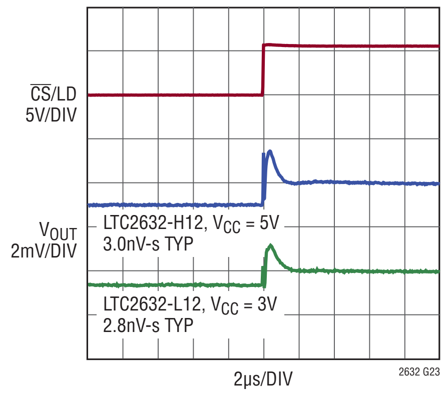
TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25°C$, unless otherwise noted.

LTC2632

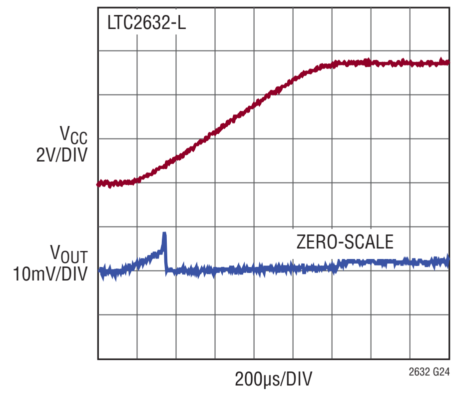
Large-Signal Response



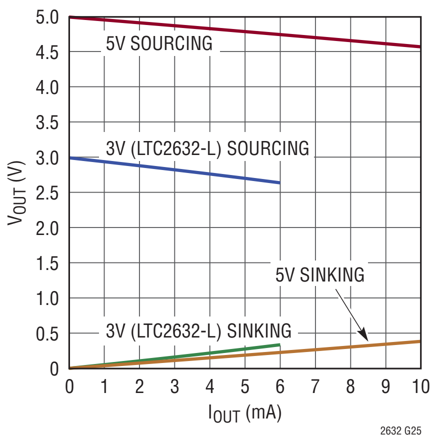
Mid-Scale Glitch Impulse



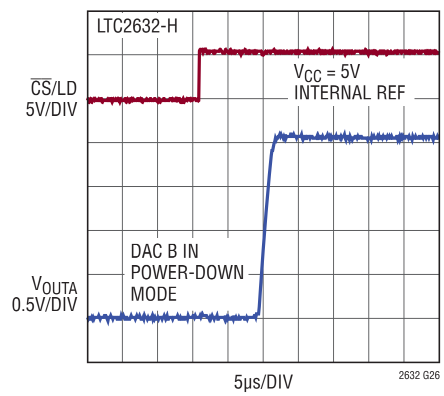
Power-On Reset Glitch



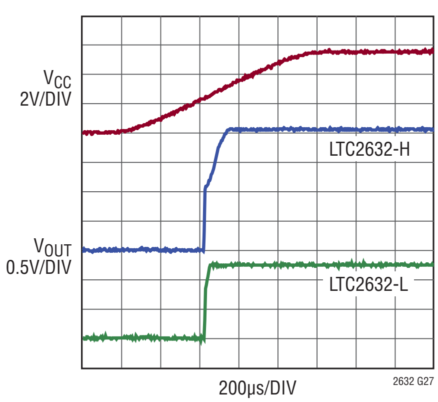
Headroom at Rails vs Output Current



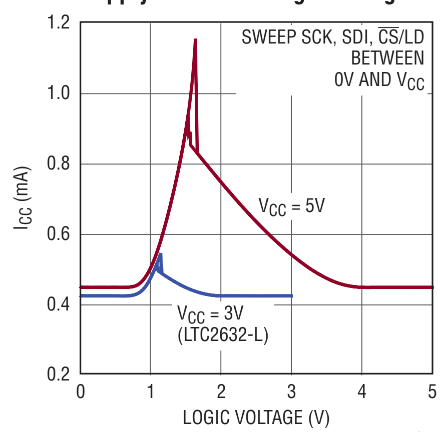
Exiting Power-Down to Mid-Scale



Power-On Reset to Mid-Scale

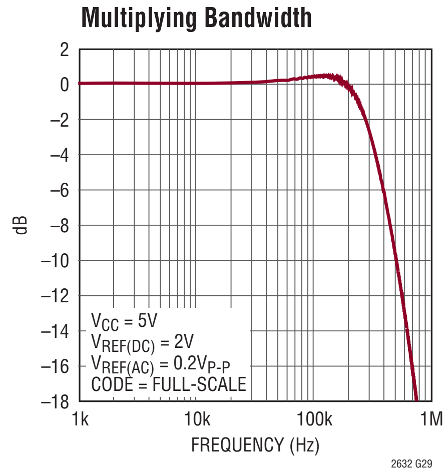


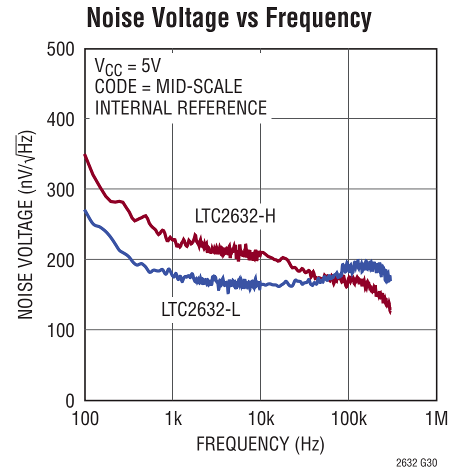
Supply Current vs Logic Voltage

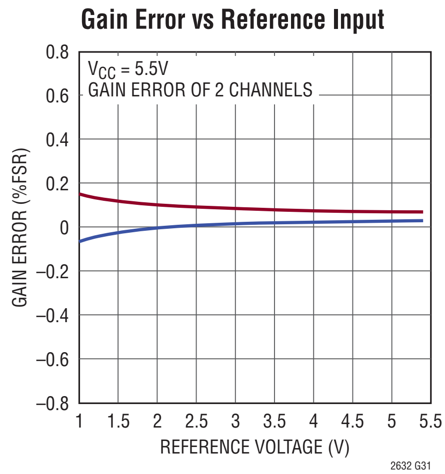


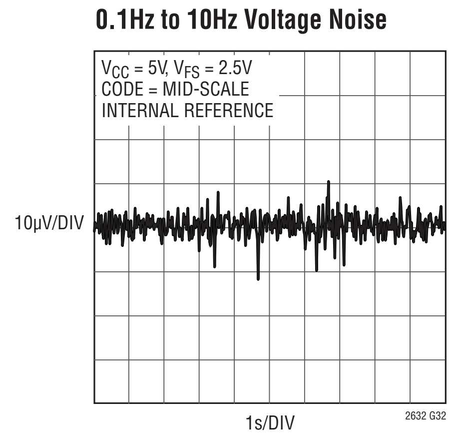
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

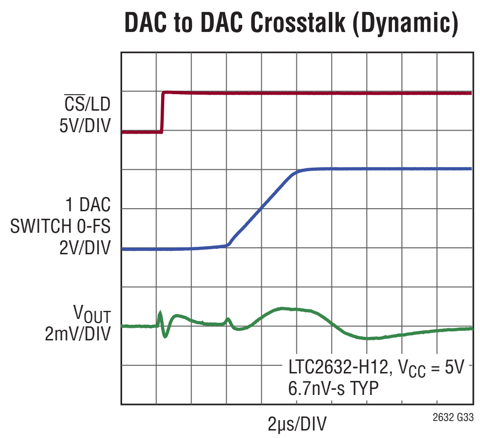
LTC2632

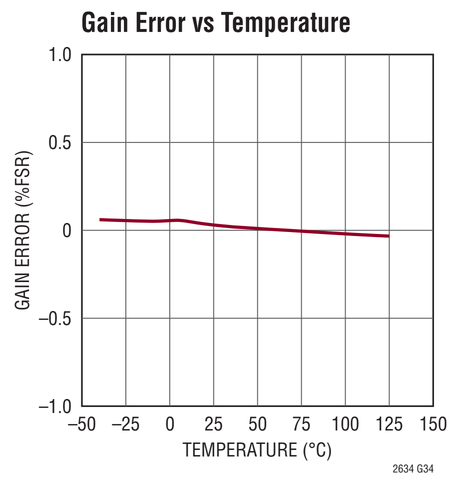












PIN FUNCTIONS

SCK (Pin 1): Serial Interface Clock Input. CMOS and TTL compatible.

$\overline{CS}$/LD (Pin 2): Serial Interface Chip Select/Load Input. When $\overline{CS}$/LD is low, SCK is enabled for shifting data on SDI into the register. When $\overline{CS}$/LD is taken high, SCK is disabled and the specified command (see Table 1) is executed.

REF (Pin 3): Reference Voltage Input or Output. When external reference mode is selected, REF is an input ($1V \le V_{REF} \le V_{CC}$) where the voltage supplied sets the full-scale DAC output voltage. When internal reference is selected, the 10ppm/°C 1.25V (LTC2632-L) or 2.048V (LTC2632-H) internal reference (half full-scale) is available at the pin. This output may be bypassed to GND with up to 10µF (0.1µF is recommended) and must be buffered when driving external DC load current.

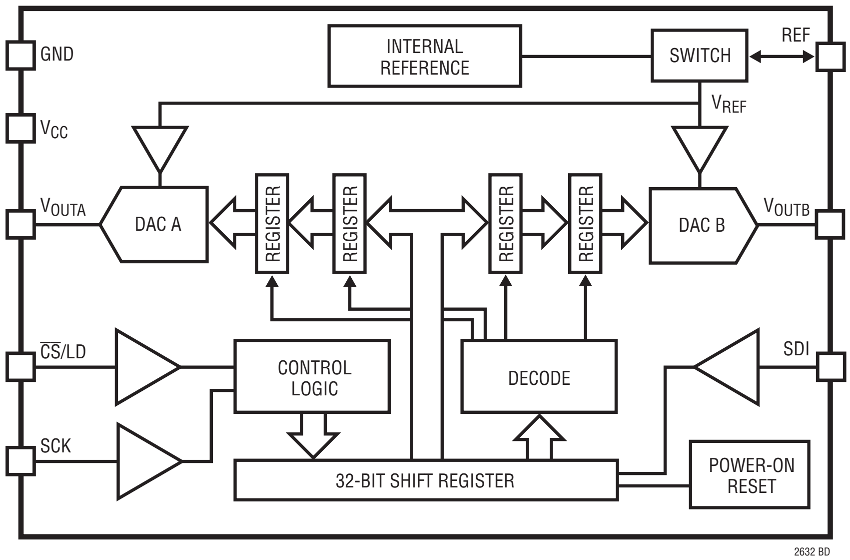
GND (Pin 4): Ground.

V_{OUT} A, V_{OUT} B (Pins 5, 6): DAC Analog Voltage Output.

V_{CC} (Pin 7): Supply Voltage Input. $2.7V \le V_{CC} \le 5.5V$ (LTC2632-L) or $4.5V \le V_{CC} \le 5.5V$ (LTC2632-H). Bypass to GND with a 0.1µF capacitor.

SDI (Pin 8): Serial Interface Data Input. Data on SDI is clocked into the DAC on the rising edge of SCK. The LTC2632 accepts input word lengths of either 24 or 32 bits.

BLOCK DIAGRAM



TIMING DIAGRAM

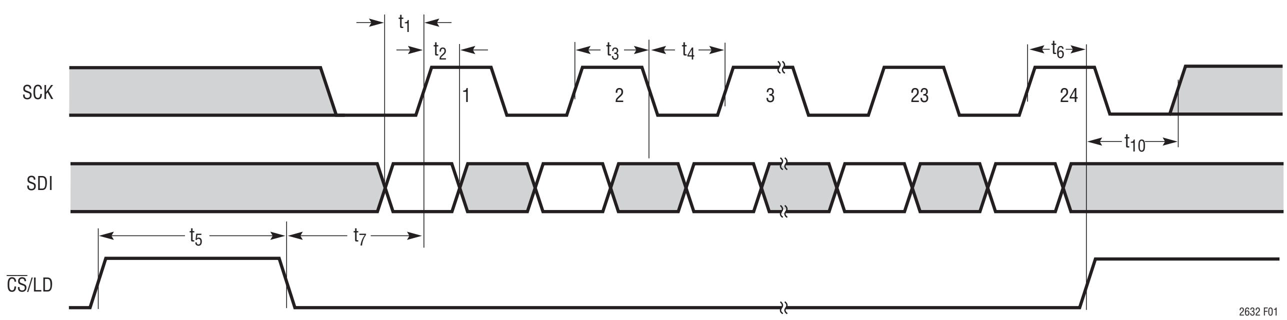


Figure 1. Serial Interface Timing

OPERATION

The LTC2632 is a family of dual voltage output DACs in an 8-lead TSOT package. Each DAC can operate rail-to-rail using an external reference, or with its full-scale voltage set by an integrated reference. Fifteen combinations of accuracy (12-, 10-, and 8-bit), power-on reset value (zero-scale, mid-scale in internal reference mode, or mid-scale in external reference mode), and full-scale voltage (2.5V or 4.096V) are available. The LTC2632 is controlled using a 3-wire SPI/MICROWIRE compatible interface.

Power-On Reset

The LTC2632-HZ/LTC2632-LZ clear the output to zero-scale when power is first applied, making system initialization consistent and repeatable.

For some applications, downstream circuits are active during DAC power-up, and may be sensitive to nonzero outputs from the DAC during this time. The LTC2632 contains circuitry to reduce the power-on glitch: the analog output typically rises less than 10mV above zero-scale during power-on if the power supply is ramped to 5V in 1ms or more. In general, the glitch amplitude decreases as the power supply ramp time is increased. See "Power-On Reset Glitch" in the Typical Performance Characteristics section.

The LTC2632-HMI/LTC2632-LMI/LTC2632-LMX provides an alternative reset, setting the output to mid-scale when power is first applied. The LTC2632-LMI and LTC2632-HMI power-up in internal reference mode, with the output set to a mid-scale voltage of 1.25V and 2.048V respectively. The LTC2632-LMX powers up in external reference mode, with the output set to mid-scale of the external reference. Default reference mode selection is described in the Reference Modes section.

Power Supply Sequencing

The voltage at REF (Pin 3) must be kept within the range $-0.3V \le V_{REF} \le V_{CC} + 0.3V$ (see the Absolute Maximum Ratings section). Particular care should be taken to observe these limits during power supply turn-on and turn-off sequences, when the voltage at V_{CC} is in transition.

Transfer Function

The digital-to-analog transfer function is

$$V_{OUT(IDEAL)} = \left(\frac{k}{2^N}\right) \bullet V_{REF}$$

where k is the decimal equivalent of the binary DAC input code, N is the resolution, and V_{REF} is either 2.5V (LTC2632-LMI/LTC2632-LMX/LTC2632-LZ) or 4.096V (LTC2632-HMI/LTC2632-HZ) when in internal reference mode, and the voltage at REF when in external reference mode.

Table 1. Command Codes

COMMAND*				
C3	**C2**	**C1**	**C0**	
0	0	0	0	Write to Input Register *n*
0	0	0	1	Update (Power-Up) DAC Register *n*
0	0	1	0	Write to Input Register n, Update (Power-Up) All
0	0	1	1	Write to and Update (Power-Up) DAC Register *n*
0	1	0	0	Power-Down *n*
0	1	0	1	Power-Down Chip (All DAC's and Reference)
0	1	1	0	Select Internal Reference (Power-Up Reference)
0	1	1	1	Select External Reference (Power-Down Internal Reference)
1	1	1	1	No Operation

*Command codes not shown are reserved and should not be used.

Table 2. Address Codes

ADDRESS (*n*)*				
A3	**A2**	**A1**	**A0**	
0	0	0	0	DAC A
0	0	0	1	DAC B
1	1	1	1	All DACs

* Address codes not shown are reserved and should not be used.

OPERATION

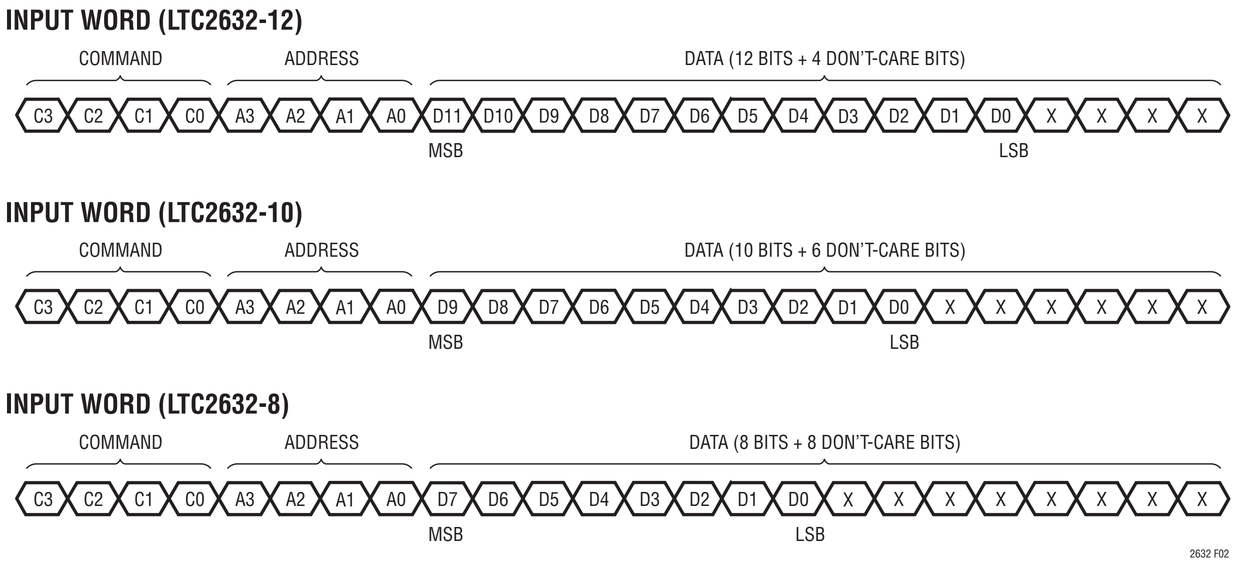


Figure 2. Command and Data Input Format

Serial Interface

The $\overline{CS}$/LD input is level triggered. When this input is taken low, it acts as a chip-select signal, enabling the SDI and SCK buffers and the input shift register. Data (SDI input) is transferred at the next 24 rising SCK edges. The 4-bit command, C3-C0, is loaded first; then the 4-bit DAC address, A3-A0; and finally the 16-bit data word. The data word comprises the 12-, 10- or 8-bit input code, ordered MSB-to-LSB, followed by 4, 6 or 8 don't-care bits (LTC2632-12, LTC2632-10 and LTC2632-8 respectively; see Figure 2). Data can only be transferred to the device when the $\overline{CS}$/LD signal is low, beginning on the first rising edge of SCK. SCK may be high or low at the falling edge of $\overline{CS}$/LD. The rising edge of $\overline{CS}$/LD ends the data transfer and causes the device to execute the command specified in the 24-bit input sequence. The complete sequence is shown in Figure 3a.

The command (C3-C0) and address (A3-A0) assignments are shown in Tables 1 and 2. The first four commands in Table 1 consist of write and update operation. A Write operation loads a 16-bit data word from the 24-bit shift register into the input register of the selected DAC, *n*. An Update operation copies the data word from the input register to the DAC register. Once copied into the DAC register, the data word becomes the active 12-, 10-, or 8-bit input code, and is converted to an analog voltage at the DAC output. Write to and Update combines the first two commands. The Update operation also powers up the DAC if it had been in power-down mode. The data path and registers are shown in the Block Diagram.

While the minimum input sequence is 24 bits, it may optionally be extended to 32 bits to accommodate microprocessors that have a minimum word width of 16 bits (2 bytes). To use the 32-bit width, 8 don't-care bits are transferred to the device first, followed by the 24-bit sequence described. Figure 3b shows the 32-bit sequence.

The 16-bit data word is ignored for all commands that do not include a Write operation.

OPERATION

Reference Modes

For applications where an accurate external reference is not available, nor desirable due to limited space, the LTC2632 has a user-selectable, integrated reference. The integrated reference voltage is internally amplified by 2x to provide the full-scale DAC output voltage range. The LTC2632-LMI/LTC2632-LMX/LTC2632-LZ provides a full-scale output of 2.5V. The LTC2632-HMI/LTC2632-HZ provides a full-scale output of 4.096V. The internal reference can be useful in applications where the supply voltage is poorly regulated. Internal reference mode can be selected by using command 0110b, and is the power-on default for LTC2632-HZ/LTC2632-LZ, as well as for LTC2632-HMI/LTC2632-LMI.

The 10ppm/°C, 1.25V (LTC2632-LMI/LTC2632-LMX/LTC2632-LZ) or 2.048V (LTC2632-HMI/LTC2632-HZ) internal reference is available at the REF pin. Adding bypass capacitance to the REF pin will improve noise performance; 0.1µF is recommended, and up to 10µF can be driven without oscillation. This output must be buffered when driving an external DC load current.

Alternatively, the DAC can operate in external reference mode using command 0111b. In this mode, an input voltage supplied externally to the REF pin provides the reference ($1V \le V_{REF} \le V_{CC}$) and the supply current is reduced. The external reference voltage supplied sets the full-scale DAC output voltage. External reference mode is the power-on default for the LTC2632-LMX.

The reference mode of LTC2632-HZ/LTC2632-LZ/LTC2632-HMI/LTC2632-LMI (internal reference power-on default), can be changed by software command after power-up. The same is true for the LTC2632-LMX (external reference power-on default).

Power-Down Mode

For power-constrained applications, power-down mode can be used to reduce the supply current whenever less than two DAC outputs are needed. When in power-down, the buffer amplifiers, bias circuits, and integrated reference circuits are disabled, and draw essentially zero current. The DAC outputs are put into a high-impedance state, and the output pins are passively pulled to ground through individual 200k resistors. Input and DAC-register contents are not disturbed during power-down.

Either channel or both channels can be put into power-down mode by using command 0100b in combination with the appropriate DAC address (*n*). The supply current is reduced approximately 30% for each DAC powered down. The integrated reference is automatically powered down when external reference is selected using command 0111b. In addition, all the DAC channels and the integrated reference together can be put into power-down mode using power-down chip command 0101b. When the integrated reference is in power-down mode, the REF pin becomes high impedance (typically > 1GΩ). For all power-down commands the 16-bit data word is ignored.

Normal operation resumes after executing any command that includes a DAC update (as shown in Table 1). The selected DAC is powered up as its voltage output is updated. When a DAC which is in a powered-down state is powered up and updated, normal settling is delayed. If less than two DACs are in a powered-down state prior to the update command, the power-up delay time is 10µs. However, if both DACs and the integrated reference are powered down, then the main bias generation circuit block has been automatically shut down in addition to the DAC amplifiers and reference buffers. In this case, the power up delay time is 12µs. The power-up of the integrated reference depends on the command that powered it down. If the reference is powered down using the select external reference command (0111b), then it can only be powered back up using select internal reference command (0110b). However, if the reference was powered down using power-down chip command (0101b), then in addition to the select internal reference command (0110b), any command that powers up the DACs will also power-up the integrated reference.

OPERATION

Voltage Output

The LTC2632's integrated rail-to-rail amplifier has guaranteed load regulation when sourcing or sinking up to 10mA at 5V, and 5mA at 3V.

Load regulation is a measure of the amplifier's ability to maintain the rated voltage accuracy over a wide range of load current. The measured change in output voltage per change in forced load current is expressed in LSB/mA.

DC output impedance is equivalent to load regulation, and may be derived from it by simply calculating a change in units from LSB/mA to ohms. The amplifier's DC output impedance is 0.1Ω when driving a load well away from the rails.

When drawing a load current from either rail, the output voltage headroom with respect to that rail is limited by the 50Ω typical channel resistance of the output devices (e.g., when sinking 1mA, the minimum output voltage is 50Ω • 1mA, or 50mV). See the graph *Headroom at Rails vs Output Current* in the Typical Performance Characteristics section.

The amplifier is stable driving capacitive loads of up to 500pF.

Rail-to-Rail Output Considerations

In any rail-to-rail voltage output device, the output is limited to voltages within the supply range.

Since the analog output of the DAC cannot go below ground, it may limit for the lowest codes as shown in Figure 4b. Similarly, limiting can occur near full-scale when the REF pin is tied to V_{CC}. If $V_{REF} = V_{CC}$ and the DAC full-scale error (FSE) is positive, the output for the highest codes limits at V_{CC}, as shown in Figure 4c. No full-scale limiting can occur if V_{REF} is less than $V_{CC} – FSE$.

Offset and linearity are defined and tested over the region of the DAC transfer function where no output limiting can occur.

Board Layout

The PC board should have separate areas for the analog and digital sections of the circuit. A single, solid ground plane should be used, with analog and digital signals carefully routed over separate areas of the plane. This keeps digital signals away from sensitive analog signals and minimizes the interaction between digital ground currents and the analog section of the ground plane. The resistance from the LTC2632 GND pin to the ground plane should be as low as possible. Resistance here will add directly to the effective DC output impedance of the device (typically 0.1Ω). Note that the LTC2632 is no more susceptible to this effect than any other parts of this type; on the contrary, it allows layout-based performance improvements to shine rather than limiting attainable performance with excessive internal resistance.

Another technique for minimizing errors is to use a separate power ground return trace on another board layer. The trace should run between the point where the power supply is connected to the board and the DAC ground pin. Thus the DAC ground pin becomes the common point for analog ground, digital ground, and power ground. When the LTC2632 is sinking large currents, this current flows out the ground pin and directly to the power ground trace without affecting the analog ground plane voltage.

It is sometimes necessary to interrupt the ground plane to confine digital ground currents to the digital portion of the plane. When doing this, make the gap in the plane only as long as it needs to be to serve its purpose and ensure that no traces cross over the gap.

Bypass capacitors should be placed as close to the pins as possible with a low impedance path to GND.

OPERATION

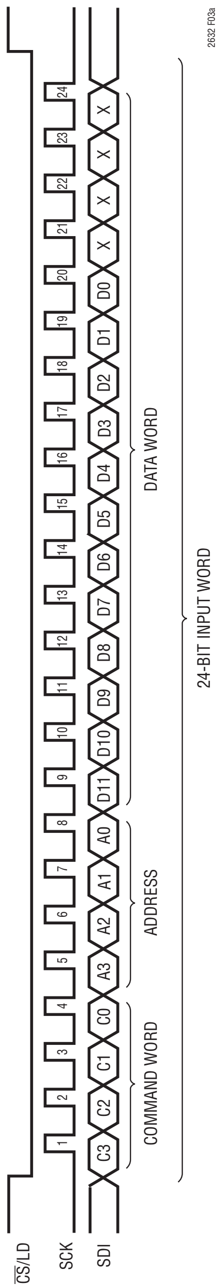


**Figure 3a. LTC2632-12 24-Bit Load Sequence (Minimum Input Word)
LTC2632-10 SDI Data Word: 10-Bit Input Code + 6 Don't-Care Bits;
LTC2632-8 SDI Data Word: 8-Bit Input Code + 8 Don't-Care Bits**

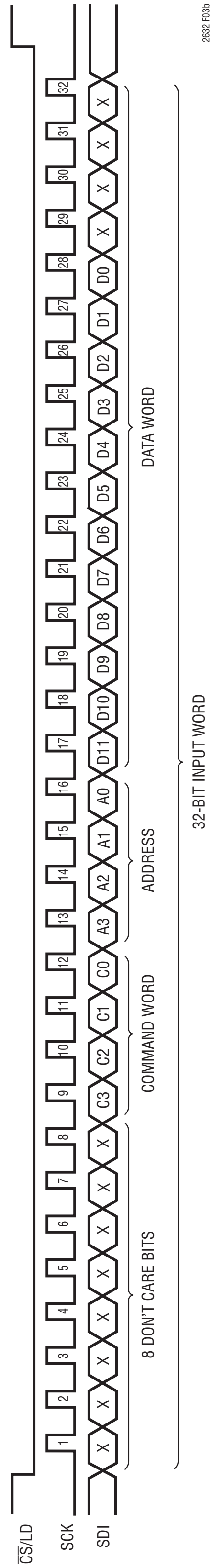


**Figure 3b. LTC2632-12 32-Bit Load Sequence
LTC2632-10 SDI Data Word: 10-Bit Input Code + 6 Don't-Care Bits;
LTC2632-8 SDI Data Word: 8-Bit Input Code + 8 Don't-Care Bits**

OPERATION

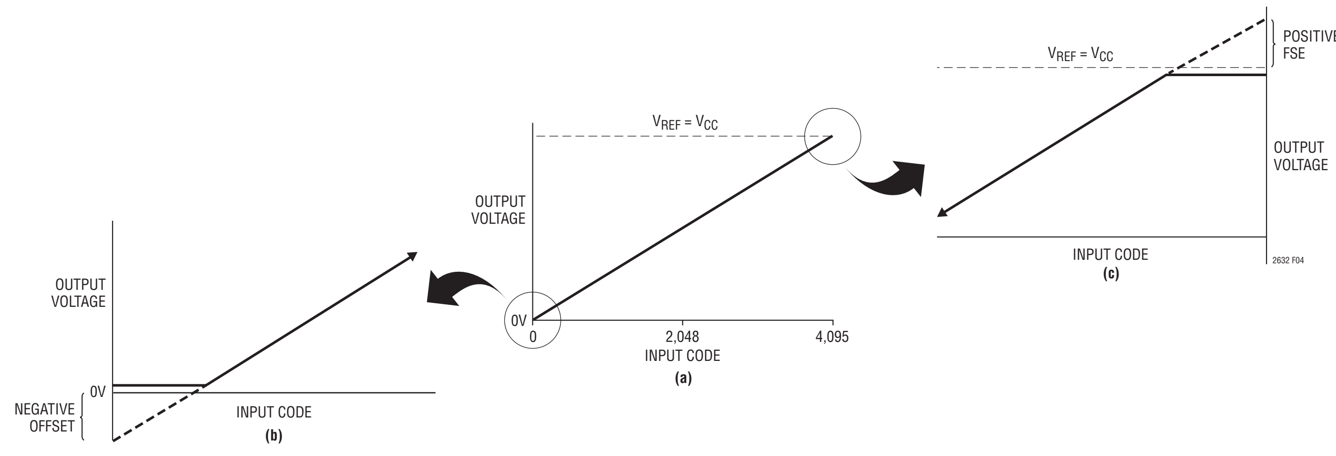
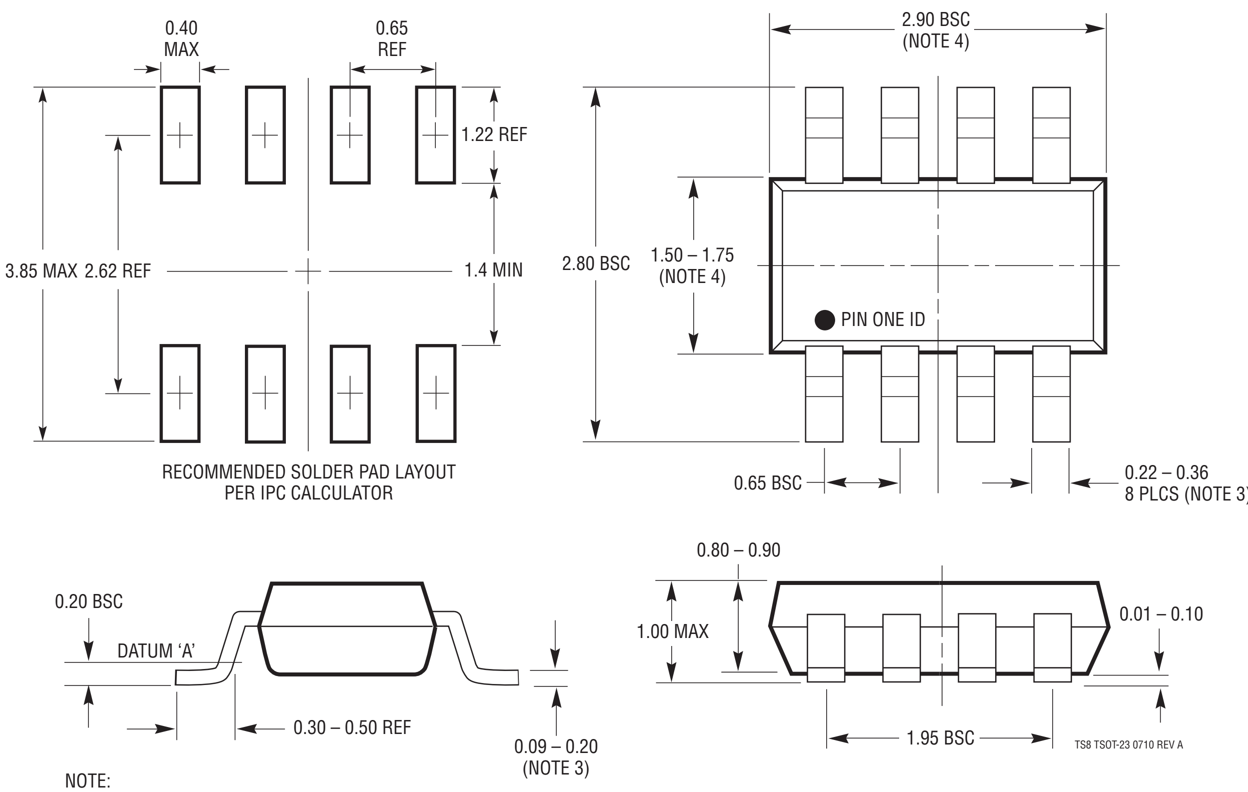


Figure 4. Effects of Rail-to-Rail Operation On a DAC Transfer Curve (Shown for 12 Bits)
(a) Overall Transfer Function
(b) Effect of Negative Offset for Codes Near Zero
(c) Effect of Positive Full-Scale Error for Codes Near Full-Scale

PACKAGE DESCRIPTION

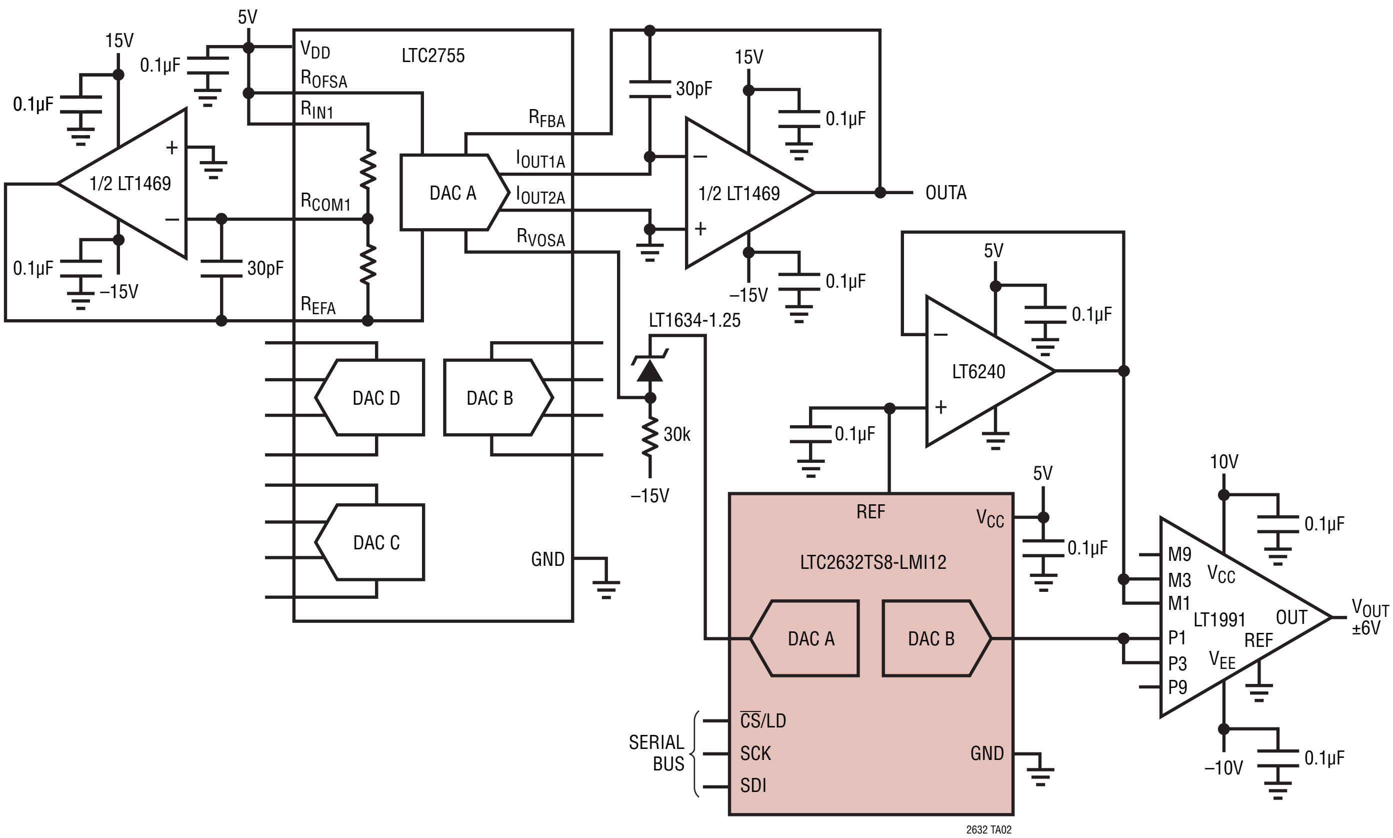
TS8 Package
8-Lead Plastic TSOT-23
(Reference LTC DWG # 05-08-1637 Rev A)



NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOLD FLASH SHALL NOT EXCEED 0.254mm
6. JEDEC PACKAGE REFERENCE IS MO-193

TYPICAL APPLICATION

LTC2632 DACs Adjust LTC2755-16 Offset, Amplified with LT1991 PGA to ±5V



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1662	Dual 10-Bit Ultralow Power V_{OUT} DAC in 8-Lead MSOP with External Reference	1.5µA per DAC, 2.7V to 5.5V Supply Range, Rail-to-Rail Output, SPI Serial Interface
LTC2602/LTC2612/ LTC2622	Dual 16-/14-/12-Bit V_{OUT} DACs in 8-Lead MSOP with External Reference	300µA per DAC, 2.5V to 5.5V Supply Range, Rail-to-Rail Output, SPI Serial Interface
LTC2607/LTC2617/ LTC2627	Dual 16-/14-/12-Bit V_{OUT} DACs in 12-Lead DFN with External Reference	260µA per DAC, 2.7V to 5.5V Supply Range, Rail-to-Rail Output, I^2C Serial Interface
LTC2630	Single 12-/10-/8-Bit V_{OUT} DACs with 10ppm/°C Reference in SC70	180µA per DAC, 2.7V to 5.5V Supply Range, 10ppm/°C Reference, Rail-to-Rail Output, SPI Serial Interface
LTC2631	Single 12-/10-/8-Bit I2C V_{OUT} DACs with 10ppm/°C Reference in ThinSOT	180µA per DAC, 2.7V to 5.5V Supply Range, 10ppm/°C Reference, External REF Mode, Rail-to-Rail Output, I^2C Interface
LTC2634	Quad 12-/10-/8-Bit V_{OUT} DACs with 10ppm/°C Reference	125µA per DAC, 2.7V to 5.5V Supply Range, 10ppm/°C Reference, External REF Mode, Rail-to-Rail Output, SPI Interface
LTC2636	Octal 12-/10-/8-Bit V_{OUT} DACs with 10ppm/°C Reference	125µA per DAC, 2.7V to 5.5V Supply Range, 10ppm/°C Reference, External REF Mode, Rail-to-Rail Output, SPI Interface
LTC2640	Single 12-/10-/8-Bit V_{OUT} DACs with 10ppm/°C Reference in ThinSOT	180µA per DAC, 2.7V to 5.5V Supply Range, 10ppm/°C Reference, External REF Mode, Rail-to-Rail Output, SPI Interface
LTC2654	Quad 16-/12-Bit V_{OUT} DACs with ±4 LSB INL, ±1 LSB DNL	4mm × 4mm QFN-20, SSOP-16 Packages, SPI Interface, Internal 10ppm/°C (Max) Reference

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