USB Compatible Switching Power Manager/LiFePO$_4$ Charger with Overvoltage Protection

FEATURES

- **Switching Regulator with Bat-Track™ Adaptive Output Control Makes Optimal Use of Limited Power Available from USB Port to Charge Battery and Power Application**
- **Charge Control Algorithm Specifically Designed for LiFePO$_4$ (Lithium Iron Phosphate)**
- **Overvoltage Protection Guards Against Damage**
- **Bat-Track External Step-Down Switching Regulator Control Maximizes Efficiency from Automotive, Firewire and Other High Voltage Input Sources**
- 180mΩ Internal Ideal Diode Plus External Ideal Diode Controller Seamlessly Provide Low Loss PowerPath™ When Input Power Is Limited or Unavailable
- Preset 3.6V Charge Voltage with 0.5% Accuracy
- Instant-On Operation with Discharged Battery
- 700mA Maximum Load Current from USB Port
- 2A Maximum Input Current from Internal Switching Regulator
- 1.5A Maximum Charge Current with Thermal Limiting
- 20-Lead 3mm × 4mm × 0.75mm QFN Package

APPLICATIONS

- High Peak Power Battery-Powered Equipment
- Backup Applications
- High Reliability Handhelds

DESCRIPTION

The LTC®4098-3.6 is a high efficiency USB PowerPath controller and full-featured LiFePO$_4$ battery charger. It seamlessly manages power distribution from multiple sources including USB, wall adapter, automotive, Firewire or other high voltage DC/DC converters, and a LiFePO$_4$ battery.

The LTC4098-3.6 charge algorithm is optimized for LiFePO$_4$ by implementing a 1-hour float voltage termination timer and a 0°C to 60°C NTC-based charge qualification range. Furthermore, completely discharged batteries are charged at the full programmed charge current.

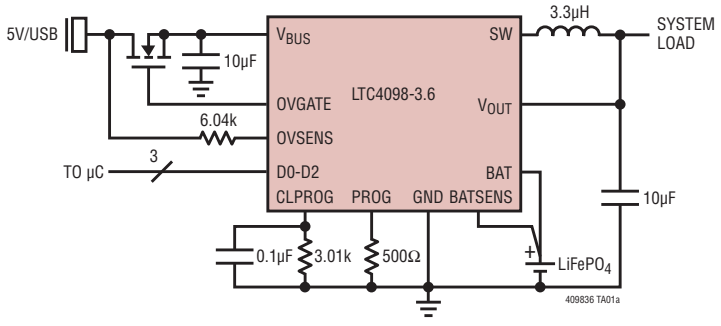
The LTC4098-3.6's switching regulator can automatically limit its input current for USB compatibility. For automotive and other high voltage applications, the LTC4098-3.6 interfaces with an external switching regulator. Both the USB input and the auxiliary input controller feature Bat-Track optimized charging to provide maximum power to the application and reduced heat in high power density applications with input supplies from 5V to as high as 38V.

An overvoltage protection circuit guards the LTC4098-3.6 from high voltage damage on the VBUS pin with just two external components.

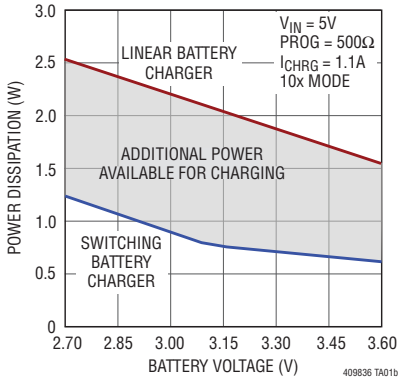
The LTC4098-3.6 is available in a 20-lead 3mm × 4mm × 0.75mm QFN surface mount package.

TYPICAL APPLICATION

High Efficiency USB Compatible LiFePO$_4$ Battery Charger with Overvoltage Protection



Reduced Power Dissipation vs Linear Battery Charger

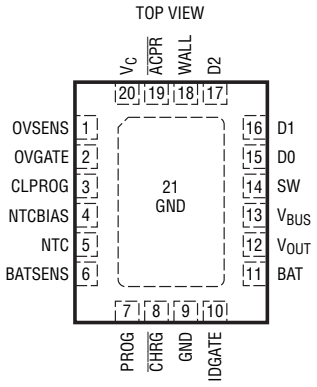


ABSOLUTE MAXIMUM RATINGS

(Notes 1, 3)

V_{BUS}, WALL (Transient) t < 1ms, Duty Cycle < 1% ..... –0.3V to 7V
V_{BUS}, WALL (Static), BAT, BATSENS, $\overline{CHRG}$, NTC, ... –0.3V to 6V
D0, D1, D2 .....–0.3V to Max (V_{BUS}, V_{OUT}, BAT) + 0.3V
I_{OVSENS}.....±10mA
I_{CLPROG} 3mA
I_{PROG}.....2mA
$I_{\overline{CHRG}}$.....50mA
I_{VOUT}, I_{SW}, I_{BAT}.....2.25A
$I_{\overline{ACPR}}$ .....±5mA
Operating Temperature Range.....–40°C to 85°C
Junction Temperature .....125°C
Storage Temperature Range.....–65°C to 125°C

PIN CONFIGURATION



UDC PACKAGE
20-LEAD (3mm × 4mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 21) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4098EUDC-3.6#PBF	LTC4098EUDC-3.6#TRPBF	LFYR	20-Lead (3mm × 4mm) Plastic QFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{BUS} = 5V, BAT = 3.3V, R_{CLPROG} = 3.01k, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Power Supply							
V_{BUS}	Input Supply Voltage		●	4.35		5.5	V
$I_{VBUS(LIM)}$	Total Input Current	1x Mode	●	92	96	100	mA
		5x Mode	●	445	473	500	mA
		10x Mode	●	815	883	1000	mA
		Low Power Suspend Mode	●	0.32	0.39	0.5	mA
		High Power Suspend Mode	●	1.6	2.05	2.5	mA
I_{VBUSQ} (Note 4)	Input Quiescent Current	1x Mode			6		mA
		5x Mode			15		mA
		10x Mode			15		mA
		Low Power Suspend Mode			0.042		mA
		High Power Suspend Mode			0.042		mA
h_{CLPROG} (Note 4)	Ratio of Measured V_{BUS} Current to CLPROG Program Current	1x Mode			230		mA/mA
		5x Mode			1164		mA/mA
		10x Mode			2210		mA/mA
		Low Power Suspend Mode			11.6		mA/mA
		High Power Suspend Mode			60		mA/mA

ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{VOUT}	V_{OUT} Current Available Before Discharging Battery	1x Mode 5x Mode 10x Mode Low Power Suspend Mode High Power Suspend Mode			135 659 1231 0.32 2.04		mA mA mA mA mA
V_{CLPROG}	CLPROG Servo Voltage in Current Limit	1x, 5x, 10x Modes Suspend Modes			1.188 100		V mV
V_{UVLO}	V_{BUS} Undervoltage Lockout	Rising Threshold Falling Threshold		 3.95	4.30 4.00	4.35	V V
V_{OUT}	V_{OUT} Voltage	1x, 5x, 10x Modes, 0V < BAT ≤ 3.6V, I_{VOUT} = 0mA, Battery Charger Off		3.1	BAT + 0.4	4.3	V
		USB Suspend Modes, I_{VOUT} = 250µA		3.7	3.8	3.9	V
f_{OSC}	Switching Frequency			1.96	2.25	2.65	MHz
R_{PMOS}	PMOS On-Resistance				0.18		Ω
R_{NMOS}	NMOS On-Resistance				0.30		Ω
I_{PEAK}	Peak Inductor Current Clamp	1x Mode 5x Mode 10x Mode			1.2 1.7 3		A A A
R_{SUSP}	Suspend LDO Output Resistance				15		Ω
Bat-Track External Switching Regulator Control							
V_{WALL}	Absolute WALL Input Threshold	Rising Threshold Falling Threshold		4.1	4.25 3.2	4.4	V V
ΔV_{WALL}	Differential WALL Input Threshold	WALL-BAT Rising Threshold WALL-BAT Falling Threshold		 0	90 25	 50	mV mV
	Regulation Target			3.5	BAT + 0.4		V
	WALL Quiescent Current				100		µA
	$\overline{ACPR}$ High Voltage	$I_{\overline{ACPR}}$ = 0mA			V_{OUT}		V
	$\overline{ACPR}$ Low Voltage	$I_{\overline{ACPR}}$ = 0mA			0		V
Overvoltage Protection							
V_{OVP}	Overvoltage Protection Threshold	Rising Threshold, R_{OVSENS} = 6.04k		6.10	6.35	6.70	V
V_{OVGATE}	OVGATE Output Voltage	Input Below V_{OVP} Input Above V_{OVP}			1.88 • $V_{OVSENSE}$ 0	12	V V
t_{RISE}	OVGATE Time to Reach Regulation	C_{OVGATE} = 1nF			2.2		ms
Battery Charger							
V_{FLOAT}	BAT Regulated Output Voltage	 0°C ≤ T_A ≤ 85°C		3.582 3.565	3.6 3.6	3.618 3.635	V V
I_{CHG}	Constant-Current Mode Charge Current	R_{PROG} = 1k, 10x Mode R_{PROG} = 5k, 5x, 10x Modes		980 192	1030 206	1080 220	mA mA
I_{BAT}	Battery Drain Current	V_{BUS} > V_{UVLO}, PowerPath Switching Regulator On, Battery Charger Off, I_{VOUT} = 0µA			3.7	5	µA
		V_{BUS} = 0V, I_{VOUT} = 0µA (Ideal Diode Mode)			25	35	µA
V_{PROG}	PROG Pin Servo Voltage				1.000		V
h_{PROG}	Ratio of I_{BAT} to PROG Pin Current				1030		mA/mA
V_{RECHRG}	Recharge Battery Threshold Voltage	Threshold Voltage Relative to V_{FLOAT}		–80	–100	–120	mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{BUS} = 5V, BAT = 3.3V, R_{CLPROG} = 3.01k, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{TERM}	Safety Timer Termination Period	Timer Starts When BAT = V_{FLOAT}		0.85	1	1.15	Hour
t_{BADBAT}	Bad Battery Termination Time	BAT < V_{TRKL}		0.43	0.5	0.58	Hour
$h_{C/10}$	End of Charge Indication Current Ratio	(Note 5)		0.09	0.1	0.11	mA/mA
$V_{\overline{CHRG}}$	$\overline{CHRG}$ Pin Output Low Voltage	$I_{\overline{CHRG}}$ = 5mA			65	100	mV
$I_{\overline{CHRG}}$	$\overline{CHRG}$ Pin Input Current	BAT = 4.5V, $V_{\overline{CHRG}}$ = 5V			0	1	µA
R_{ON_CHG}	Battery Charger Power FET On-Resistance (Between V_{OUT} and BAT)	I_{BAT} = 200mA			0.18		Ω
T_{LIM}	Junction Temperature in Constant-Temperature Mode				110		°C
NTC							
V_{COLD}	Cold Temperature Fault Threshold Voltage Hysteresis	Rising Threshold		75.0	76.5 2.9	78.0	%NTCBIAS %NTCBIAS
V_{HOT}	Hot Temperature Fault Threshold Voltage Hysteresis	Falling Threshold		18.4	19.9 1.9	21.4	%NTCBIAS %NTCBIAS
V_{DIS}	NTC Disable Threshold Voltage Hysteresis	Falling Threshold		0.5	1.3 50	2.3	%NTCBIAS mV
I_{NTC}	NTC Leakage Current	NTC = 5V		–50		50	nA
Ideal Diode							
V_{FWD}	Forward Voltage Detection	I_{VOUT} = 10mA			15		mV
$R_{DROPOUT}$	Internal Diode On-Resistance, Dropout	I_{VOUT} = 200mA			0.18		Ω
I_{MAX}	Diode Current Limit			2			A
Logic (D0, D1, D2)							
V_{IL}	Input Low Voltage					0.4	V
V_{IH}	Input High Voltage			1.2			V
I_{PD}	Static Pull-Down Current	V_{PIN} = 1V			2		µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC4098E-3.6 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC4098E-3.6 is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

Note 3: The LTC4098E-3.6 includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

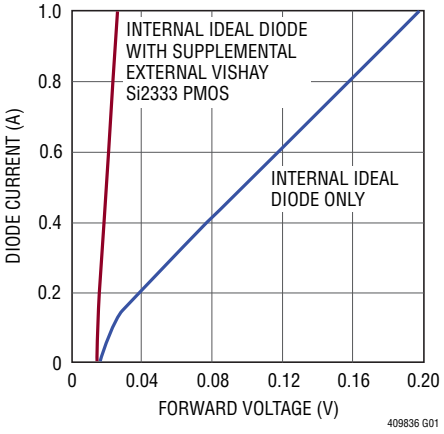
Note 4: Total input current is:

$I_{VBUSQ} + (V_{CLPROG}/R_{CLPROG}) \bullet (h_{CLPROG} + 1)$

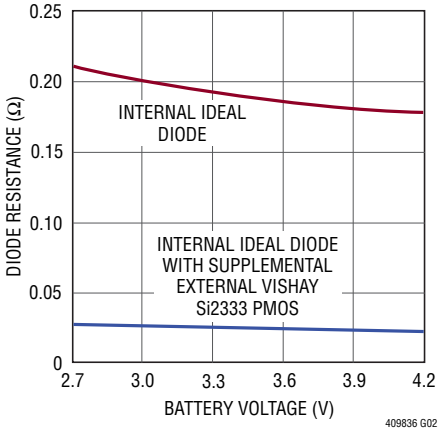
Note 5: $h_{C/10}$ is expressed as a fraction of measured full charge current with a 5k PROG resistor.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

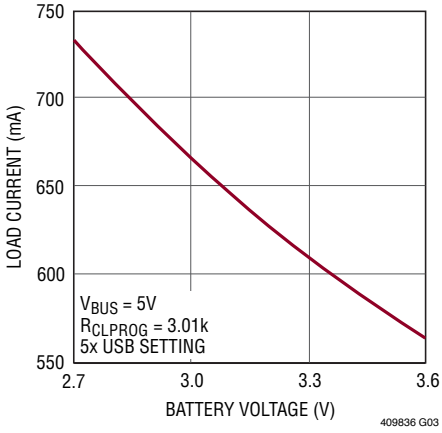
Ideal Diode V-I Characteristics



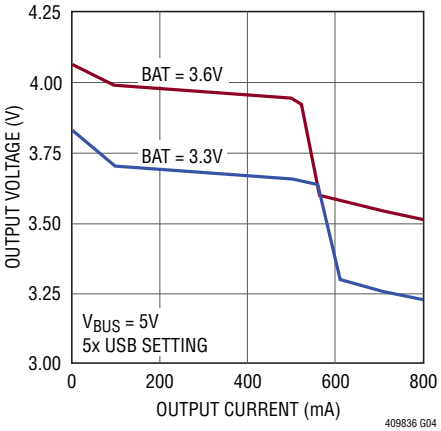
Ideal Diode Resistance vs Battery Voltage



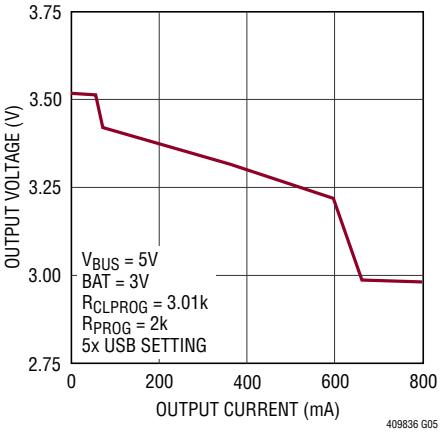
USB Compliant Load Current Available Before Discharging Battery



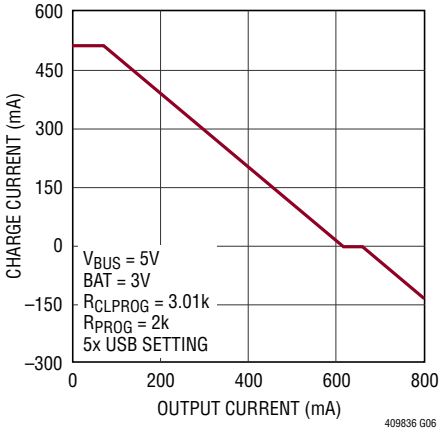
V_{OUT} Voltage vs V_{OUT} Current (Battery Charger Disabled)



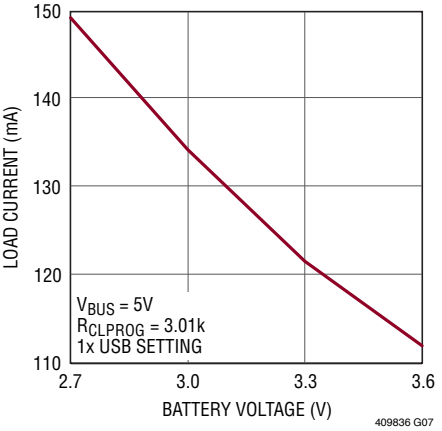
V_{OUT} Voltage vs V_{OUT} Current (Battery Charger Enabled)



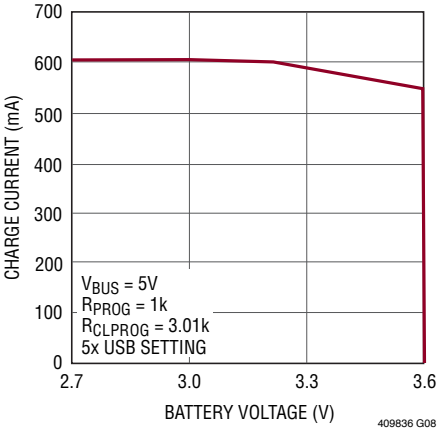
Battery Charge Current vs V_{OUT} Current (Battery Charger Enabled)



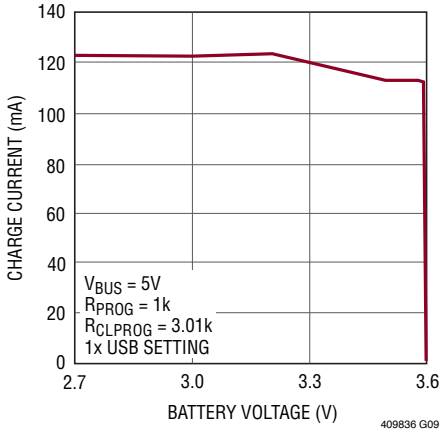
USB Compliant Load Current Available Before Discharging Battery



USB Limited Battery Charge Current vs Battery Voltage

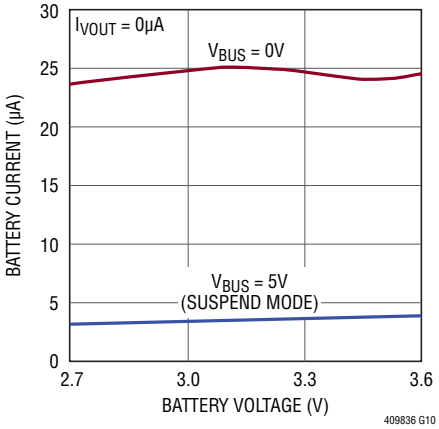


USB Limited Battery Charge Current vs Battery Voltage

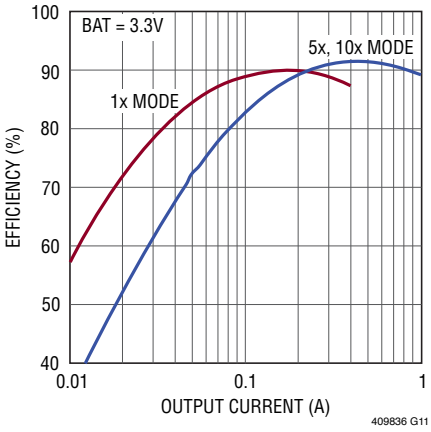


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

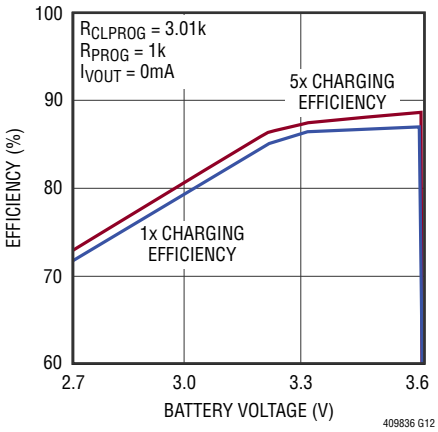
Battery Drain Current vs Battery Voltage



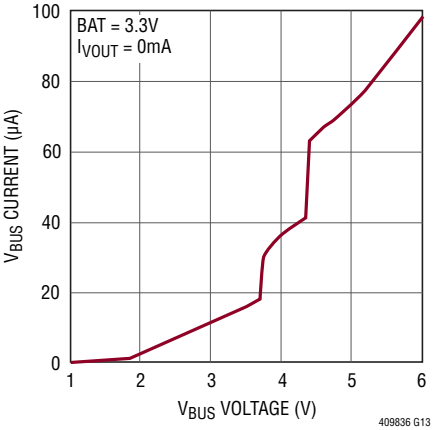
PowerPath Switching Regulator Efficiency vs Output Current



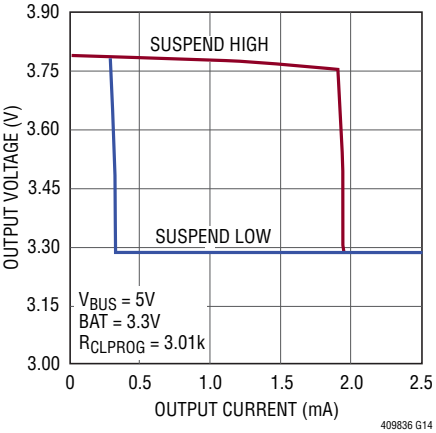
Battery Charging Efficiency vs Battery Voltage with No External Load (P_{BAT}/P_{VBUS})



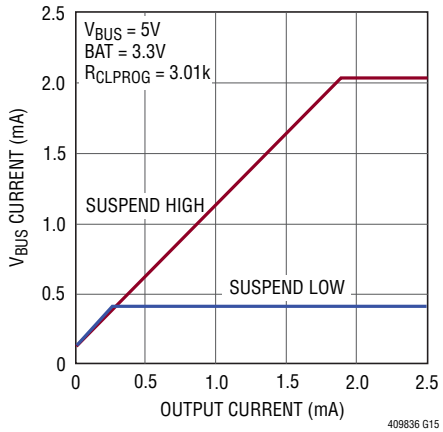
V_{BUS} Current vs V_{BUS} Voltage (Suspend Mode—Includes OVP)



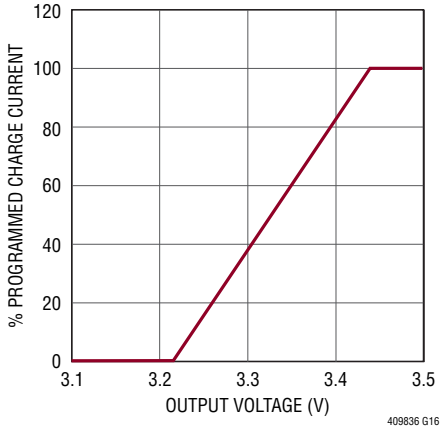
V_{OUT} Voltage vs V_{OUT} Current in Suspend



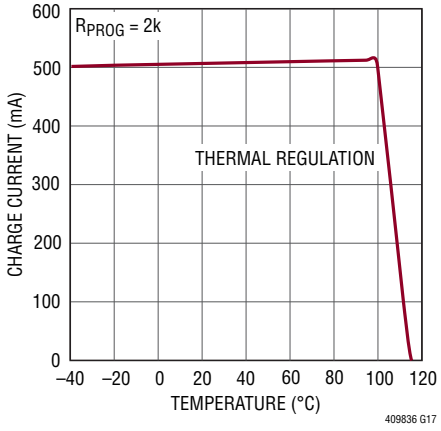
V_{BUS} Current vs V_{OUT} Current in Suspend (Includes OVP)



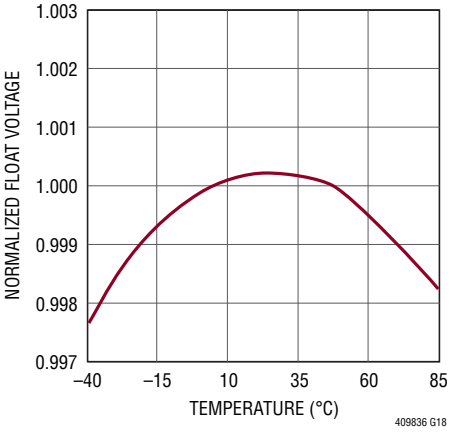
Automatic Battery Charge Current vs Output Voltage



Battery Charge Current vs Temperature

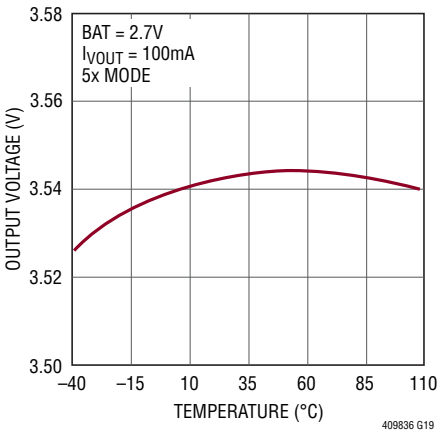


Normalized Battery Charger Float Voltage vs Temperature

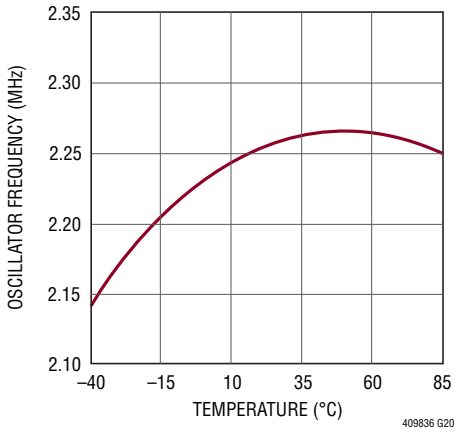


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

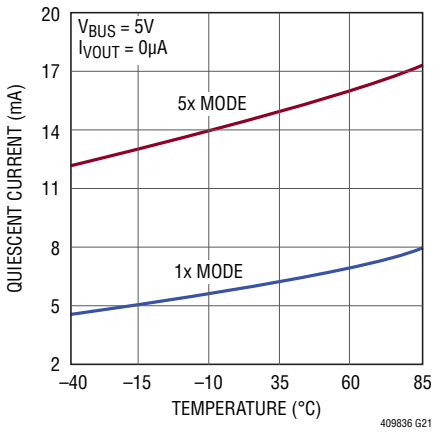
Low Battery (Instant-On, Charger Disabled) Output Voltage vs Temperature



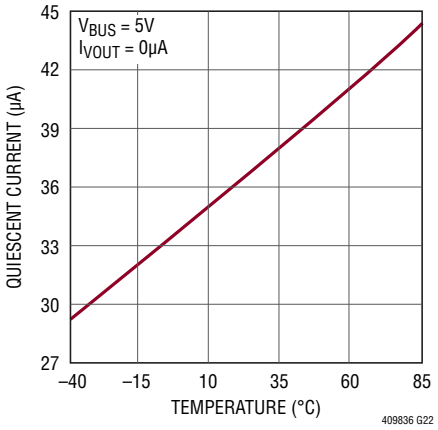
Oscillator Frequency vs Temperature



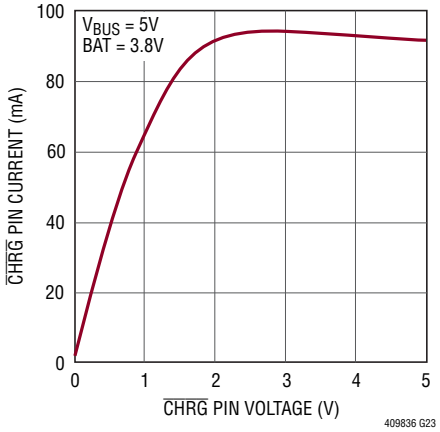
V_{BUS} Quiescent Current vs Temperature



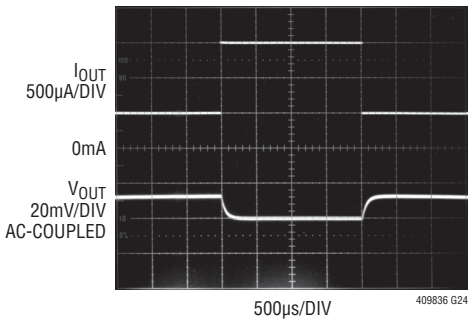
Quiescent Current in Suspend vs Temperature



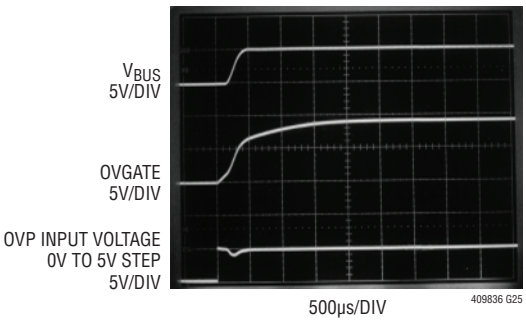
$\overline{CHRG}$ Pin Current vs Voltage (Pull-Down State)



Suspend LDO Transient Response (500µA to 1.5mA)

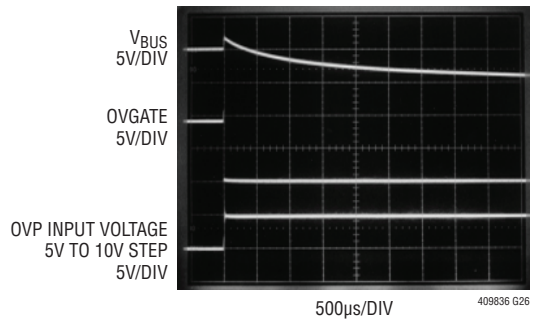


OVP Connection Waveform

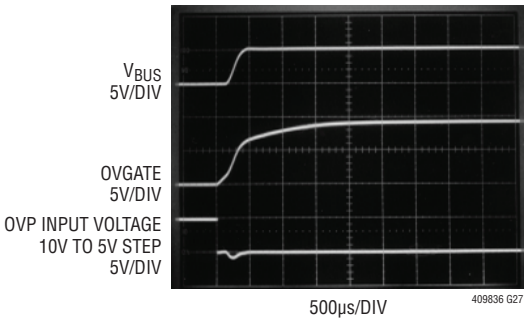


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

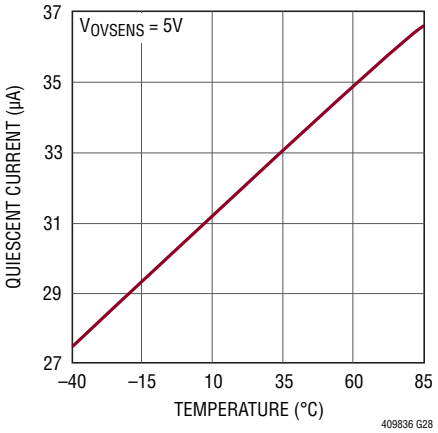
OVP Protection Waveform



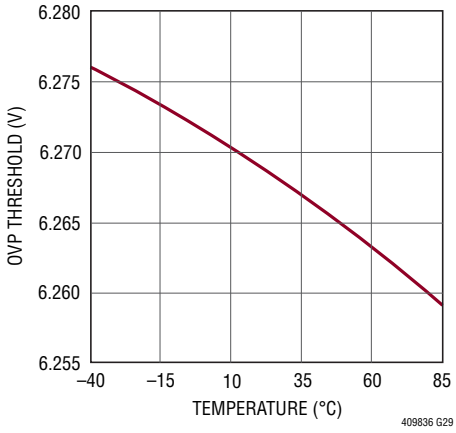
OVP Reconnection Waveform



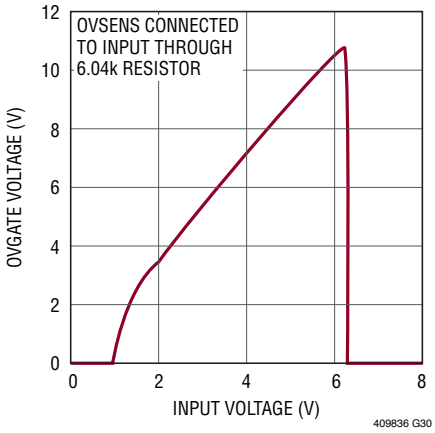
OVSENS Quiescent Current vs Temperature



Rising Overvoltage Threshold vs Temperature



OVGATE vs OVSENS



PIN FUNCTIONS

OVSENS (Pin 1): Overvoltage Protection Sense Input. OVSENS should be connected through a 6.04k resistor to the input power connector and the drain of an external N-channel MOSFET pass transistor. When the voltage on this pin exceeds a preset level, the OVGATE pin will be pulled to GND to disable the pass transistor and protect downstream circuitry. If overvoltage protection is not desired, connect OVSENS to GND.

OVGATE (Pin 2): Overvoltage Protection Gate Output. Connect OVGATE to the gate pin of an external N-channel MOSFET pass transistor. The source of the transistor should be connected to V_{BUS} and the drain should be connected to the product's DC input connector. This pin is connected to an internal charge pump capable of creating sufficient overdrive to fully enhance the pass transistor. If an overvoltage condition is detected, OVGATE is brought rapidly to GND to prevent damage to downstream circuitry. OVGATE works in conjunction with OVSENS to provide this protection. If overvoltage protection is not desired, leave OVGATE open.

CLPROG (Pin 3): USB Current Limit Program and Monitor Pin. A 1% resistor from CLPROG to ground determines the upper limit of the current drawn from the V_{BUS} pin. A precise fraction of the input current, h_{CLPROG}, is sent to the CLPROG pin when the high side switch is on. The switching regulator delivers power until the CLPROG pin reaches 1.188V. Therefore, the current drawn from V_{BUS} will be limited to an amount given by h_{CLPROG} and R_{CLPROG}. There are several ratios for h_{CLPROG} available, two of which correspond to the 500mA and 100mA USB specifications. A multilayer ceramic averaging capacitor is also required at CLPROG for filtering.

NTCBIAS (Pin 4): NTC Thermistor Bias Output. If NTC operation is desired, connect a bias resistor between NTCBIAS and NTC, and an NTC thermistor between NTC and GND. To disable NTC operation, connect NTC to GND and leave NTCBIAS open.

NTC (Pin 5): Input to the NTC Thermistor Monitoring Circuits. The NTC pin connects to a negative temperature coefficient thermistor which is typically co-packaged with the battery pack to determine if the battery is too hot or too cold to charge. If the battery's temperature is out of range, charging is paused until the battery temperature re-enters the valid range. A low drift bias resistor is required from NTCBIAS to NTC and a thermistor is required from NTC to ground. If the NTC function is not desired, the NTC pin should be grounded.

BATSENS (Pin 6): Battery Voltage Sense Input. For proper operation, this pin must always be connected to BAT. For best performance, connect BATSENS to BAT physically close to the $LiFePO_4$ cell.

PROG (Pin 7): Charge Current Program and Charge Current Monitor Pin. Connecting a 1% resistor from PROG to ground programs the charge current. If sufficient input power is available in constant-current mode, this pin servos to 1V. The voltage on this pin always represents the actual charge current by using the following formula:

$$I_{BAT} = \frac{V_{PROG}}{R_{PROG}} \bullet 1030$$

$\overline{CHRG}$ (Pin 8): Open-Drain Charge Status Output. The $\overline{CHRG}$ pin indicates the status of the battery charger. Four possible states are represented by $\overline{CHRG}$: charging, not charging, unresponsive battery and battery temperature out of range. $\overline{CHRG}$ is modulated at 35kHz and switches between a low and a high duty cycle for easy recognition by either humans or microprocessors. $\overline{CHRG}$ requires a pull-up resistor and/or LED to provide indication.

GND (Pin 9, Exposed Pad Pin 21): The exposed pad and pin must be soldered to the PCB to provide a low electrical and thermal impedance connection to ground.

IDGATE (Pin 10): Ideal Diode Amplifier Output. This pin controls the gate of an external P-channel MOSFET transistor used to supplement the internal ideal diode. The source of the P-channel MOSFET should be connected to V_{OUT} and the drain should be connected to BAT.

BAT (Pin 11): Single-Cell $LiFePO_4$ Battery Pin. Depending on available power and load, a $LiFePO_4$ battery on BAT will either deliver system power to V_{OUT} through the ideal diode or be charged from the battery charger. The LTC4098-3.6 will charge to a float voltage of 3.600V.

V_{OUT} (Pin 12): Output Voltage of the Switching PowerPath Controller and Input Voltage of the Battery Charger. The

PIN FUNCTIONS

majority of the portable product should be powered from V_{OUT}. The LTC4098-3.6 will partition the available power between the external load on V_{OUT} and the internal battery charger. Priority is given to the external load and any extra power is used to charge the battery. An ideal diode from BAT to V_{OUT} ensures that V_{OUT} is powered even if the load exceeds the allotted power from V_{BUS} or if the V_{BUS} power source is removed. V_{OUT} should be bypassed with a low impedance multilayer ceramic capacitor.

V_{BUS} (Pin 13): Input Voltage for the Switching PowerPath Controller. V_{BUS} will usually be connected to the USB port of a computer or a DC output wall adapter. V_{BUS} should be bypassed with a low impedance multilayer ceramic capacitor.

SW (Pin 14): The SW pin delivers power from V_{BUS} to V_{OUT} via the step-down switching regulator. An inductor should be connected from SW to V_{OUT}. See the Applications Information section for a discussion of inductance value and current rating.

D0 (Pin 15): Mode Select Input Pin. D0, in combination with the D1 pin and the D2 pin, controls the current limit and battery charger functions of the LTC4098-3.6 (see Table 1). This pin is pulled low by a weak current sink.

D1 (Pin 16): Mode Select Input Pin. D1, in combination with the D0 pin and the D2 pin, controls the current limit and battery charger functions of the LTC4098-3.6 (see Table 1). This pin is pulled low by a weak current sink.

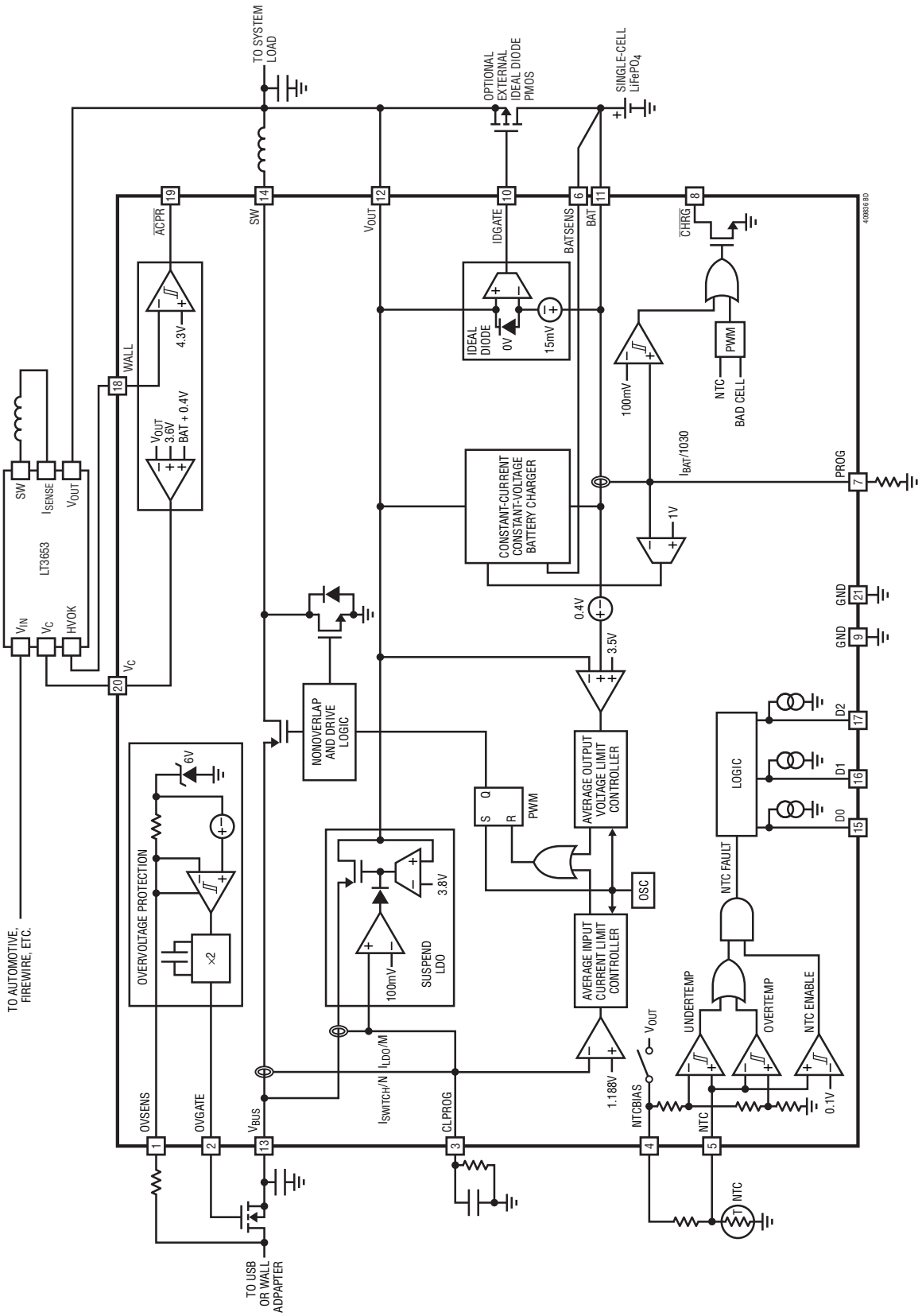
D2 (Pin 17): Mode Select Input Pin. D2, in combination with the D0 pin and D1 pin, controls the current limit and battery charger functions of the LTC4098-3.6 (see Table 1). This pin is pulled low by a weak current sink.

WALL (Pin 18): External Power Source Sense Input. WALL should be connected to the output of the external high voltage switching regulator and to the drain of an external P-channel MOSFET transistor. It is used to determine when power is applied to the external regulator. When power is detected, $\overline{ACPR}$ is driven low and the USB input is automatically disabled.

$\overline{ACPR}$ (Pin 19): External Power Source Present Output (Active Low). $\overline{ACPR}$ indicates that the output of the external high voltage step-down switching regulator is suitable for use by the LTC4098-3.6. It should be connected to the gate of an external P-channel MOSFET transistor whose source is connected to V_{OUT} and whose drain is connected to WALL. $\overline{ACPR}$ has a high level of V_{OUT} and a low level of GND.

V_C (Pin 20): Bat-Track External Switching Regulator Control Output. This pin drives the V_C pin of a Linear Technology external step-down switching regulator. In concert with WALL and $\overline{ACPR}$, it will regulate V_{OUT} to maximize battery charger efficiency.

BLOCK DIAGRAM



OPERATION

Introduction

The LTC4098-3.6 is a high efficiency power management and $LiFePO_4$ charger solution designed to make optimal use of the power available from a variety of sources, while minimizing power dissipation and easing thermal budgeting constraints. The innovative PowerPath architecture ensures that the application is powered immediately after external voltage is applied, even with a completely dead battery, by prioritizing power to the application over the battery.

The LTC4098-3.6 includes a Bat-Track monolithic step-down switching regulator for USB, wall adapters and other 5V sources. Designed specifically for USB applications, the switching regulator incorporates a precision average input current limit for USB compatibility. Because power is conserved, the LTC4098-3.6 allows the load current on V_{OUT} to exceed the current drawn by the USB port, making maximum use of the allowable USB power for battery charging.

The switching regulator and battery charger communicate to ensure that the average input current never exceeds the USB specifications.

For automotive, Firewire, and other high voltage applications, the LTC4098-3.6 provides Bat-Track control of an external LTC step-down switching regulator to maximize battery charger efficiency and minimize heat production.

When power is available from both the USB and high voltage inputs, the high voltage input is prioritized and the USB input is automatically disabled.

The LTC4098-3.6 features an overvoltage protection circuit which is designed to work with an external N-channel MOSFET to prevent damage to its inputs caused by accidental application of high voltage.

The LTC4098-3.6 contains both an internal 180mΩ ideal diode and an ideal diode controller designed for use with an external P-channel MOSFET. The ideal diodes from BAT to V_{OUT} guarantee that ample power is always available to V_{OUT} even if there is insufficient or absent power at V_{BUS} or WALL.

Finally, to prevent battery drain when a device is connected to a suspended USB port, an LDO from V_{BUS} to V_{OUT} provides either low power or high power USB suspend current to the application.

Bat-Track Input Current Limited Step Down Switching Regulator

The power delivered from V_{BUS} to V_{OUT} is controlled by a 2.25MHz constant-frequency step-down switching regulator. To meet the USB maximum load specification, the switching regulator contains a measurement and control system that ensures that the average input current remains below the level programmed at CLPROG. V_{OUT} drives the combination of the external load and the battery charger.

If the combined load does not cause the switching power supply to reach the programmed input current limit, V_{OUT} will track approximately 0.4V above the battery voltage. By keeping the voltage across the battery charger at this low level, power lost to the battery charger is minimized. Figure 1 shows the power path components.

If the combined external load plus battery charge current is large enough to cause the switching power supply to reach the programmed input current limit, the battery charger will reduce its charge current by precisely the amount necessary to enable the external load to be satisfied. Even if the battery charge current is programmed to exceed the allowable USB current, the USB specification for average input current will not be violated; the battery charger will reduce its current as needed. Furthermore, if the load current at V_{OUT} exceeds the programmed power from V_{BUS}, load current will be drawn from the battery via the ideal diodes even when the battery charger is enabled.

The current at CLPROG is a precise fraction of the V_{BUS} current. When a programming resistor and an averaging capacitor are connected from CLPROG to GND, the voltage on CLPROG represents the average input current of the switching regulator. As the input current approaches the programmed limit, CLPROG reaches 1.188V and power delivered by the switching regulator is held constant. Several ratios of current are available which can be set to correspond to USB low and high power modes with a single programming resistor.

OPERATION

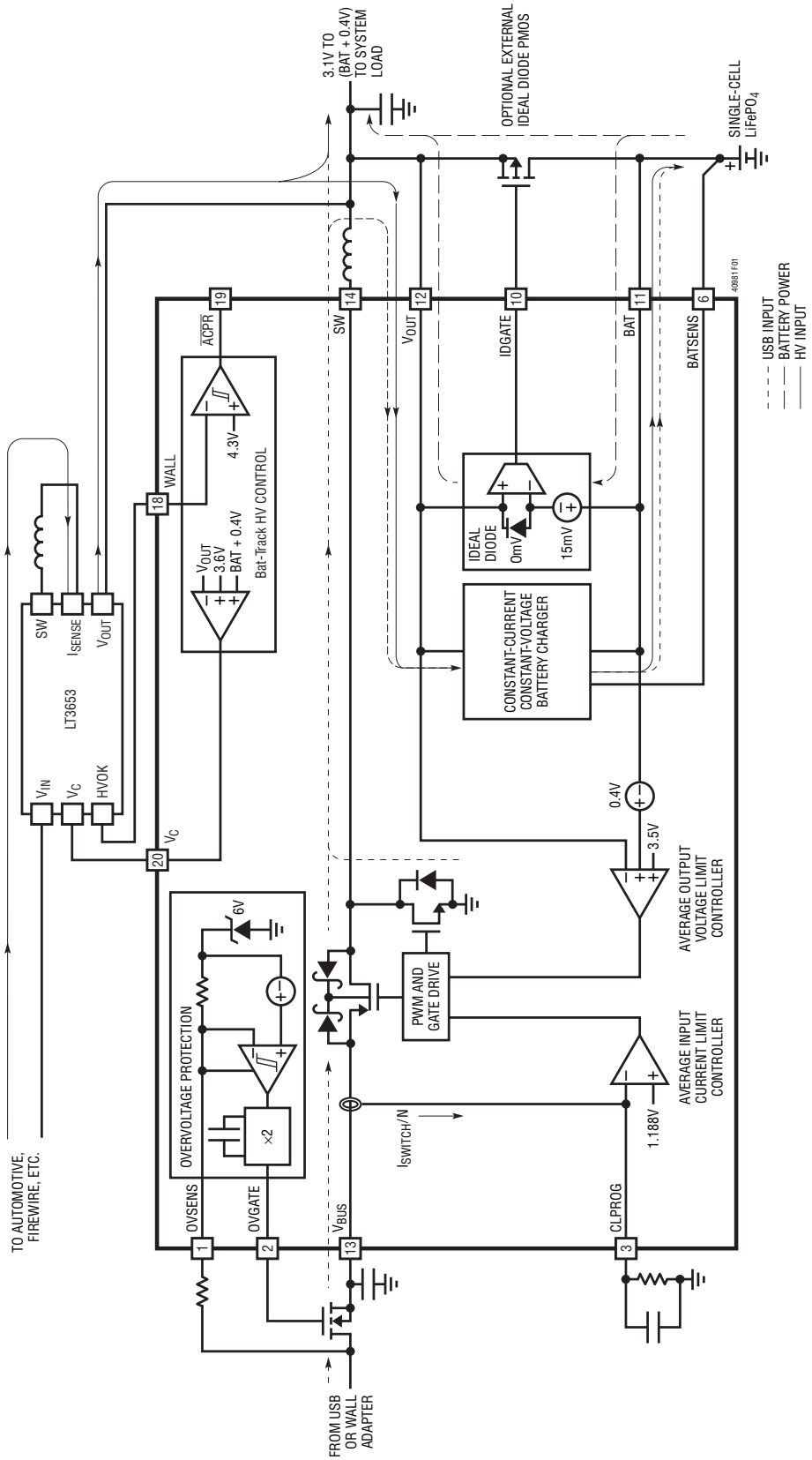


Figure 1. Simplified Power Flow Diagram

OPERATION

The input current limit is programmed by various combinations of the D0, D1 and D2 pins as shown in Table 1. The switching input regulator can also be deactivated (USB suspend).

The average input current will be limited by the CLPROG programming resistor according to the following expression:

$$I_{VBUS} = I_{VBUSQ} + \frac{V_{CLPROG}}{R_{CLPROG}} \bullet (h_{CLPROG} + 1)$$

where I_{VBUSQ} is the quiescent current of the LTC4098-3.6, V_{CLPROG} is the CLPROG servo voltage in current limit, R_{CLPROG} is the value of the programming resistor and h_{CLPROG} is the ratio of the measured current at V_{BUS} to the sample current delivered to CLPROG. Refer to the Electrical Characteristics table for values of h_{CLPROG}, V_{CLPROG} and I_{VBUSQ}. Given worst-case circuit tolerances, the USB specification for the average input current in 1x or 5x mode will not be violated, provided that R_{CLPROG} is 3.01k or greater.

Table 1 shows the available settings for the D0, D1 and D2 pins.

Table 1. Controlled Input Current Limit

D2	D1	D0	CHARGER STATUS	$I_{BUS(LIM)}$
0	0	0	On	100mA (1x)
0	0	1	On	1A (10x)
0	1	0	On	500mA (5x)
0	1	1	Off	500µA (Susp Low)
1	0	0	Off	100mA (1x)
1	0	1	Off	1A (10x)
1	1	0	Off	500mA (5x)
1	1	1	Off	2.5mA (Susp High)

Notice that when D0 is high and D1 is low, the switching regulator is set to a higher current limit for increased charging and power availability at V_{OUT}. These modes will typically be used when there is line power available from a wall adapter.

While not in current limit, the switching regulator's Bat-Track feature will set V_{OUT} to approximately 400mV above the voltage at BAT. However, if the voltage at BAT is below 3.1V, and the load requirement does not cause the switching regulator to exceed its current limit, V_{OUT} will regulate at a fixed 3.5V, as shown in Figure 2. This instant-on operation will allow a portable product to run immediately when power is applied without waiting for the battery to charge.

If the load does exceed the current limit at V_{BUS}, V_{OUT} will range between the no-load voltage and slightly below the battery voltage, indicated by the shaded region of Figure 2.

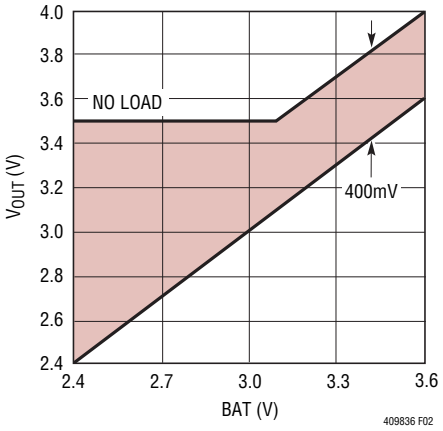


Figure 2. V_{OUT} vs BAT

OPERATION

For very low battery voltages, the battery charger acts like a load and, due to limited input power, its current will tend to pull V_{OUT} below the 3.5V instant-on voltage. To prevent V_{OUT} from falling below this level, an undervoltage circuit automatically detects that V_{OUT} is falling and reduces the battery charge current as needed. This reduction ensures that load current and voltage are always prioritized while allowing as much battery charge current as possible. Refer to Overprogramming the Battery Charger in the Applications Information section.

The voltage regulation loop compensation is controlled by the capacitance on V_{OUT}. An MLCC capacitor of 10µF is required for loop stability. Additional capacitance beyond this value will improve transient response.

An internal undervoltage lockout circuit monitors V_{BUS} and keeps the switching regulator off until V_{BUS} rises above the rising UVLO threshold (4.3V). If V_{BUS} falls below the falling UVLO threshold (4V), system power at V_{OUT} will be drawn from the battery via the ideal diodes.

Bat-Track High Voltage External Switching Regulator Control

The WALL, $\overline{ACPR}$ and V_C pins can be used in conjunction with an external high voltage step-down switching regulator such as the LT3653 or LT3480 to minimize heat production when operating from higher voltage sources, as shown in Figures 3 and 4. Bat-Track control circuitry regulates the external switching regulator's output voltage to the larger of BAT + 400mV or 3.6V. This maximizes battery charger efficiency while still allowing instant-on operation when the battery is deeply discharged.

When using the LT3480, the feedback network should be set to generate an output voltage between 4.5V and 5.5V. When high voltage is applied to the external regulator, WALL will rise toward this programmed output voltage. When WALL exceeds approximately 4.3V, $\overline{ACPR}$ is brought low and the Bat-Track control of the LTC4098-3.6 overdrives the local V_C control of the external high voltage step-down switching regulator. Therefore, once the Bat-Track control is enabled, the output voltage is set independent of the switching regulator feedback network.

Bat-Track control provides a significant efficiency advantage over the simple use of a 5V switching regulator output to drive the battery charger. With a 5V output driving V_{OUT}, battery charger efficiency is approximately:

$$\eta_{TOTAL} = \eta_{BUCK} \bullet \frac{V_{BAT}}{5V}$$

where η_{BUCK} is the efficiency of the high voltage switching regulator and 5V is the output voltage of the switching regulator. With a typical switching regulator efficiency of 87% and a typical battery voltage of 3.4V, the total battery charger efficiency is approximately 59%. Assuming a 1A charge current, well over 2W of power is dissipated just to charge the battery!

With Bat-Track, battery charger efficiency is approximately:

$$\eta_{TOTAL} = \eta_{BUCK} \bullet \frac{BAT}{BAT + 0.4V}$$

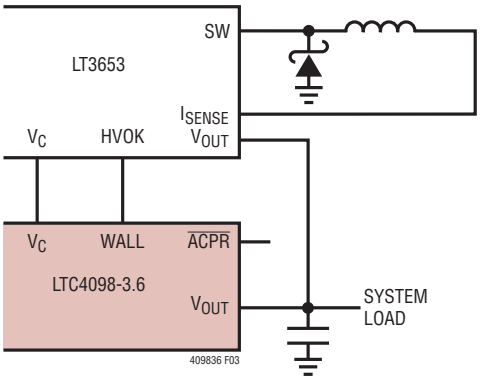


Figure 3. LT3653 Typical Interface

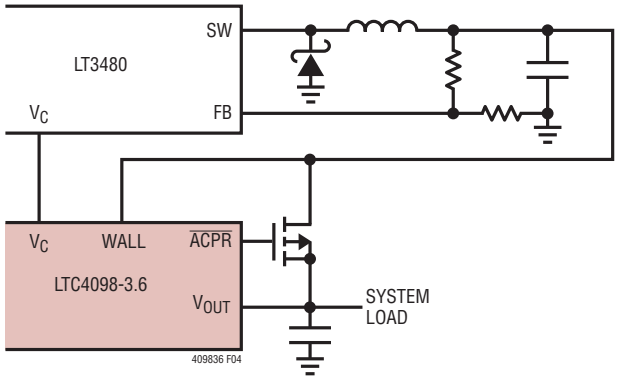


Figure 4. LT3480 Typical Interface

OPERATION

With the same assumptions as previously stated, the total battery charger efficiency is approximately 78%. This example works out to just over 1W of power dissipation, or almost 50% less heat.

See the Typical Applications section for complete circuits using the LT3653 and LT3480 with Bat-Track control.

Overvoltage Protection

The LTC4098-3.6 can protect itself from the inadvertent application of excessive voltage to V_{BUS} or WALL with just two external components: an N-channel MOSFET and a 6.04k resistor. The maximum safe overvoltage magnitude will be determined by the choice of the external N-channel MOSFET and its associated drain breakdown voltage.

The overvoltage protection module consists of two pins. The first, OVSENS, is used to measure the externally applied voltage through an external resistor. The second, OVGATE, is an output used to drive the gate pin of an external FET. The voltage at OVSENS will be lower than the OVP input voltage by (I_{OVSENS} • 6.04k) due to the OVP circuit's quiescent current. The OVP input will be 200mV to 400mV higher than OVSENS under normal operating conditions. When OVSENS is below 6V, an internal charge pump will drive OVGATE to approximately 1.88 • OVSENS. This will enhance the N-channel MOSFET and provide a low impedance connection to V_{BUS} or WALL which will, in turn, power the LTC4098-3.6. If OVSENS should rise above 6V (6.35V OVP input) due to a fault or use of an incorrect wall adapter, OVGATE will be pulled to GND, disabling the external FET to protect downstream circuitry. When the voltage drops below 6V again, the external MOSFET will be reenabled.

In an overvoltage condition, the OVSENS pin will be clamped at 6V. The external 6.04k resistor must be sized appropriately to dissipate the resultant power. For example, a 1/10W 6.04k resistor can have at most $\sqrt{P_{MAX} \bullet 6.04k} = 24V$ applied across its terminals. With the 6V at OVSENS, the maximum overvoltage magnitude that this resistor can withstand is 30V. A 1/4W 6.04k resistor raises this value to 44V. WALL's absolute maximum current rating of 10mA imposes an upper protection limit of 66V.

The charge pump output on OVGATE has limited output drive capability. Care must be taken to avoid leakage on this pin, as it may adversely affect operation.

See the Applications Information section for examples of multiple input protection, reverse input protection, and a table of recommended components.

Ideal Diode from BAT to V_{OUT}

The LTC4098-3.6 has an internal ideal diode as well as a controller for an external ideal diode. Both the internal and the external ideal diodes are always on and will respond quickly whenever V_{OUT} drops below BAT.

If the load current increases beyond the power allowed from the switching regulator, additional power will be pulled from the battery via the ideal diodes. Furthermore, if power to V_{BUS} (USB or wall power) is removed, then all of the application power will be provided by the battery via the ideal diodes. The ideal diodes will be fast enough to keep V_{OUT} from drooping with only the storage capacitance required for the switching regulator. The internal ideal diode consists of a precision amplifier that activates a large on-chip MOSFET transistor whenever the voltage at V_{OUT} is approximately 15mV (V_{FWD}) below the voltage at BAT. Within the amplifier's linear range, the small-signal resistance of the ideal diode will be quite low, keeping the forward drop near 15mV. At higher current levels, the MOSFET will be in full conduction. If additional conductance is needed, an external P-channel MOSFET

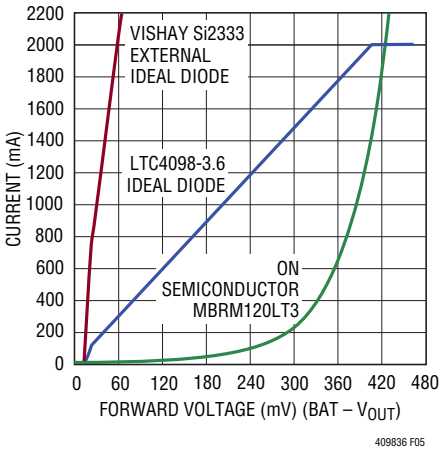


Figure 5. Ideal Diode V-I Characteristics

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transistor may be added from BAT to V_{OUT}. The IDGATE pin of the LTC4098-3.6 drives the gate of the external P-channel MOSFET transistor for automatic ideal diode control. The source of the external P-channel MOSFET should be connected to V_{OUT} and the drain should be connected to BAT. Capable of driving a 1nF load, the IDGATE pin can control an external P-channel MOSFET transistor having an on-resistance of 30mΩ or lower. Figure 5 shows the decreased forward voltage compared to a conventional Schottky diode.

Suspend LDO

The LTC4098-3.6 provides a small amount of power to V_{OUT} in suspend mode by including an LDO from V_{BUS} to V_{OUT}. This LDO will prevent the battery from running down when the portable product has access to a suspended USB port. Regulating at 3.8V, this LDO only becomes active when the switching converter is disabled. In accordance with the USB specification, the input to the LDO is current limited so that it will not exceed the low power or high power suspend specification. If the load on V_{OUT} exceeds the suspend current limit, the additional current will come from the battery via the ideal diodes. The suspend LDO sends a scaled copy of the V_{BUS} current to the CLPROG pin, which will servo to approximately 100mV in this mode. Thus, the high power and low power suspend settings are related to the levels programmed by the same resistor for 1x and 5x modes.

Battery Charger

The LTC4098-3.6 includes a constant-current/constant-voltage battery charger with automatic recharge, automatic termination by safety timer and thermistor sensor input for out-of-temperature charge pausing.

The charger begins charging in full power constant-current mode. The current delivered to the battery will try to reach 1030V/R_{PROG}. Depending on available input power and external load conditions, the battery charger may or may not be able to charge at the full programmed rate. The external load will always be prioritized over the battery charge current. The USB current limit programming will always be observed and only additional power will be available to charge the battery. When system loads are light, battery charge current will be maximized.

Charge Termination

The battery charger has a built-in safety timer. Once the voltage on the battery reaches the preprogrammed float voltage of 3.600V, the charger will regulate the battery voltage there and the charge current will decrease naturally. Once the charger detects that the battery has reached 3.600V, the 1-hour safety timer is started. After the safety timer expires, charging of the battery will discontinue and no more current will be delivered.

Automatic Recharge

Once the battery charger terminates, it will remain off drawing only microamperes of current from the battery. If the portable product remains in this state long enough, the battery will eventually self discharge. To ensure that the battery is always topped off, a charge cycle will automatically begin when the battery voltage falls below V_{RECHRG} (typically 3.5V). In the event that the safety timer is running when the battery voltage falls below V_{RECHRG}, it will reset back to zero. To prevent brief excursions below V_{RECHRG} from resetting the safety timer, the battery voltage must be below V_{RECHRG} for more than 1.5ms. The charge cycle and safety timer will also restart if the V_{BUS} UVLO cycles low and then high (e.g., V_{BUS} is removed and then replaced) or if the charger is momentarily disabled using the D2 pin.

Charge Current

The charge current is programmed using a single resistor from PROG to ground. 1/1030th of the battery charge current is delivered to PROG, which will attempt to servo to 1.000V. Thus, the battery charge current will try to reach 1030 times the current in the PROG pin. The program resistor and the charge current are calculated using the following equations:

$$R_{PROG} = \frac{1030V}{I_{CHG}},\ I_{CHG} = \frac{1030V}{R_{PROG}}$$

In either the constant-current or constant-voltage charging modes, the voltage at the PROG pin will be proportional to the *actual* charge current delivered to the battery. The charge current can be determined at any time

OPERATION

by monitoring the PROG pin voltage and using the following equation:

$$I_{BAT} = \frac{V_{PROG}}{R_{PROG}} \bullet 1030$$

In many cases, the actual battery charge current, I_{BAT}, will be lower than the programmed current, I_{CHG}, due to limited input power available and prioritization to the system load drawn from V_{OUT}.

Charge Status Indication

The $\overline{CHRG}$ pin indicates the status of the battery charger. Four possible states are represented by $\overline{CHRG}$ which include charging, not charging (or float charge current less than programmed end of charge indication current), unresponsive battery and battery temperature out of range.

The signal at the $\overline{CHRG}$ pin can be easily recognized as one of the above four states by either a human or a microprocessor. An open-drain output, the $\overline{CHRG}$ pin can drive an indicator LED through a current limiting resistor for human interfacing or simply a pull-up resistor for microprocessor interfacing.

To make the $\overline{CHRG}$ pin easily recognized by both humans and microprocessors, the pin is either a DC signal of ON for charging, OFF for not charging or it is switched at high frequency (35kHz) to indicate an NTC fault. While switching at 35kHz, its duty cycle is modulated at a slow rate that can be recognized by a human.

When charging begins, $\overline{CHRG}$ is pulled low and remains low for the duration of a normal charge cycle. When charge current drops to 1/10th the value programmed by R_{PROG}, the $\overline{CHRG}$ pin is released (Hi-Z). The $\overline{CHRG}$ pin does not respond to the C/10 threshold if the LTC4098-3.6 is in V_{BUS} current limit. This prevents false end-of-charge indications due to insufficient power available to the battery charger. If a fault occurs while charging, the pin is switched at 35kHz. While switching, its duty cycle is modulated between a high and low value at a very low frequency. The low and high duty cycles are disparate enough to make an LED appear to be on or off thus giving the appearance of "blinking."

Each of the two faults has its own unique "blink" rate for human recognition as well as two unique duty cycles for machine recognition.

Table 2 illustrates the four possible states of the $\overline{CHRG}$ pin when the battery charger is active.

Table 2. $\overline{CHRG}$ Signal

STATUS	FREQUENCY	MODULATION (BLINK) FREQUENCY	DUTY CYCLES
Charging	0Hz	0Hz (Low Z)	100%
I_{BAT} < C/10	0Hz	0Hz (Hi-Z)	0%
NTC Fault	35kHz	1.5Hz at 50%	6.25% or 93.75%
Bad Battery	35kHz	6.1Hz at 50%	12.5% or 87.5%

Notice that an NTC fault is represented by a 35kHz pulse train whose duty cycle toggles between 6.25% and 93.75% at a 1.5Hz rate. A human will easily recognize the 1.5Hz rate as a "slow" blinking which indicates the out of range battery temperature while a microprocessor will be able to decode either the 6.25% or 93.75% duty cycles as an NTC fault.

If a battery is found to be unresponsive to charging (i.e., its voltage remains below 2.85V for 1/2 hour), the $\overline{CHRG}$ pin gives the battery fault indication. For this fault, a human would easily recognize the frantic 6.1Hz "fast" blink of the LED while a microprocessor would be able to decode either the 12.5% or 87.5% duty cycles as a bad cell fault.

Because the LTC4098-3.6 is a 3-terminal PowerPath product, system load is always prioritized over battery charging. Due to excessive system load, there may not be sufficient power to charge the battery beyond the bad-cell threshold voltage within the bad-cell timeout period. In this case the battery charger will falsely indicate a bad cell. System software may then reduce the load and reset the battery charger to try again.

Although very improbable, it is possible that a duty cycle reading could be taken at the bright-dim transition (low duty cycle to high duty cycle). When this happens the duty cycle reading will be precisely 50%. If the duty cycle reading is 50%, system software should disqualify it and take a new duty cycle reading.

OPERATION

NTC Thermistor

The battery temperature is measured by placing a negative temperature coefficient (NTC) thermistor close to the battery pack. The NTC circuitry is shown in the Block Diagram.

To use this feature, connect the NTC thermistor, R_{NTC}, between the NTC pin and ground and a bias resistor, R_{NOM}, from NTCBIAS to NTC. R_{NOM} should be a 1% resistor with a value equal to the value of the chosen NTC thermistor at 25°C (R25).

The LTC4098-3.6 will pause charging when the resistance of the NTC thermistor drops to 0.25 times the value of R25 or approximately 25k (for a Vishay curve 1 thermistor, this corresponds to approximately 60°C). If the battery charger is in constant-voltage (float) mode, the safety timer also pauses until the thermistor indicates a return to a valid temperature. As the temperature drops, the resistance of the NTC thermistor rises. The LTC4098-3.6 is also designed to pause charging when the value of the NTC thermistor increases to 3.26 times the value of R25. For a Vishay curve 1 thermistor, this resistance, 326k, corresponds to approximately 0°C. The hot and cold comparators each have approximately 3°C of hysteresis to prevent oscillation about the trip point. Grounding the NTC pin disables all NTC functionality.

Figure 6 is a flow chart representation of the battery charger algorithm employed by the LTC4098-3.6.

Thermal Regulation

To prevent thermal damage to the LTC4098-3.6 or surrounding components, an internal thermal feedback loop will automatically decrease the programmed charge current if the die temperature rises to approximately 110°C. Thermal regulation protects the LTC4098-3.6 from excessive temperature due to high power operation or high ambient thermal conditions, and allows the user to push the limits of the power handling capability with a given circuit board design without risk of damaging the LTC4098-3.6 or external components. The benefit of the LTC4098-3.6 thermal regulation loop is that charge current can be set according to actual conditions rather than worst-case conditions for a given application with the assurance that the charger will automatically reduce the current in worst-case conditions.

Shutdown Mode

The USB switching regulator is enabled whenever V_{BUS} is above the UVLO voltage and the LTC4098-3.6 is not in one of the two USB suspend modes (500µA or 2.5mA). When power is available from both the USB and high voltage inputs, the high voltage regulator is prioritized and the USB switching regulator is disabled.

The ideal diode is enabled at all times and cannot be disabled.

OPERATION

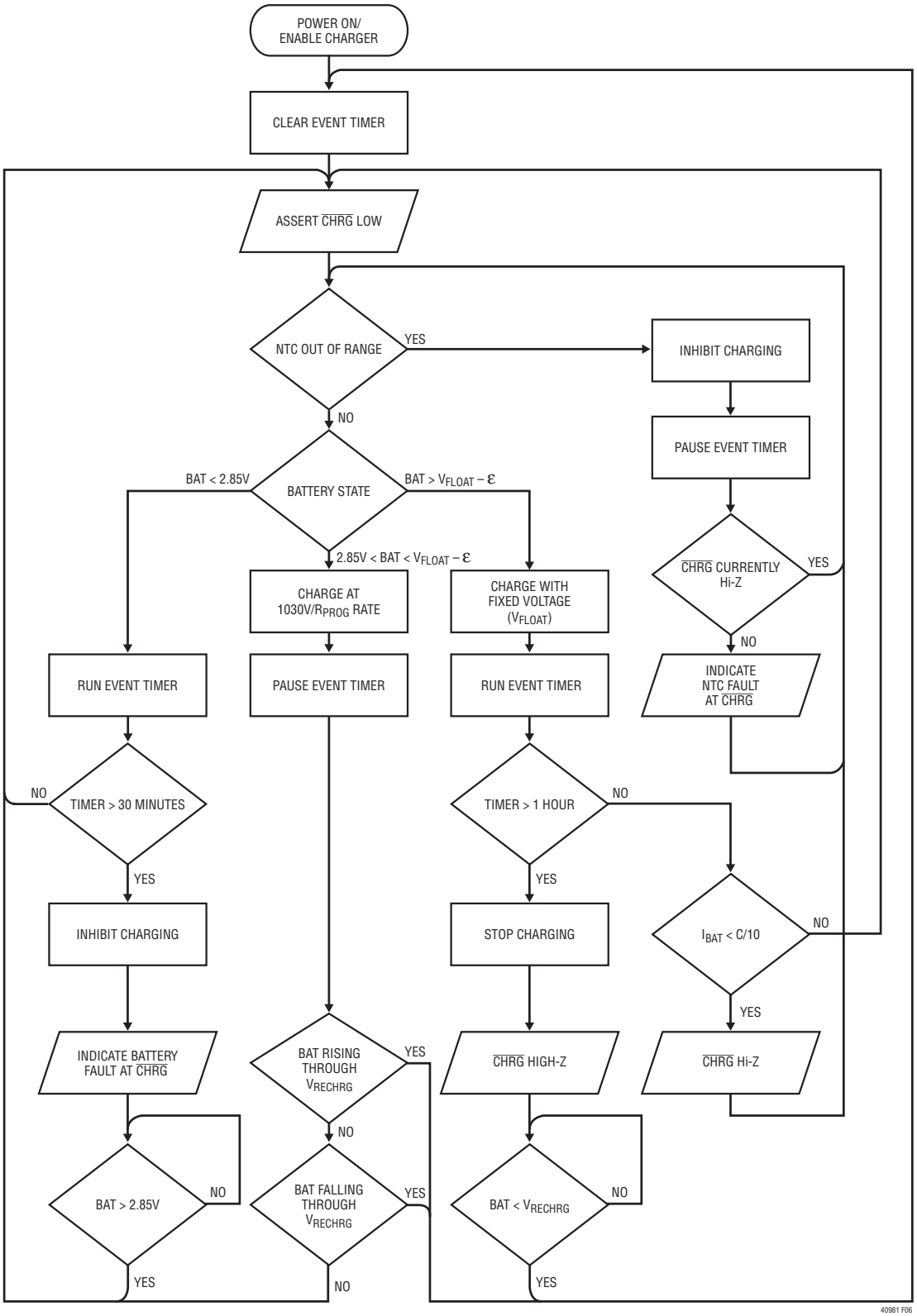


Figure 6. Battery Charger State Diagram

APPLICATIONS INFORMATION

CLPROG Resistor and Capacitor

As described in the Bat-Track Input Current Limited Step Down Switching Regulator section, the resistor on the CLPROG pin determines the average input current limit in each of the five current limit modes. The input current will be comprised of two components, the current that is used to drive V_{OUT} and the quiescent current of the switching regulator. To ensure that the total average input current remains below the USB specification, both components of input current should be considered. The Electrical Characteristics table gives the typical values for quiescent currents in all settings as well as current limit programming accuracy. To get as close to the 500mA or 100mA specifications as possible, a precision resistor should be used.

An averaging capacitor is required in parallel with the resistor so that the switching regulator can determine the average input current. This capacitor also provides the dominant pole for the feedback loop when current limit is reached. To ensure stability, the capacitor on CLPROG should be 0.1µF or larger.

Choosing the Inductor

Because the input voltage range and output voltage range of the PowerPath switching regulator are both fairly narrow, the LTC4098-3.6 was designed for a specific inductance value of 3.3µH. Some inductors which may be suitable for this application are listed in Table 3.

V_{BUS} and V_{OUT} Bypass Capacitors

The style and value of capacitors used with the LTC4098-3.6 determine several important parameters such as regulator control loop stability and input voltage ripple. Because the LTC4098-3.6 uses a step-down switching power supply from V_{BUS} to V_{OUT}, its input current waveform contains high frequency components. It is strongly recommended that a low equivalent series resistance (ESR) multilayer ceramic capacitor be used to bypass V_{BUS}. Tantalum and aluminum capacitors are not recommended because of their high ESR. The value of the capacitor on V_{BUS} directly controls the amount of input ripple for a given load current. Increasing the size of this capacitor will reduce the input ripple. The USB specification allows a maximum of 10µF to be connected directly across the USB power bus. If additional capacitance is required for noise performance, it may be connected directly to the V_{BUS} pin when using the OVP feature of the LTC4098-3.6. This extra capacitance will be soft-connected over several milliseconds to limit inrush current and avoid excessive transient voltage drops on the bus.

To prevent large V_{OUT} voltage steps during transient load conditions, it is also recommended that a ceramic capacitor be used to bypass V_{OUT}. The output capacitor is used in the compensation of the switching regulator. At least 10µF with low ESR are required on V_{OUT}. Additional capacitance will improve load transient performance and stability.

Table 3. Recommended Inductors for the LTC4098-3.6

INDUCTOR TYPE	L (µH)	MAX I_{DC} (A)	MAX DCR (Ω)	SIZE IN mm (L × W × H)	MANUFACTURER
LPS4018	3.3	2.2	0.08	3.9 × 3.9 × 1.7	Coilcraft www.coilcraft.com
D53LC DB318C	3.3 3.3	2.26 1.55	0.034 0.070	5 × 5 × 3 3.8 × 3.8 × 1.8	Toko www.toko.com
WE-TPC Type M1	3.3	1.95	0.065	4.8 × 4.8 × 1.8	Würth Elektronik www.we-online.com
CDRH6D12 CDRH6D38	3.3 3.3	2.2 3.5	0.0625 0.020	6.7 × 6.7 × 1.5 7 × 7 × 4	Sumida www.sumida.com

APPLICATIONS INFORMATION

Multilayer ceramic chip capacitors typically have exceptional ESR performance. MLCCs combined with a tight board layout and an unbroken ground plane will yield very good performance and low EMI emissions.

There are several types of ceramic capacitors available each having considerably different characteristics. For example, X7R ceramic capacitors have the best voltage and temperature stability. X5R ceramic capacitors have apparently higher packing density but poorer performance over their rated voltage and temperature ranges. Y5V ceramic capacitors have the highest packing density, but must be used with caution, because of their extreme nonlinear characteristic of capacitance versus voltage. The actual in-circuit capacitance of a ceramic capacitor should be measured with a small AC signal and DC bias as is expected in-circuit. Many vendors specify the capacitance versus voltage with a $1V_{RMS}$ AC test signal and, as a result, over state the capacitance that the capacitor will present in the application. Using similar operating conditions as the application, the user must measure or request from the vendor the actual capacitance to determine if the selected capacitor meets the minimum capacitance that the application requires.

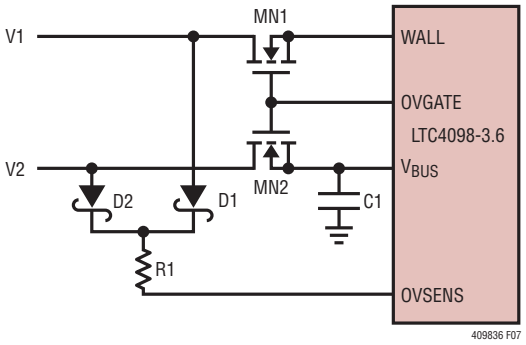


Figure 7. Dual Input Overvoltage Protection

Overprogramming the Battery Charger

The USB high power specification allows for up to 2.5W to be drawn from the USB port. The switching regulator transforms the voltage at V_{BUS} to just above the voltage at BAT with high efficiency, while limiting power to less than the amount programmed at CLPROG. The charger should be programmed (with the PROG pin) to deliver the maximum safe charging current without regard to the USB specifications. If there is insufficient current available to charge the battery at the programmed rate, it will reduce charge current until the system load on V_{OUT} is satisfied and the V_{BUS} current limit is satisfied. Programming the charger for more current than is available will not cause the average input current limit to be violated. It will merely allow the battery charger to make use of all available power to charge the battery as quickly as possible, and with minimal power dissipation within the charger.

Overvoltage Protection

It is possible to protect both V_{BUS} and WALL from overvoltage damage with several additional components, as shown in Figure 7. Schottky diodes D1 and D2 pass the larger of V1 and V2 to R1 and OVSENS. If either V1 or V2 exceeds 6V plus $V_{F(SCHOTTKY)}$, OVGATE will be pulled to GND and both the WALL and USB inputs will be protected. Each input is protected up to the drain-source breakdown, BVDSS, of MN1 and MN2. R1 must also be rated for the power dissipated during maximum overvoltage. See the Operations section for an explanation of this calculation. Table 4 shows some N-channel MOSFETs that may be suitable for overvoltage protection.

Table 4. Recommended OVP MOSFETs

N-CHANNEL MOSFET	BVDSS	R_{ON}	PACKAGE
Si2302ADS	20V	70mΩ	SOT-23
IRLML2502	20V	35mΩ	SOT-23
Si1472DH	30V	65mΩ	SC70-6
NTLJS4114N	30V	20mΩ	2mm × 2mm DFN
FDN372S	30V	45mΩ	SOT-23

APPLICATIONS INFORMATION

Reverse Voltage Protection

The LTC4098-3.6 can also be easily protected against the application of reverse voltage, as shown in Figure 8. D1 and R1 are necessary to limit the maximum VGS seen by MP1 during positive overvoltage events. D1's breakdown voltage must be safely below MP1's BVGS. The circuit shown in Figure 8 offers forward voltage protection up to MN1's BVDSS and reverse voltage protection up to MP1's BVDSS.

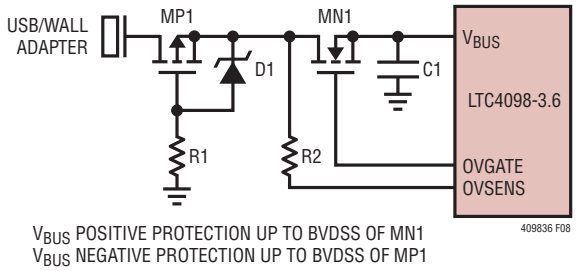


Figure 8. Dual-Polarity Voltage Protection

Alternate NTC Thermistors and Biasing

The LTC4098-3.6 provides temperature-qualified charging if a grounded thermistor and a bias resistor are connected to NTC and NTCBIAS. By using a bias resistor whose value is equal to the room temperature resistance of the thermistor (R25) the upper and lower temperatures are preprogrammed to approximately 60°C and 0°C, respectively (assuming a Vishay curve 1 thermistor).

The upper and lower temperature thresholds can be adjusted by either a modification of the bias resistor value or by adding a second adjustment resistor to the circuit. If only the bias resistor is adjusted, then either the upper or the lower threshold can be modified but not both. The other trip point will be determined by the characteristics of the thermistor. Using the bias resistor in addition to an adjustment resistor, both the upper and the lower temperature trip points can be independently programmed with the constraint that the difference between the upper and lower temperature thresholds cannot decrease. Examples of each technique follow.

NTC thermistors have temperature characteristics which are indicated on resistance-temperature conversion tables. The Vishay-Dale thermistor NTHS0603N011-N1003F, used in the following examples, has a nominal value of 100k and follows the Vishay curve 1 resistance-temperature characteristic.

In the explanation below, the following notation is used.

R25 = Value of the thermistor at 25°C

$R_{NTC|COLD}$ = Value of thermistor at the cold trip point

$R_{NTC|HOT}$ = Value of thermistor at the hot trip point

α_{COLD} = Ratio of $R_{NTC|COLD}$ to R25

α_{HOT} = Ratio of $R_{NTC|HOT}$ to R25

R_{NOM} = Primary thermistor bias resistor (see Figure 9a)

R1 = Optional temperature range adjustment resistor (see Figure 9b)

The trip points for the LTC4098-3.6's temperature qualification are internally programmed at 0.199 • NTCBIAS for the hot threshold and 0.765 • NTCBIAS for the cold threshold.

Therefore, the hot trip point is set when:

$$\frac{R_{NTC|HOT}}{R_{NOM} + R_{NTC|HOT}} \bullet NTCBIAS = 0.199 \bullet NTCBIAS$$

and the cold trip point is set when:

$$\frac{R_{NTC|COLD}}{R_{NOM} + R_{NTC|COLD}} \bullet NTCBIAS = 0.765 \bullet NTCBIAS$$

APPLICATIONS INFORMATION

Solving these equations for $R_{NTC|COLD}$ and $R_{NTC|HOT}$ results in the following:

$$R_{NTC|HOT} = 0.25 \bullet R_{NOM}$$

and

$$R_{NTC|COLD} = 3.26 \bullet R_{NOM}$$

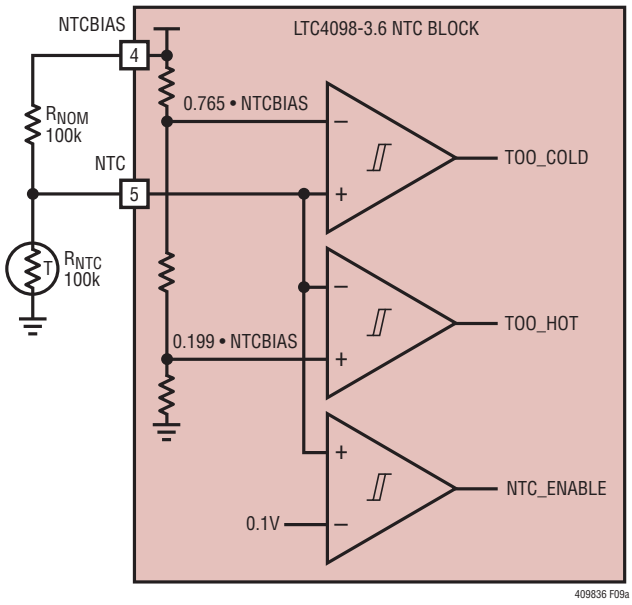
By setting R_{NOM} equal to R25, the previous equations result in α_{HOT} = 0.25 and α_{COLD} = 3.26. Referencing these ratios to the Vishay Resistance-Temperature curve 1 chart gives a hot trip point of about 60°C and a cold trip point of about 0°C. The difference between the hot and cold trip points is approximately 60°C.

By using a bias resistor, R_{NOM}, different in value from R25, the hot and cold trip points can be moved in either direction. The temperature span will change somewhat due to the nonlinear behavior of the thermistor. The following equations can be used to easily calculate a new value for the bias resistor:

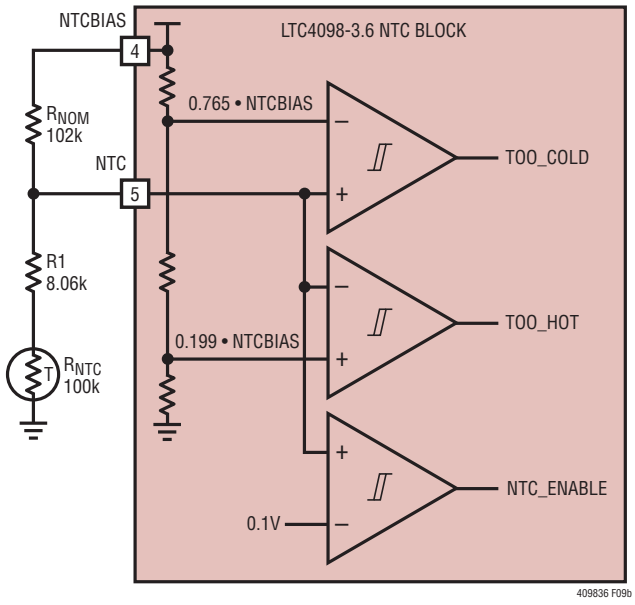
$$R_{NOM} = \frac{\alpha_{HOT}}{0.25} \bullet R25$$

$$R_{NOM} = \frac{\alpha_{COLD}}{3.26} \bullet R25$$

where α_{HOT} and α_{COLD} are the resistance ratios at the *desired* hot and cold trip points. Note that these equations



(9a)



(9b)

Figure 9. NTC Circuits

APPLICATIONS INFORMATION

are linked. Therefore, only one of the two trip points can be chosen, the other is determined by the default ratios designed in the IC. Consider an example where a 70°C hot trip point is desired.

From the Vishay curve 1 R-T characteristics, α_{HOT} is 0.1753 at 70°C. Using the previous equation, R_{NOM} should be set to 70.4k. With this value of R_{NOM}, the cold trip point is 7°C. Notice that the span is now 63°C rather than the previous 60°C. This is due to the decrease in temperature gain of the thermistor as absolute temperature increases.

The upper and lower temperature trip points can be independently programmed by using an additional bias resistor as shown in Figure 9b. The following formulas can be used to compute the values of R_{NOM} and R1:

$$R_{NOM} = \frac{\alpha_{COLD} - \alpha_{HOT}}{3.01} \bullet R25$$

$$R1 = 0.25 \bullet R_{NOM} - \alpha_{HOT} \bullet R25$$

For example, to set the trip points to 0°C and 70°C with a Vishay curve 1 thermistor choose:

$$R_{NOM} = \frac{3.26 - 0.1753}{3.01} \bullet 100k = 102.5k$$

the nearest 1% value is 102k:

$$R1 = 0.25 \bullet 102k - 0.1753 \bullet 100k = 7.97k$$

the nearest 1% value is 8.06k. The final circuit is shown in Figure 9b and results in an upper trip point of 70°C and a lower trip point of 0°C.

USB Inrush Limiting

The USB specification allows at most 10µF of downstream capacitance to be hot-plugged into a USB hub. In most LTC4098-3.6 applications, 10µF should be enough to provide adequate filtering on V_{BUS}.

If more capacitance is required, the OVP circuit will provide adequate soft-connect time to prevent excessive inrush currents. An additional 22µF on the V_{BUS} pin will generally contribute less than 100mA to the hot-plug inrush current.

Voltage overshoot on V_{BUS} may sometimes be observed when connecting the LTC4098-3.6 to a lab power supply. This overshoot is caused by long leads from the power supply to V_{BUS}. Twisting the wires together from the supply to V_{BUS} can greatly reduce the parasitic inductance of these long leads, and keep the voltage at V_{BUS} to safe levels. USB cables are generally manufactured with the power leads in close proximity, and thus fairly low parasitic inductance.

APPLICATIONS INFORMATION

Board Layout Considerations

The exposed pad on the backside of the LTC4098-3.6 package must be securely soldered to the PC board ground. This is the primary ground pin in the package and it serves as the return path for both the control circuitry and the synchronous rectifier.

Furthermore, due to its high frequency switching circuitry, it is imperative that the input capacitor, inductor, and output capacitor be as close to the LTC4098-3.6 as possible and that there be an *unbroken* ground plane under the LTC4098-3.6 and all of its external high frequency components. High frequency currents, such as the input current on the LTC4098-3.6, tend to find their way on the ground plane along a mirror path directly beneath the incident path on the top of the board. If there are slits or cuts in the ground plane due to other traces on that layer, the current will be forced to go around the slits. If high frequency currents are not allowed to flow back through their natural least-area path, excessive voltage will build up and radiated emissions will occur (see Figure 10). There should be a group of vias directly under the grounded backside leading directly down to an internal ground plane. To minimize parasitic inductance, the ground plane should be as close as possible to the top plane of the PC board (layer 2).

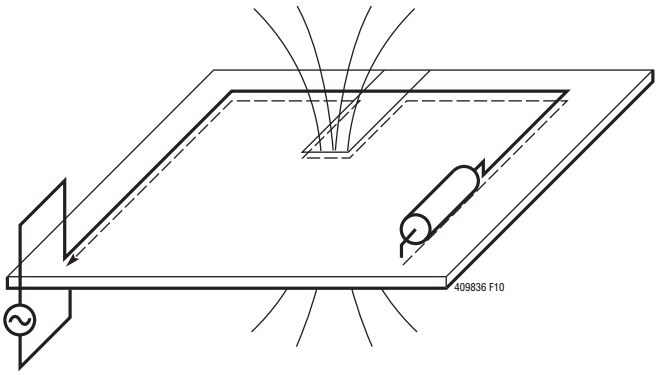


Figure 10. Ground Currents Follow Their Incident Path at High Speed. Slices in the Ground Plane Cause High Voltage and Increased Emissions

The IDGATE pin for the external ideal diode controller has extremely limited drive current. Care must be taken to minimize leakage to adjacent PC board traces. 100nA of leakage from this pin will introduce an additional offset to the ideal diode of approximately 10mV. To minimize leakage, the trace can be guarded on the PC board by surrounding it with V_{OUT} connected metal, which should generally be less than one volt higher than IDGATE.

Battery Charger Stability Considerations

The LTC4098-3.6's battery charger contains both a constant-voltage and a constant-current control loop. The constant-voltage loop is stable without any compensation when a battery is connected with low impedance leads. Excessive lead length, however, may add enough series inductance to require a bypass capacitor of at least 1µF from BAT to GND.

High value, low ESR multilayer ceramic chip capacitors reduce the constant-voltage loop phase margin, possibly resulting in instability. Ceramic capacitors up to 22µF may be used in parallel with a battery, but larger ceramics should be decoupled with 0.2Ω to 1Ω of series resistance.

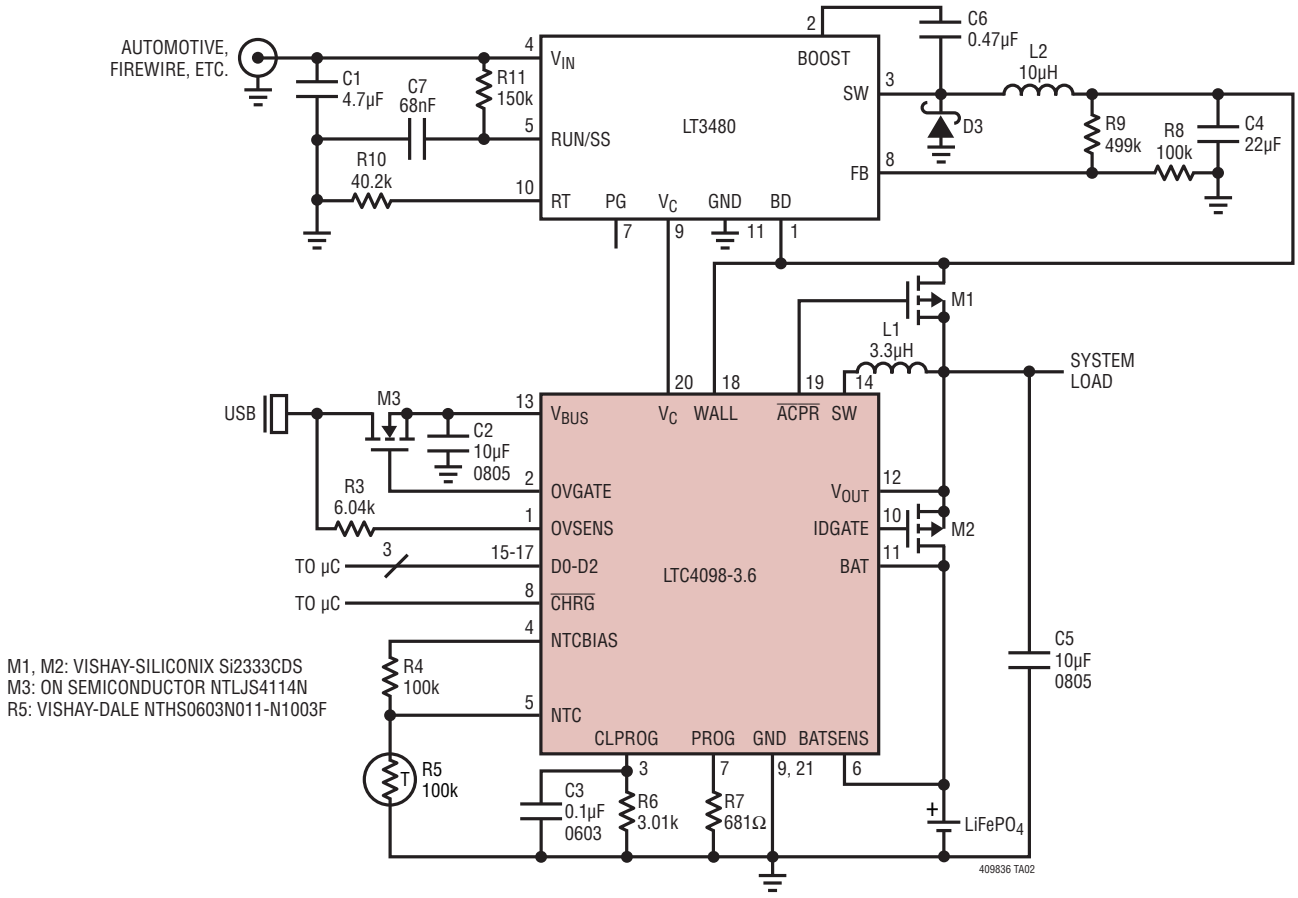
Furthermore, a 100µF MLCC in series with a 0.3Ω resistor or a 100µF OS-CON capacitor from BAT to GND is required to prevent oscillation when the battery is disconnected.

In constant-current mode, the PROG pin is in the feedback loop rather than the battery voltage. Because of the additional pole created by any PROG pin capacitance, capacitance on this pin must be kept to a minimum. With no additional capacitance on the PROG pin, the charger is stable with program resistor values as high as 25k. However, additional capacitance on this node reduces the maximum allowed program resistor. The pole frequency at the PROG pin should be kept above 100kHz. Therefore, if the PROG pin has a parasitic capacitance, C_{PROG}, the following equation should be used to calculate the maximum resistance value for R_{PROG}:

$$R_{PROG} \leq \frac{1}{2\pi \bullet 100kHz \bullet C_{PROG}}$$

TYPICAL APPLICATIONS

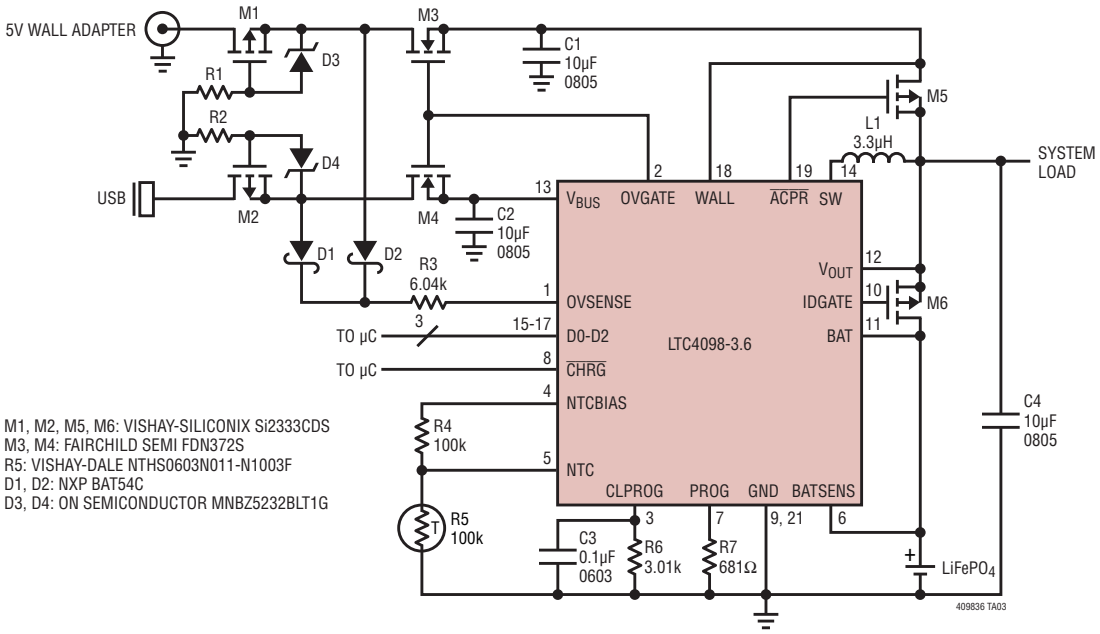
High Efficiency USB/2A Automotive Battery Charger with Overvoltage Protection and Low Battery Start-Up



M1, M2: VISHAY-SILICONIX Si2333CDS
M3: ON SEMICONDUCTOR NTLJS4114N
R5: VISHAY-DALE NTHS0603N011-N1003F

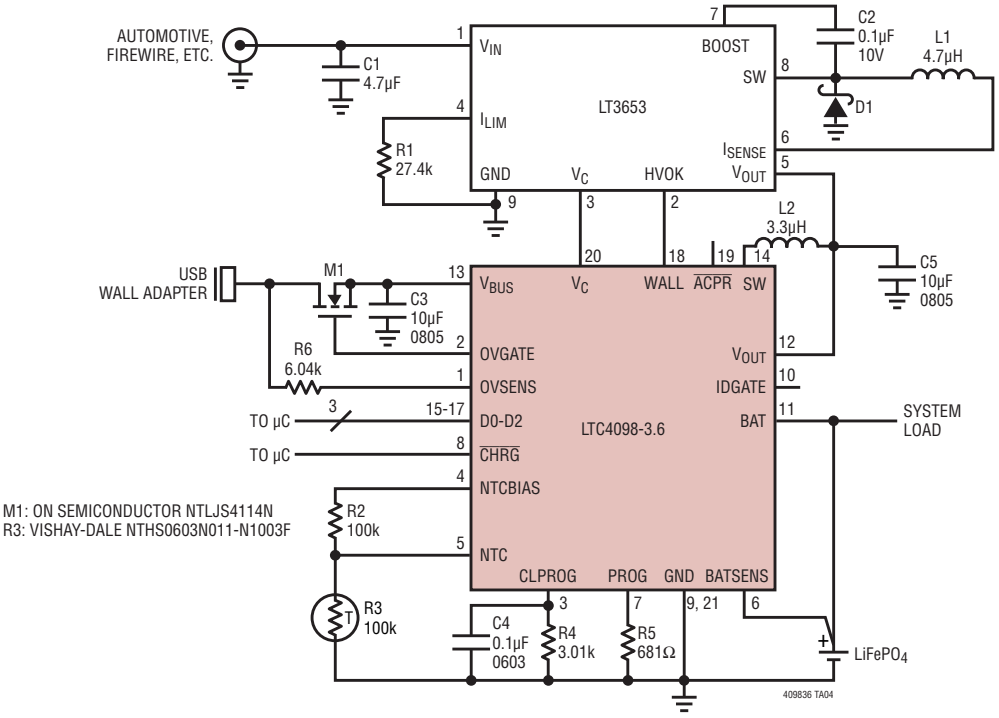
TYPICAL APPLICATIONS

USB/Wall Adapter Battery Charger with Dual Overvoltage Protection, Reverse-Voltage Protection and Low Battery Start-Up



M1, M2, M5, M6: VISHAY-SILICONIX Si2333CDS
M3, M4: FAIRCHILD SEMI FDN372S
R5: VISHAY-DALE NTHS0603N011-N1003F
D1, D2: NXP BAT54C
D3, D4: ON SEMICONDUCTOR MNBZ5232BLT1G

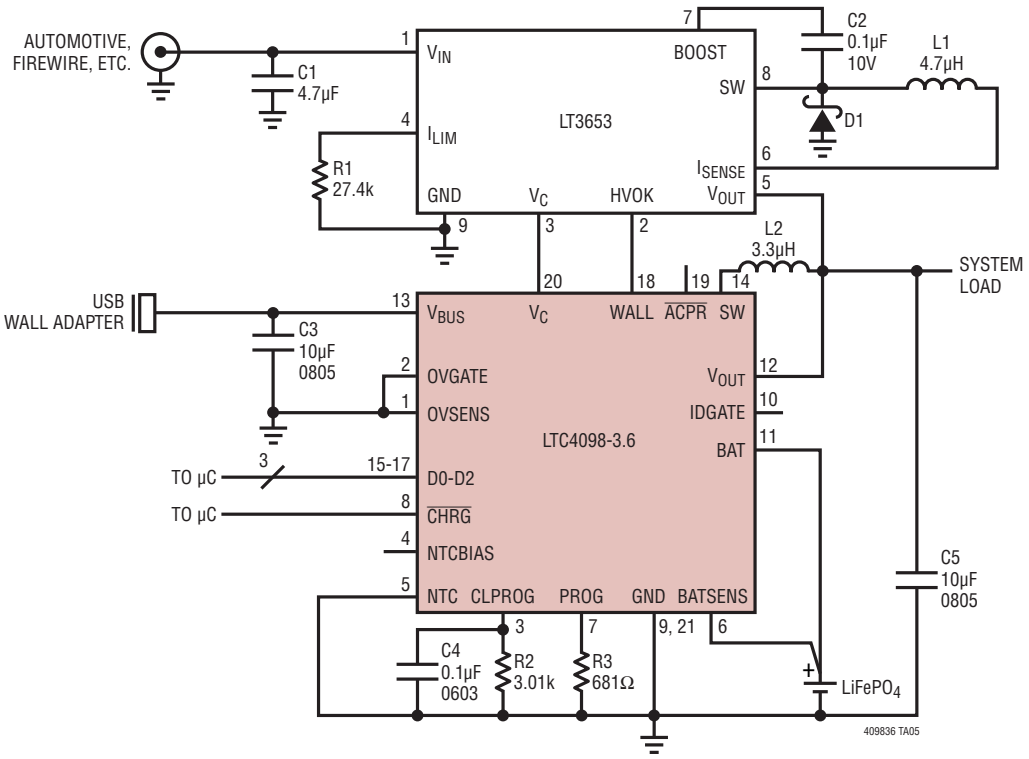
USB/Automotive Switching Battery Charger with Automatic Current Limiting on Both Inputs



M1: ON SEMICONDUCTOR NTLJS4114N
R3: VISHAY-DALE NTHS0603N011-N1003F

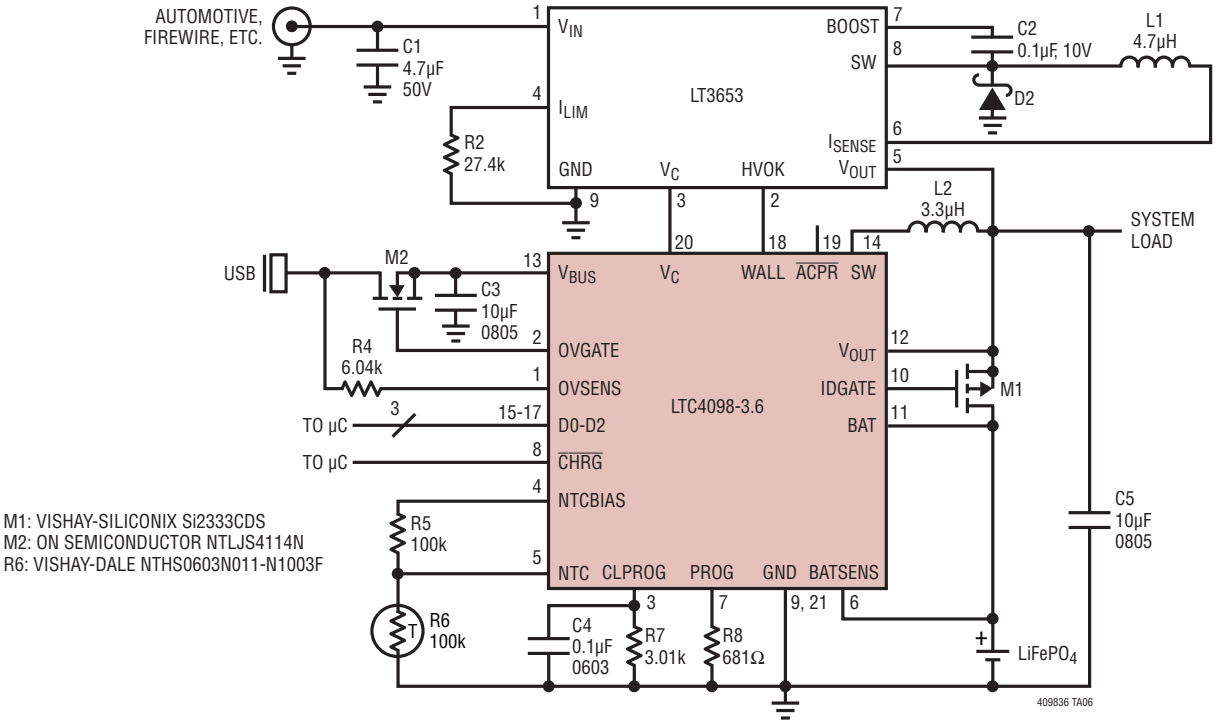
TYPICAL APPLICATIONS

Low Component Count USB and Automotive High Efficiency Power Manager



TYPICAL APPLICATIONS

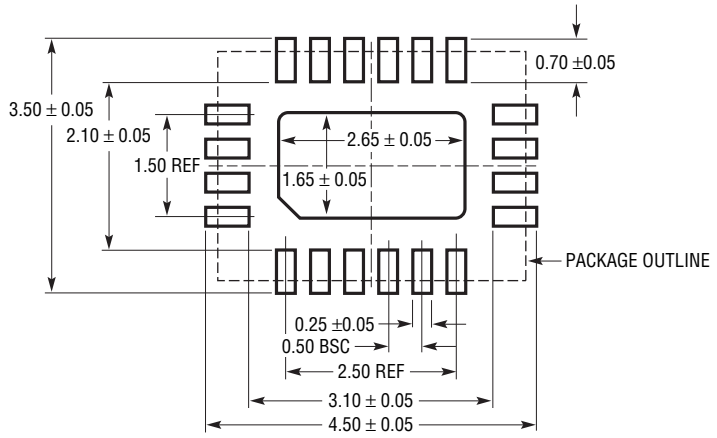
High Efficiency USB Automotive Battery Charger with Overvoltage Protection and Low Battery Start-Up



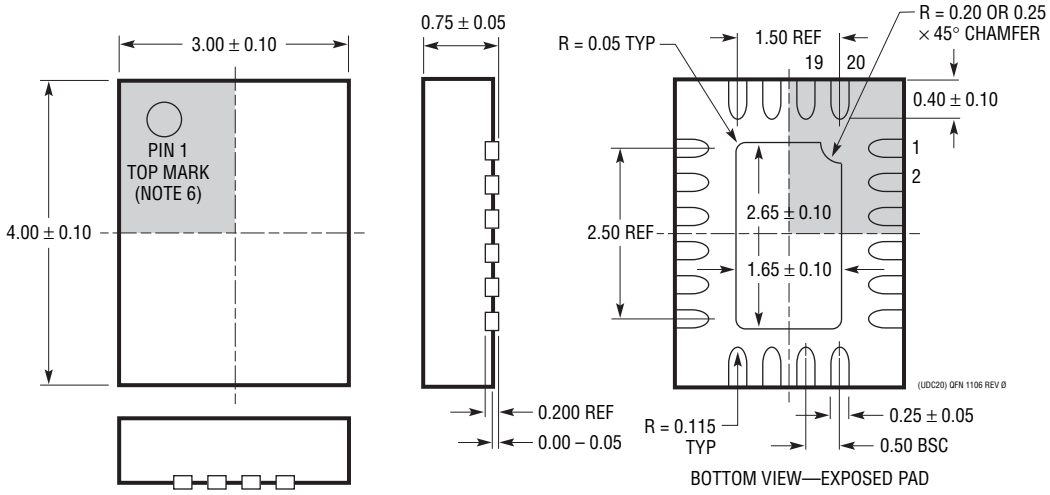
M1: VISHAY-SILICONIX Si2333CDS
M2: ON SEMICONDUCTOR NTLJS4114N
R6: VISHAY-DALE NTHS0603N011-N1003F

PACKAGE DESCRIPTION

UDC Package
20-Lead Plastic QFN (3mm × 4mm)
(Reference LTC DWG # 05-08-1742 Rev Ø)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED

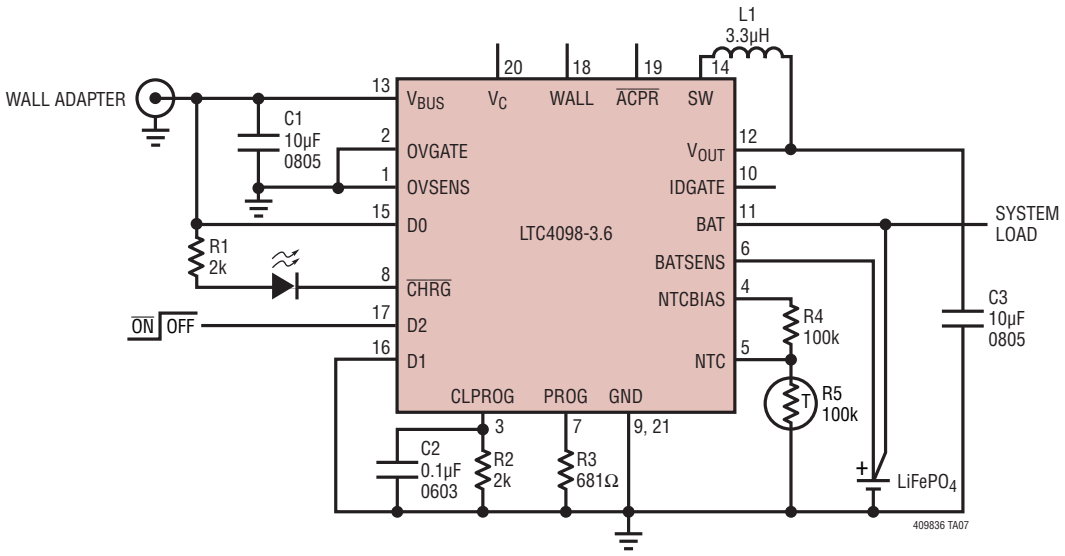


BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

TYPICAL APPLICATION

1.5A Standalone LiFePO$_4$ Charger



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3555/ LTC3555-1/ LTC3555-3	Switching USB Power Manager with Li-Ion/Polymer Charger, Triple Synchronous Buck Converter Plus LDO	Complete Multifunction PMIC: Switch Mode Power Manager and Three Buck Regulators Plus LDO Charge Current Programmable Up to 1.5A from Wall Adapter Input, Synchronous Buck Converters Efficiency >95%, ADJ Outputs: 0.8V to 3.6V at 400mA/400mA/1A Bat-Track Adaptive Output Control, 200mΩ Ideal Diode, 4mm × 5mm QFN-28 Package
LTC3576/ LTC3576-1	Switching Power Manager with USB On-The-Go Plus Triple Step-Down DC/DCs	Complete Multifunction PMIC: Bidirectional Switching Power Manager Plus Three Buck Regulators Plus LDO, ADJ Output Down to 0.8V at 400mA/400mA/1A, Overvoltage Protection, USB On-The-Go, Charge Current Programmable Up to 1.5A from Wall Adapter Input, Thermal Regulation, I^{2}C, High Voltage Bat-Track Buck Interface, 180mΩ Ideal Diode; 4mm × 6mm QFN-38 Package
LTC4088	High Efficiency USB Power Manager and Battery Charger	Maximizes Available Power from USB Port, Bat-Track, Instant-On Operation, 1.5A Max Charge Current, 180mΩ Ideal Diode with <50mΩ Option, 3.3V/25mA Always-On LDO, 4mm × 3mm DFN-14 Package
LTC4090/ LTC4090-5	High Voltage USB Power Manager with Ideal Diode Controller and High Efficiency Li-Ion Battery Charger	High Efficiency 1.2A Charger from 6V to 38V (60V Max) Input. Charges Single-Cell Li-Ion/ Polymer Batteries Directly from a USB Port, Thermal Regulation, 200mΩ Ideal Diode with <50mΩ Option, 6mm × 3mm DFN-22 Package. Bat-Track Adaptive Output Control
LTC4099	I^{2}C Controlled USB Switch Mode Power Manager with OVP	66V OVP I^{2}C for Control and Status Readback, Overtemperature Battery Conditioner for Added Battery Safety Margin, Maximizes Available Power from USB Port, Bat-Track, Instant-On Operation, 1.5A Maximum Charge Current from Wall, 600mA Charge Current from USB, 180mΩ Ideal Diode with <50mΩ Option; 3mm × 4mm QFN-20 Package
LTC4413	Dual Ideal Diodes	3mm × 3mm DFN Package, Low Loss Replacement for ORing Diodes
LT3652HV	Power Tracking 2A Battery Charger	High V_{IN}: 34V Operating, 40V Abs Max, 2A Monolithic Nonsynchronous Buck Charger with Input Voltage Regulation Loop. Programmable Float Voltage Up to 18V.

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