MCM54260B
MCM5L4260B
MCM5S4260B

Advance Information

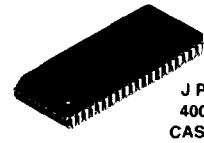
256K x 16 CMOS Dynamic RAM

Fast Page Mode – 2 CAS, 1 Write Enable

The MCM54260B is a 0.6µ CMOS high–speed dynamic random access memory. It is organized as 262,144 sixteen–bit words and fabricated with CMOS silicon–gate process technology. Advanced circuit design and fine line processing provide high performance, improved reliability, and low cost.

The MCM54260B requires only 9 address lines; row and column address inputs are multiplexed. The device is packaged in a standard 400 mil SOJ plastic package and a 400 mil thin–small–outline package (TSOP).

- Three–State Data Output
- Fast Page Mode
- TTL–Compatible Inputs and Outputs
- $\overline{RAS}$–Only Refresh
- $\overline{CAS}$ Before $\overline{RAS}$ Refresh
- Hidden Refresh
- 512 Cycle Refresh:
  MCM54260B = 8 ms
  MCM5L4260B = 64 ms
  MCM5S4260B = 64 ms
- Fast Access Time (t_{RAC}):
  MCM54260B–70, MCM5L4260B–70, and MCM5S4260B–70 = 70 ns (Max)
  MCM54260B–80, MCM5L4260B–80, and MCM5S4260B–80 = 80 ns (Max)
  MCM54260B–10, MCM5L4260B–10, and MCM5S4260B–10 = 100 ns (Max)
- Low Active Power Dissipation:
  MCM54260B–70, MCM5L4260B–70, and MCM5S4260B–70 = 550 mW (Max)
  MCM54260B–80, MCM5L4260B–80, and MCM5S4260B–80 = 468 mW (Max)
  MCM54260B–10, MCM5L4260B–10, and MCM5S4260B–10 = 413 mW (Max)
- Low Standby Power Dissipation:
  MCM54260B, MCM5L4260B, and MCM5S4260B= 5.5 mW (Max, TTL Levels)
- Battery Backup Power Dissipation:
  MCM5L4260B and MCM5S4260B = 1.7 mW (Max, Battery Backup Mode, t_{RC} = 125 µs)



J PACKAGE
400 MIL SOJ
CASE 923A–01

T PACKAGE
400 MIL TSOP
CASE 924–01

PIN NAMES	
A0 – A8	Address Inputs
DQ0 – DQ15	Data Input/Output
$\overline{W}$	Read/Write Enable
$\overline{RAS}$	Row Address Strobe
$\overline{LCAS}$, $\overline{UCAS}$	Column Address Strobe
V_{CC}	Power Supply (+ 5 V)
V_{SS}	Ground
NC	No Connect
$\overline{G}$	Output Enable

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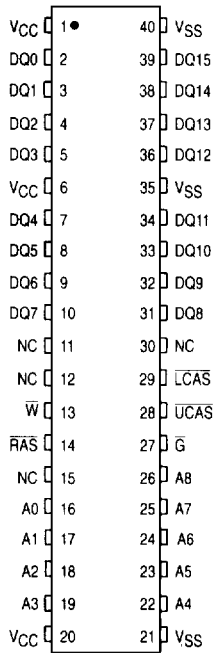
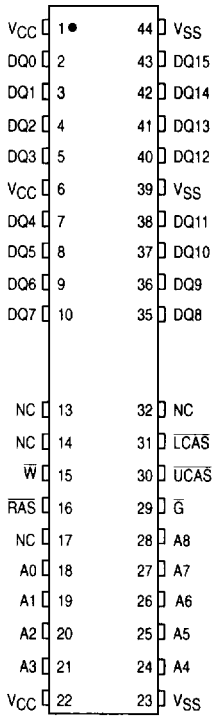
PIN ASSIGNMENTS

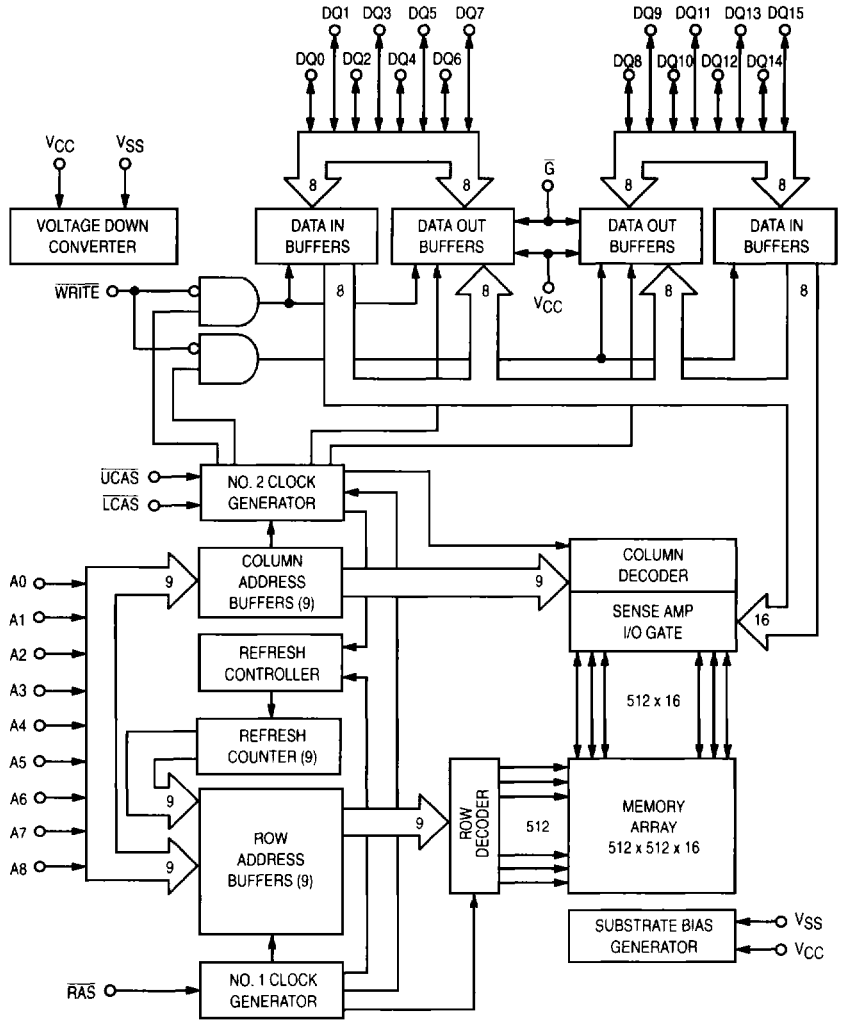
400 MIL SOJ



400 MIL TSOP



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 1 to + 7	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 1 to + 7	V
Data Out Current	I_{out}	50	mA
Power Dissipation	P_D	700	mW
Operating Temperature Range	T_A	0 to + 70	°C
Storage Temperature Range	T_{stg}	– 55 to + 150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	
Logic High Voltage, All Inputs	V_{IH}	2.4	—	6.0	V
Logic Low Voltage, All Inputs Except DQ0 – DQ15	V_{IL}	– 0.5*	—	0.8	V
Logic Low Voltage, DQ0 – DQ15	V_{IL}	– 0.5*	—	0.8	V

*– 2.0 V at pulse width ≤ 20 ns

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DC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current	I_{CC1}			mA	1, 2
MCM54260B–70, MCM5L4260B–70, and MCM5S4260B–70, t_{RC} = 130 ns		—	100		
MCM54260B–80, MCM5L4260B–80, and MCM5S4260B–80, t_{RC} = 150 ns		—	85		
MCM54260B–10, MCM5L4260B–10, and MCM5S4260B–10, t_{RC} = 180 ns		—	75		
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	—	2	mA	
V_{CC} Power Supply Current During $\overline{RAS}$ Only Refresh Cycles ($\overline{CAS}$ = V_{IH})	I_{CC3}			mA	1, 2
MCM54260B–70, MCM5L4260B–70, and MCM5S4260B–70, t_{RC} = 130 ns		—	100		
MCM54260B–80, MCM5L4260B–80, and MCM5S4260B–80, t_{RC} = 150 ns		—	85		
MCM54260B–10, MCM5L4260B–10, and MCM5S4260B–10, t_{RC} = 180 ns		—	75		
V_{CC} Power Supply Current During Fast Page Mode Cycle ($\overline{RAS}$ = V_{IL})	I_{CC4}			mA	1, 2
MCM54260B–70, MCM5L4260B–70, and MCM5S4260B–70, t_{PC} = 45 ns		—	70		
MCM54260B–80, MCM5L4260B–80, and MCM5S4260B–80, t_{PC} = 50 ns		—	60		
MCM54260B–10, MCM5L4260B–10, and MCM5S4260B–10, t_{PC} = 60 ns		—	55		
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V) MCM54260B	I_{CC5}	—	1.0	mA	
MCM5L4260B		—	200	µA	
MCM5S4260B		—	200	µA	
V_{CC} Power Supply Current During $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle	I_{CC6}			mA	1
MCM54260B–70, MCM5L4260B–70, and MCM5S4260B–70, t_{RC} = 130 ns		—	100		
MCM54260B–80, MCM5L4260B–80, and MCM5S4260B–80, t_{RC} = 150 ns		—	85		
MCM54260B–10, MCM5L4260B–10, and MCM5S4260B–10, t_{RC} = 180 ns		—	75		
V_{CC} Power Supply Current, Battery Backup Mode—MCM5L4260B and MCM5S4260B (t_{RC} = 125 µs; t_{RAS} = 1 µs; $\overline{CAS}$ = $\overline{CAS}$ Before $\overline{RAS}$ Cycle or 0.2 V; A0 – A8, $\overline{W}$, D = V_{CC} – 0.2 V or 0.2 V)	I_{CC7}	—	300	µA	1, 3
Input Leakage Current (0 V ≤ V_{in} ≤ 7.0 V)	$I_{lkg(I)}$	– 10	10	µA	
Output Leakage Current (0 V ≤ V_{out} ≤ 7.0 V, Output Disable)	$I_{lkg(O)}$	– 10	10	µA	
Output High Voltage (I_{OH} = – 5 mA)	V_{OH}	2.4	—	V	
Output Low Voltage (I_{OL} = 4.2 mA)	V_{OL}	—	0.4	V	

NOTES:
1. Current is a function of cycle rate and output loading. Maximum currents are at the specified cycle time (min) with the output open.
2. Column address can be changed once or less while $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
3. t_{RAS} (max) = 1 µs is only applied to refresh of battery back-up. t_{RAS} (max) = 10 µs is applied to functional operating.

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, periodically sampled, not 100% tested)

Parameter		Symbol	Max	Unit
Input Capacitance	A0 – A8	C_{in}	5	pF
	$\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{G}$		7	
Input/Output Capacitance ($\overline{CAS}$ = V_{IH} to Disable Output)	DQ0 – DQ15	C_{out}	7	pF

NOTE: Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: C = I Δt/ΔV.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

READ, WRITE, AND READ–MODIFY–WRITE CYCLES (See Notes 1, 2, 3, 4, and 5)

Parameter	Symbol		MCM54260B–70 MCM5L4260B–70 MCM5S4260B–70		MCM54260B–80 MCM5L4260B–80 MCM5S4260B–80		MCM54260B–10 MCM5L4260B–10 MCM5S4260B–10		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	130	—	150	—	180	—	ns	5
Read–Modify–Write Cycle Time	t_{RELREL}	t_{RWC}	185	—	205	—	245	—	ns	5
Page Mode Cycle Time	t_{CELCEL}	t_{PC}	45	—	50	—	60	—	ns	
Page Mode Read–Modify–Write Cycle Time	t_{CELCEL}	t_{PRWC}	100	—	105	—	125	—	ns	
Access Time from $\overline{RAS}$	t_{RELQV}	t_{RAC}	—	70	—	80	—	100	ns	6,7,8
Access Time from $\overline{CAS}$	t_{CELQV}	t_{CAC}	—	20	—	20	—	25	ns	6, 7
Access Time from Column Address	t_{AVQV}	t_{AA}	—	35	—	40	—	50	ns	6, 8
Access Time from $\overline{CAS}$ Precharge	t_{CEHQV}	t_{CPA}	—	40	—	45	—	55	ns	6
$\overline{CAS}$ to Output in Low–Z	t_{CELQX}	t_{CLZ}	0	—	0	—	0	—	ns	6
Output Buffer Turn–Off Delay	t_{CEHQZ}	t_{OFF}	0	15	0	15	0	20	ns	9
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{REHREL}	t_{RP}	50	—	60	—	70	—	ns	
$\overline{RAS}$ Pulse Width	t_{RELREH}	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ Pulse Width (Page Mode)	t_{RELREH}	t_{RASP}	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ Hold Time	t_{CELREH}	t_{RSH}	20	—	20	—	25	—	ns	
$\overline{CAS}$ Hold Time	t_{RELCEH}	t_{CSH}	70	—	80	—	100	—	ns	
$\overline{CAS}$ Pulse Width	t_{CELCEH}	t_{CAS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RELCEL}	t_{RCD}	20	50	20	60	25	75	ns	7
$\overline{RAS}$ to Column Address Delay Time	t_{RELAV}	t_{RAD}	15	35	15	40	20	50	ns	8
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CEHREL}	t_{CRP}	5	—	5	—	10	—	ns	
$\overline{CAS}$ Precharge Time (Page Mode Only)	t_{CEHCEL}	t_{CP}	10	—	10	—	10	—	ns	
$\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge (Page Mode Only)	t_{CEHREH}	t_{RHCP}	40	—	45	—	55	—	ns	
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	10	—	10	—	15	—	ns	
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	15	—	15	—	20	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{AVREH}	t_{RAL}	35	—	40	—	50	—	ns	

(continued)

NOTES:

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 100 µs is required after power–up followed by 8 $\overline{RAS}$ only refresh cycles or 8 CAS before $\overline{RAS}$ refresh cycles, before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. The specifications for t_{RC} (min) and t_{RMW} (min) are used only to indicate cycle time at which proper operation over the full temperature range (0 ≤ T_A ≤ 70°C) is ensured.
6. Measured with a current load equivalent to 2 TTL (– 200 µA, + 4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
7. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
8. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
9. t_{OFF} (max) and t_{GZ} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

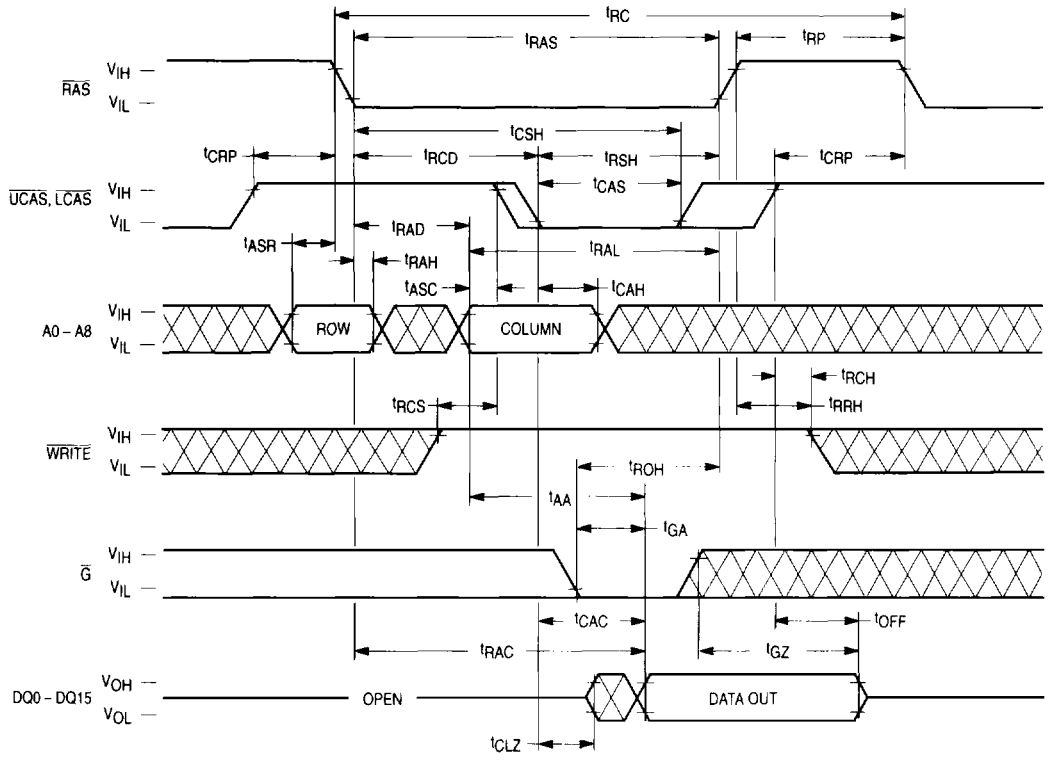
READ, WRITE, AND READ–MODIFY–WRITE CYCLES (Continued)

Parameter	Symbol		MCM54260B–70 MCM5L4260B–70 MCM5S4260B–70		MCM54260B–80 MCM5L4260B–80 MCM5S4260B–80		MCM54260B–10 MCM5L4260B–10 MCM5S4260B–10		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max		
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time	t_{CEHWX}	t_{RCH}	0	—	0	—	0	—	ns	10
Read Command Hold Time Referenced to $\overline{RAS}$	t_{REHWX}	t_{RRH}	0	—	0	—	0	—	ns	10
Write Command Hold Time	t_{CELWH}	t_{WCH}	15	—	15	—	20	—	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	15	—	15	—	20	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{WLREH}	t_{RWL}	20	—	20	—	25	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{WLCEH}	t_{CWL}	20	—	20	—	25	—	ns	
Data in Setup Time	t_{DVCEL}	t_{DS}	0	—	0	—	0	—	ns	11
Data in Hold Time	t_{CELDX}	t_{DH}	15	—	15	—	20	—	ns	11
Refresh Period MCM54260B MCM5L4260B MCM5S4260B	t_{RVRV}	t_{RFSH}	— — —	8 64 64	— — —	8 64 64	— — —	8 64 64	ms	
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	—	0	—	0	—	ns	12
$\overline{CAS}$ to Write Delay	t_{CELWL}	t_{CWD}	50	—	50	—	60	—	ns	12
$\overline{RAS}$ to Write Delay	t_{RELWL}	t_{RWD}	100	—	110	—	135	—	ns	12
Column Address to Write Delay	t_{AVWL}	t_{AWD}	65	—	70	—	85	—	ns	12
$\overline{CAS}$ Precharge to Write Delay	t_{CEHWL}	t_{CPWD}	70	—	75	—	90	—	ns	12
$\overline{CAS}$ Setup Time for CAS Before $\overline{RAS}$ Cycle	t_{RELCEL}	t_{CSR}	5	—	5	—	5	—	ns	
$\overline{CAS}$ Hold Time for $\overline{CAS}$ Before $\overline{RAS}$ Cycle	t_{RELCEH}	t_{CHR}	15	—	15	—	20	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time	t_{REHCEL}	t_{RPC}	5	—	5	—	5	—	ns	
$\overline{CAS}$ Precharge Time ($\overline{CAS}$ Before $\overline{RAS}$ Counter Test)	t_{CEHCEL}	t_{CPT}	30	—	30	—	40	—	ns	
$\overline{RAS}$ Hold Time Referenced to $\overline{G}$	t_{GLREH}	t_{ROH}	10	—	10	—	20	—	ns	
G Access Time	t_{GLQV}	t_{GA}	—	20	—	20	—	25	ns	6
$\overline{G}$ to Data Delay	t_{GLHDX}	t_{GD}	20	—	20	—	25	—	ns	
Output Buffer Turn–Off Delay Time from $\overline{G}$	t_{GHQZ}	t_{GZ}	0	20	0	20	0	25	ns	9
$\overline{G}$ Command Hold Time	t_{WLGL}	t_{GH}	20	—	20	—	25	—	ns	
Output Disable Setup Time	t_{GLCEL}	t_{GDS}	0	—	0	—	0	—	ns	

NOTES:

10. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
11. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{W}$ leading edge in late write or read–write cycles.
12. t_{WCS}, t_{RWD}, t_{CWD}, t_{CPWD}, and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{CPWD} \geq t_{CPWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read–modify–write cycle and the data out will contain data read from the selected cell. If neither of these sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

READ CYCLE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tRAS
tRP
RAS
VIH
VIL
tCSH
tCRP
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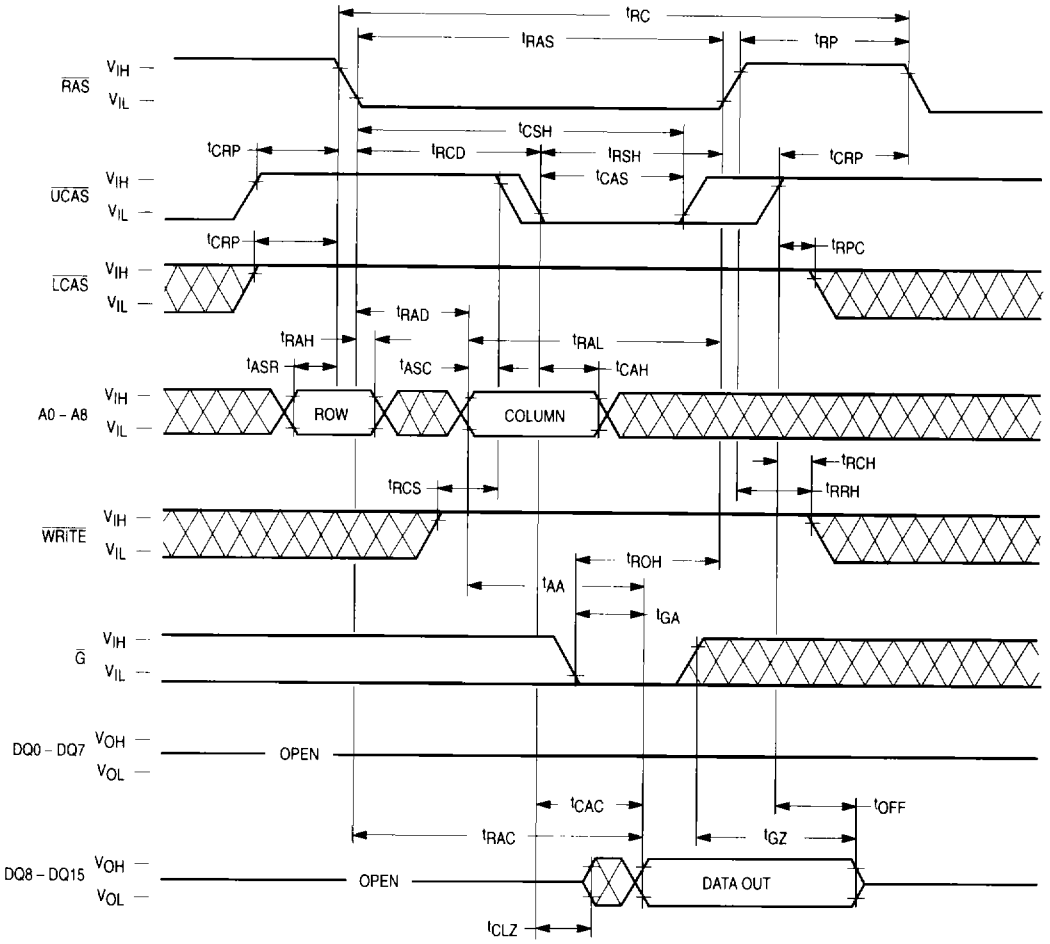
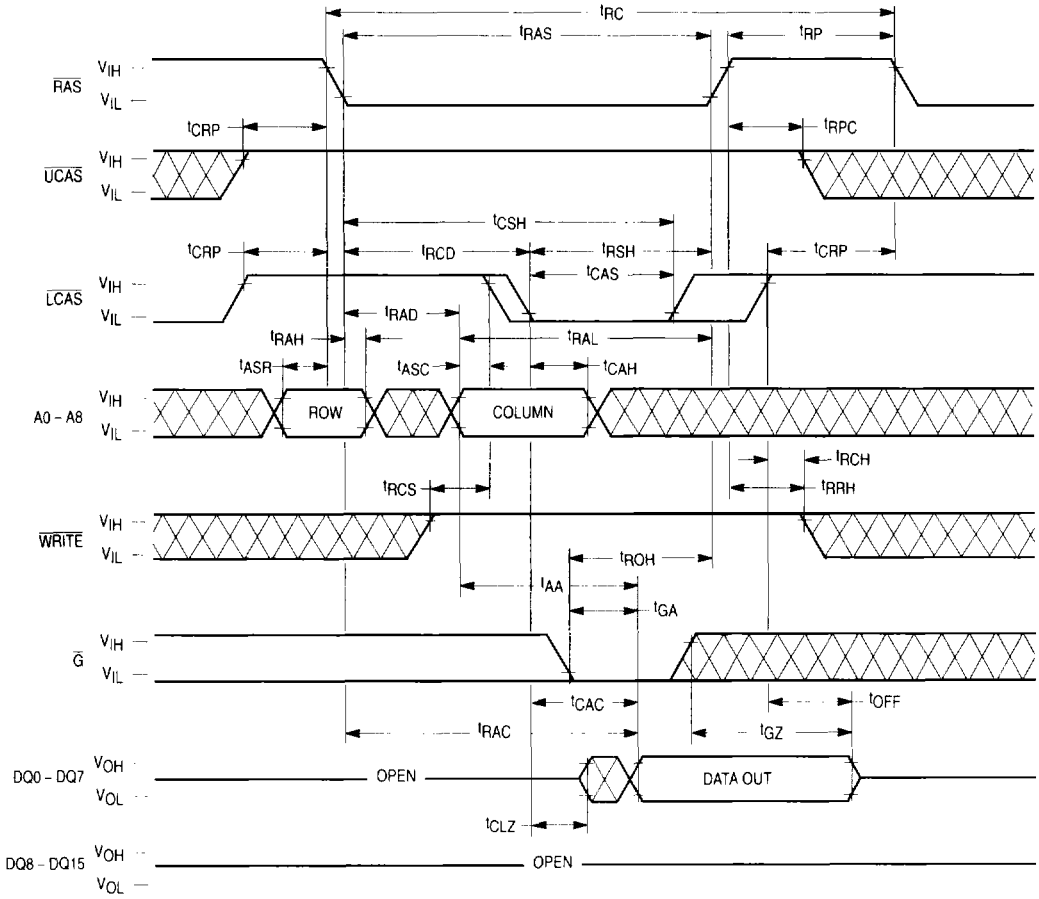
tCRP
tCAS
UCAS, LCAS
tRAD
tASR
tRAH
tRAL
tASC
tCAH
A0 – A8
ROW
COLUMN
tRCH
tRCS
tRRH
WRITE
tROH
tAA
tGA
G
tCAC
tOFF
tRAC
tGZ
DQ0 – DQ15
VOH
VOL
OPEN
DATA OUT
tCLZ

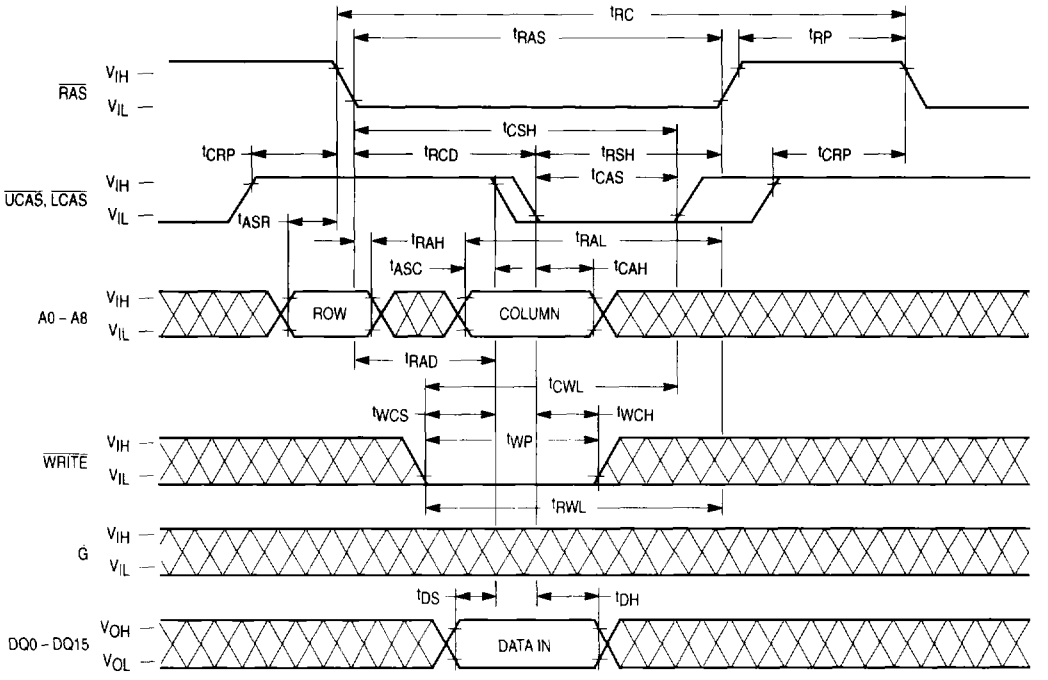
UPPER BYTE READ CYCLE



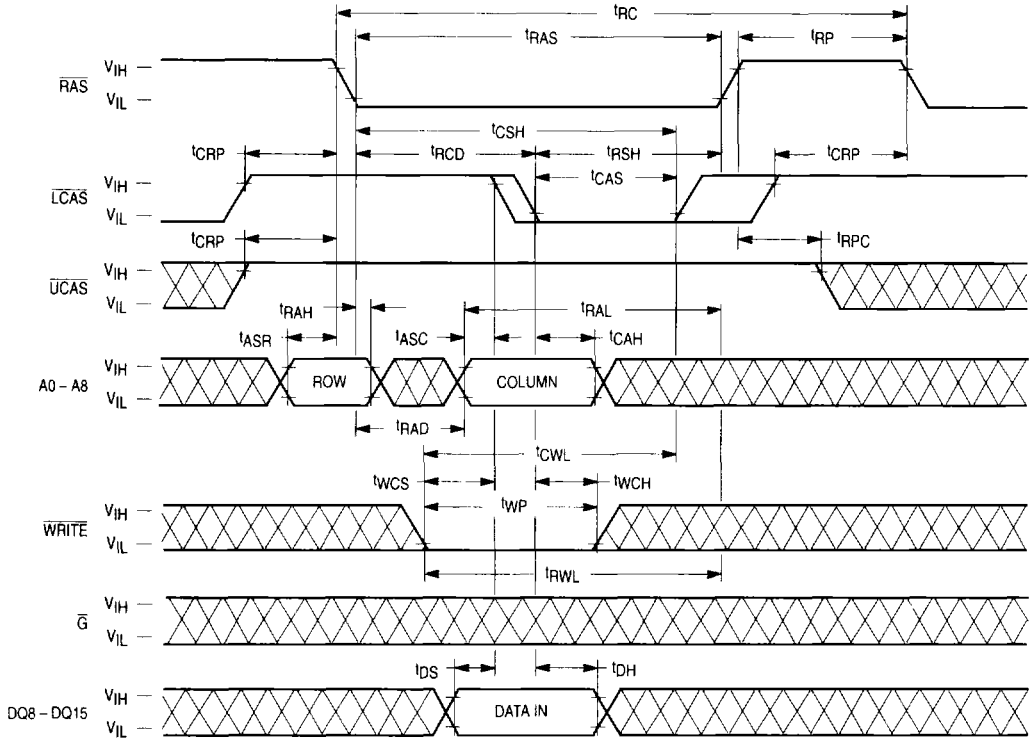
LOWER BYTE READ CYCLE



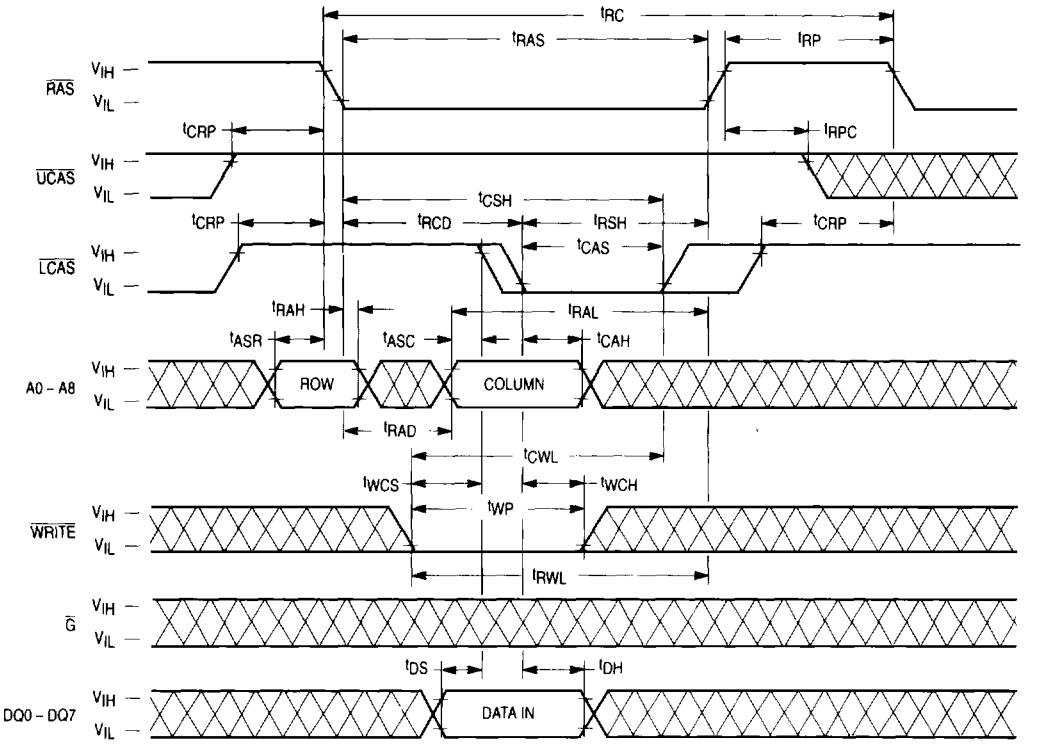
WRITE CYCLE (EARLY WRITE)



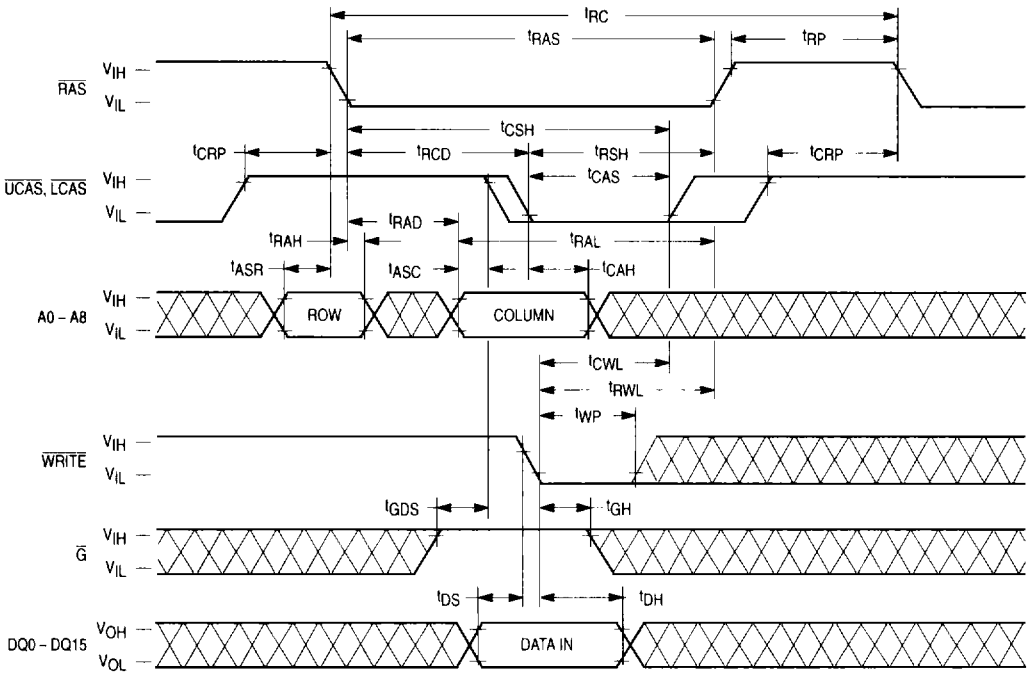
UPPER BYTE WRITE CYCLE (EARLY WRITE)



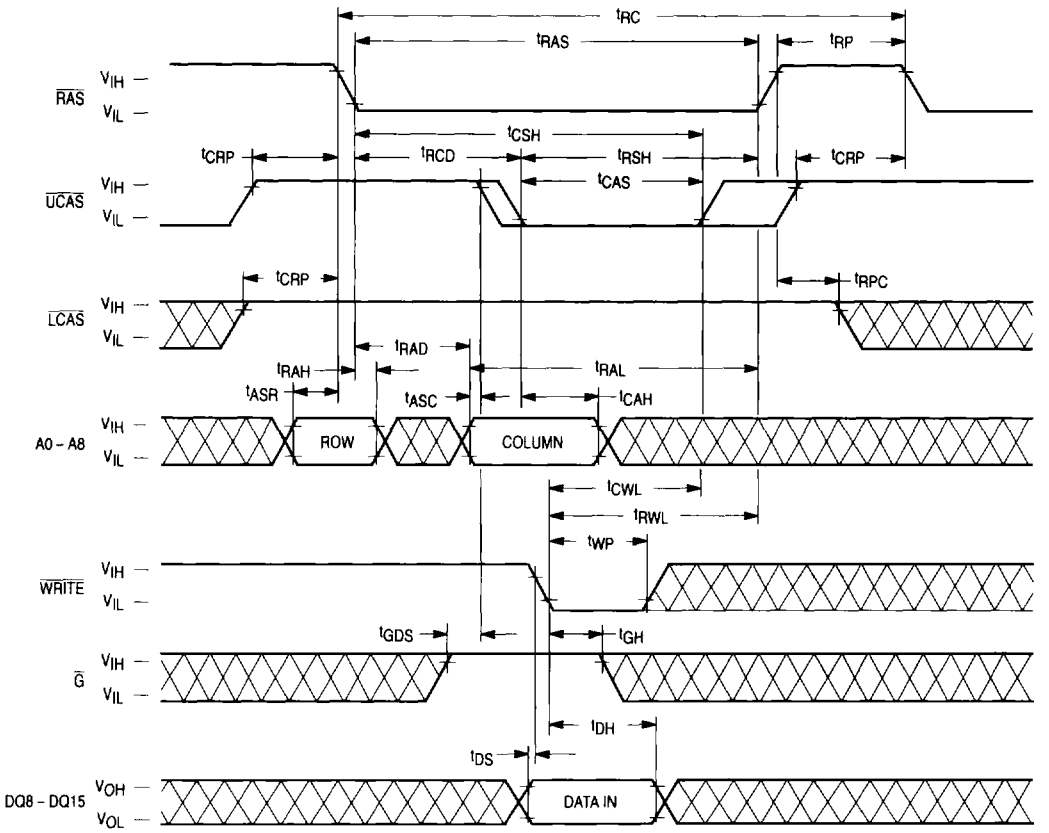
LOWER BYTE WRITE CYCLE (EARLY WRITE)



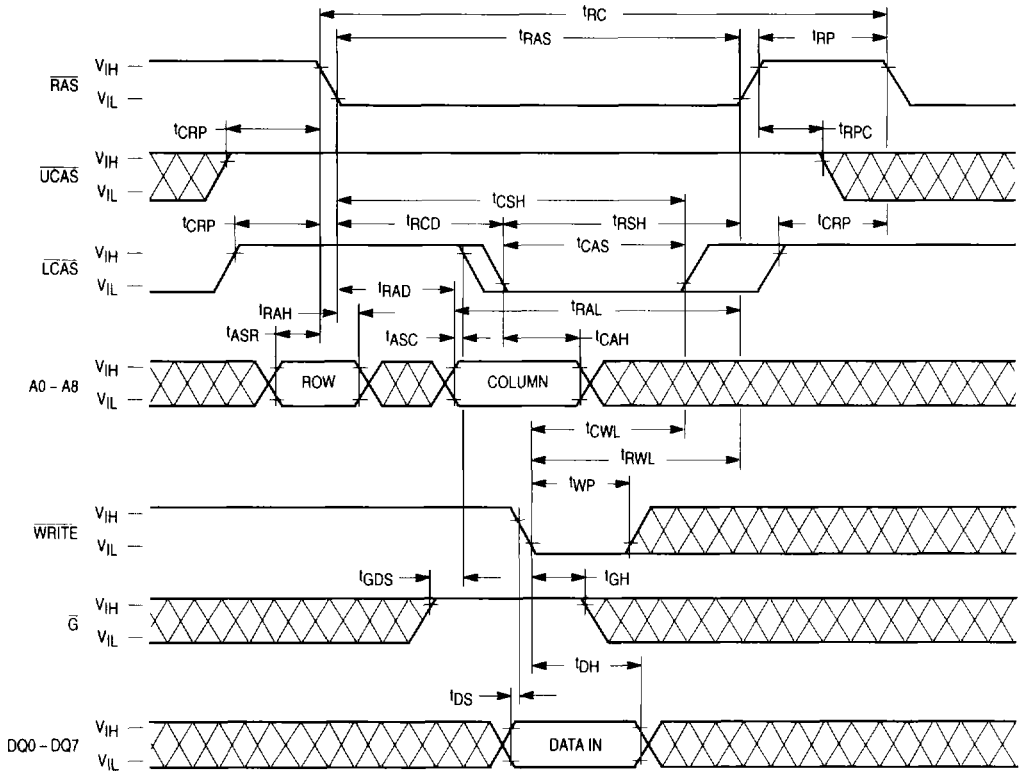
WRITE CYCLE ($\overline{G}$ CONTROLLED WRITE)



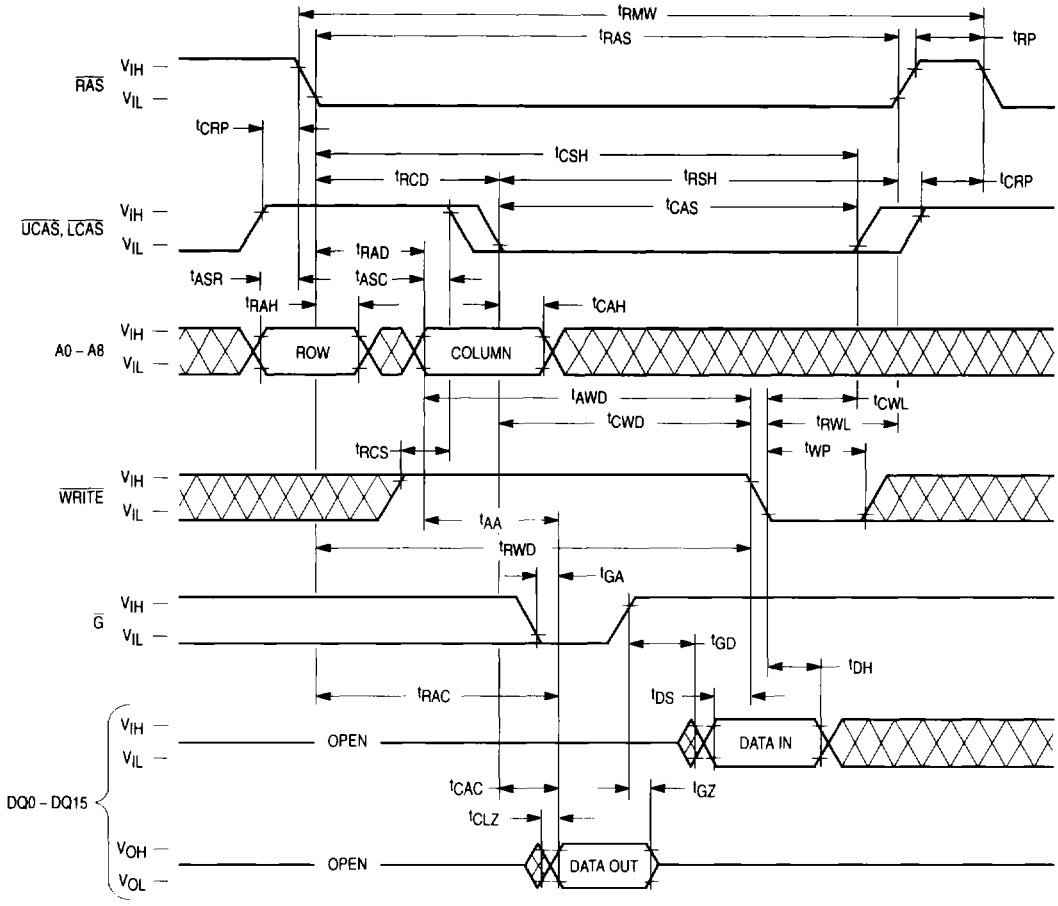
UPPER BYTE WRITE CYCLE ($\overline{G}$ CONTROLLED WRITE)



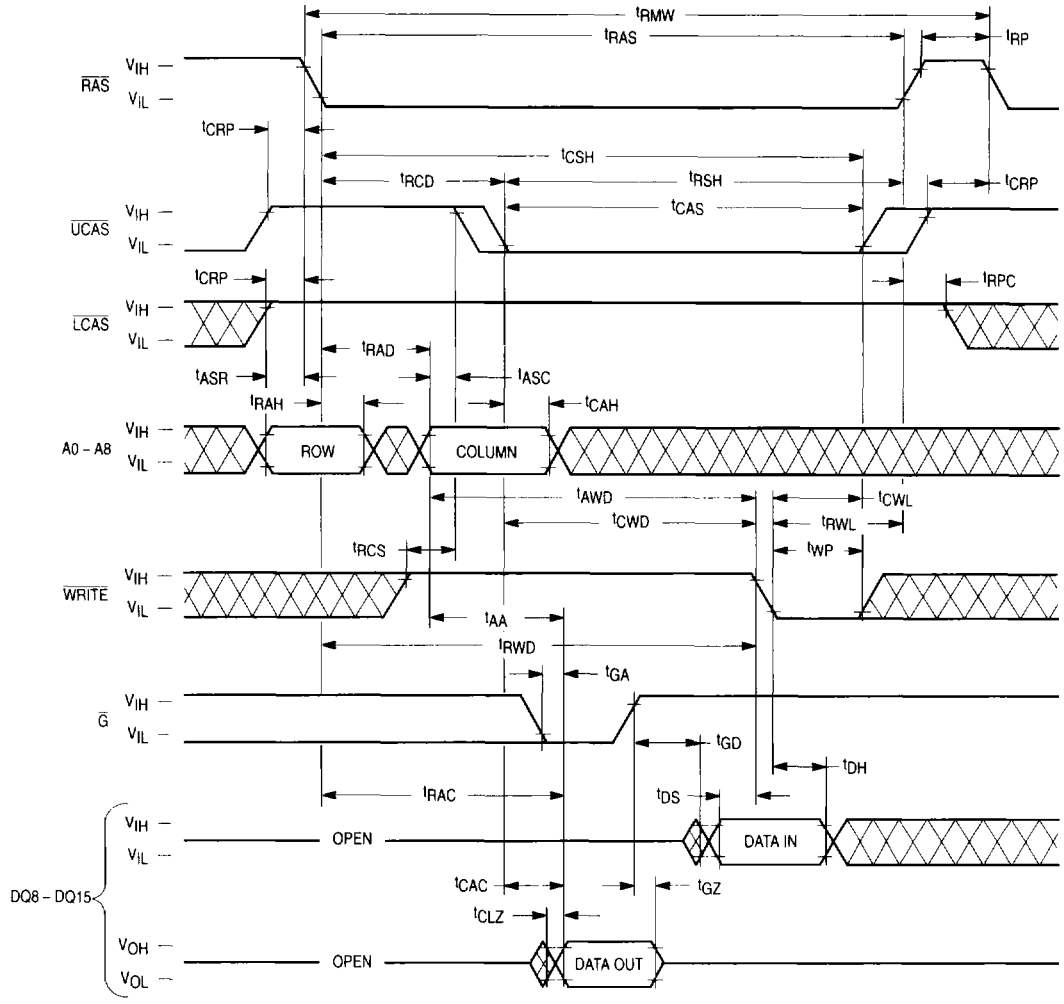
LOWER BYTE WRITE CYCLE ($\overline{G}$ CONTROLLED WRITE)



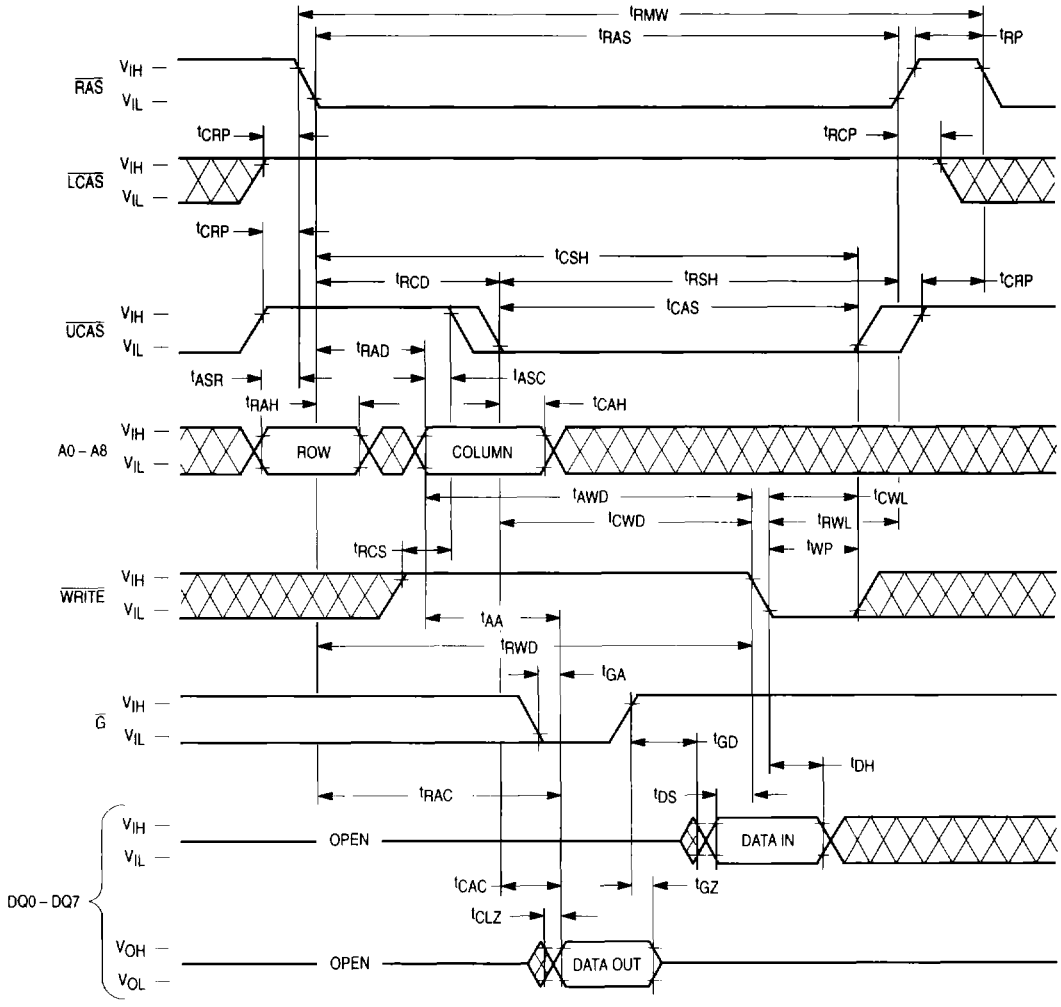
READ–MODIFY–WRITE CYCLE



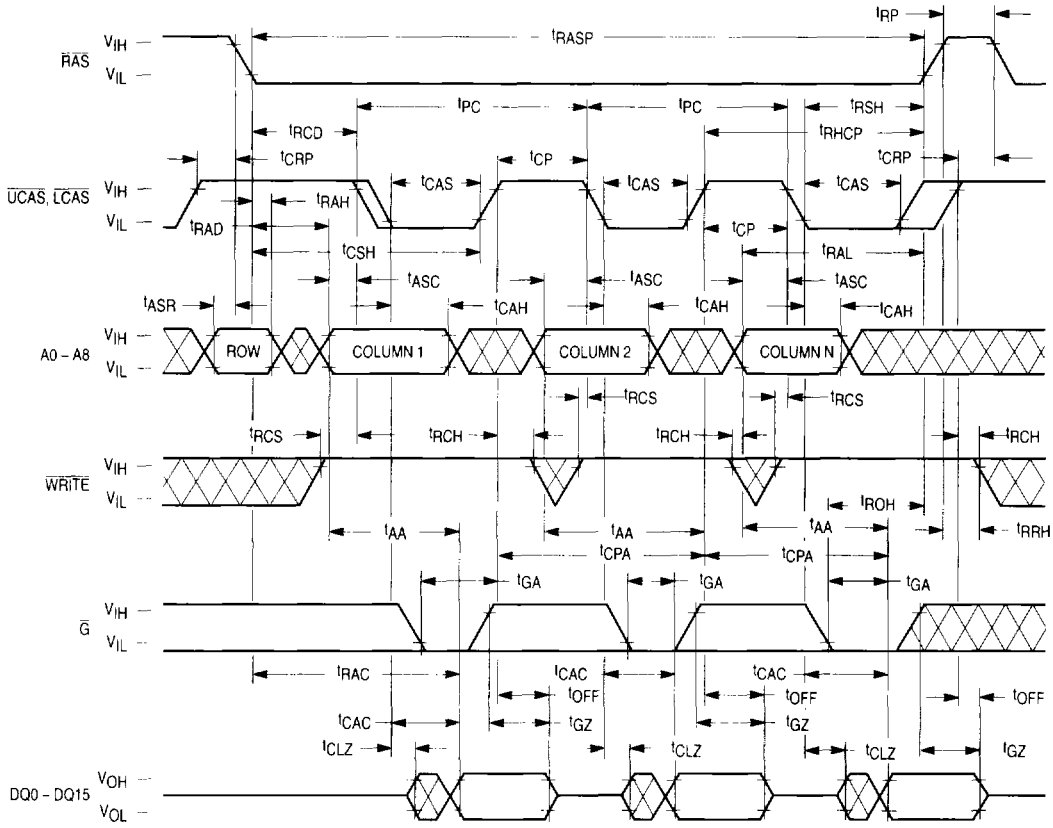
UPPER BYTE READ–MODIFY–WRITE CYCLE



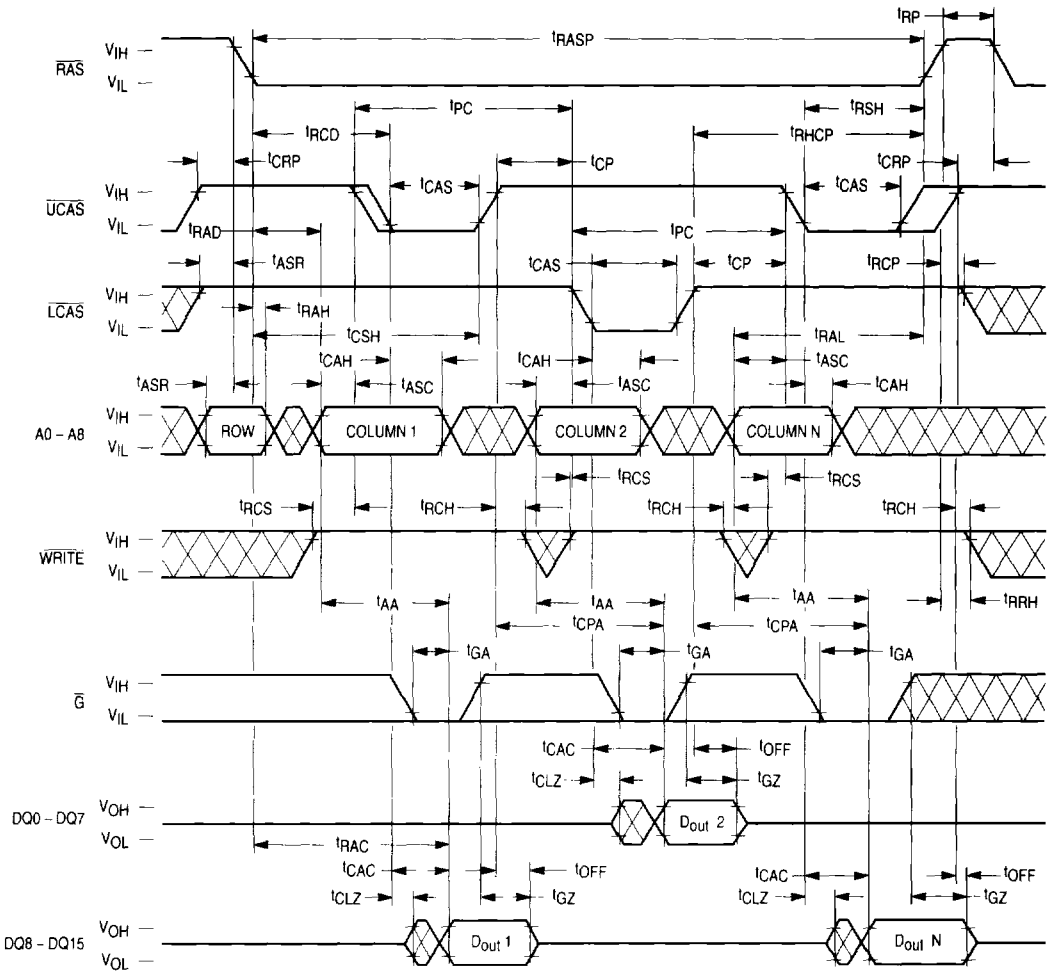
LOWER BYTE READ–MODIFY–WRITE CYCLE



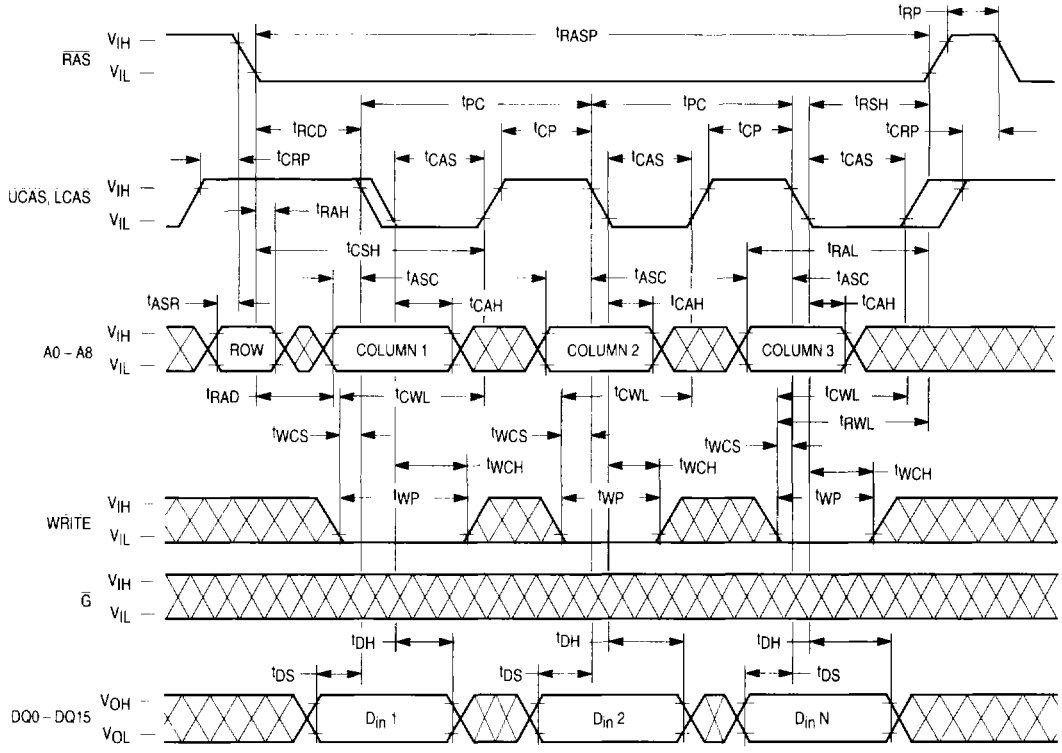
FAST PAGE MODE READ CYCLE



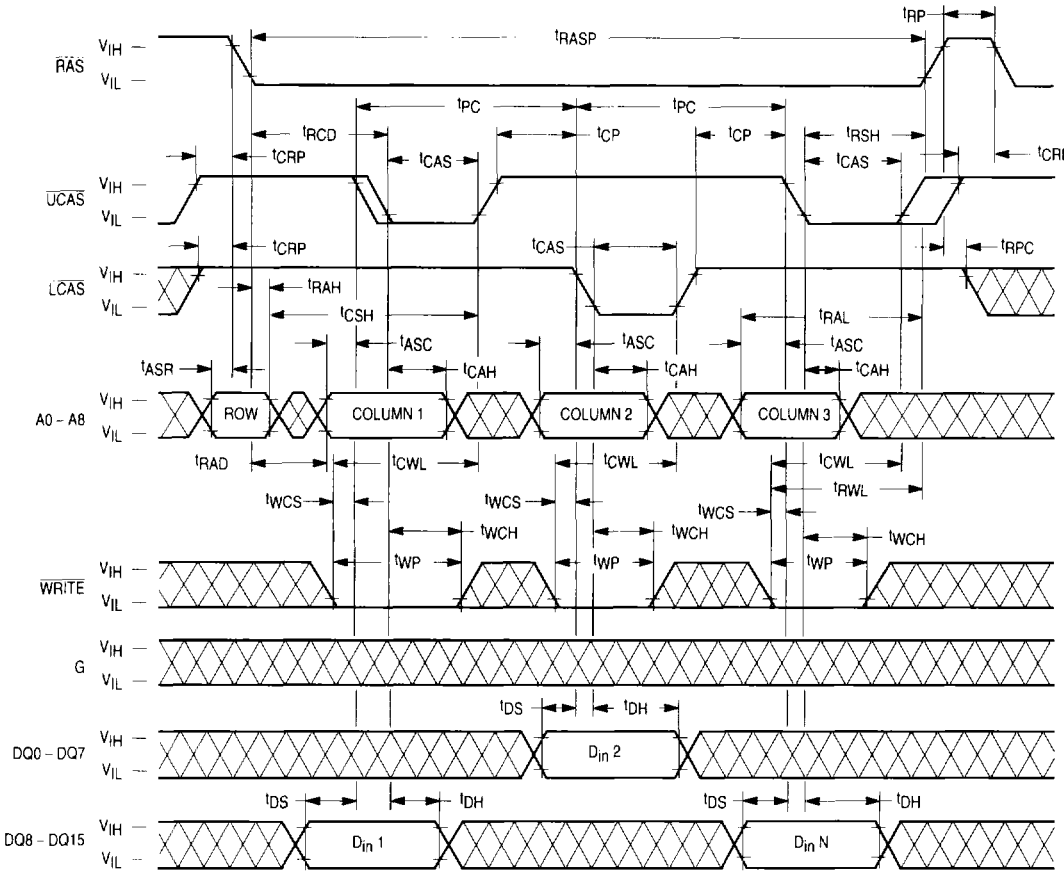
FAST PAGE MODE BYTE READ CYCLE



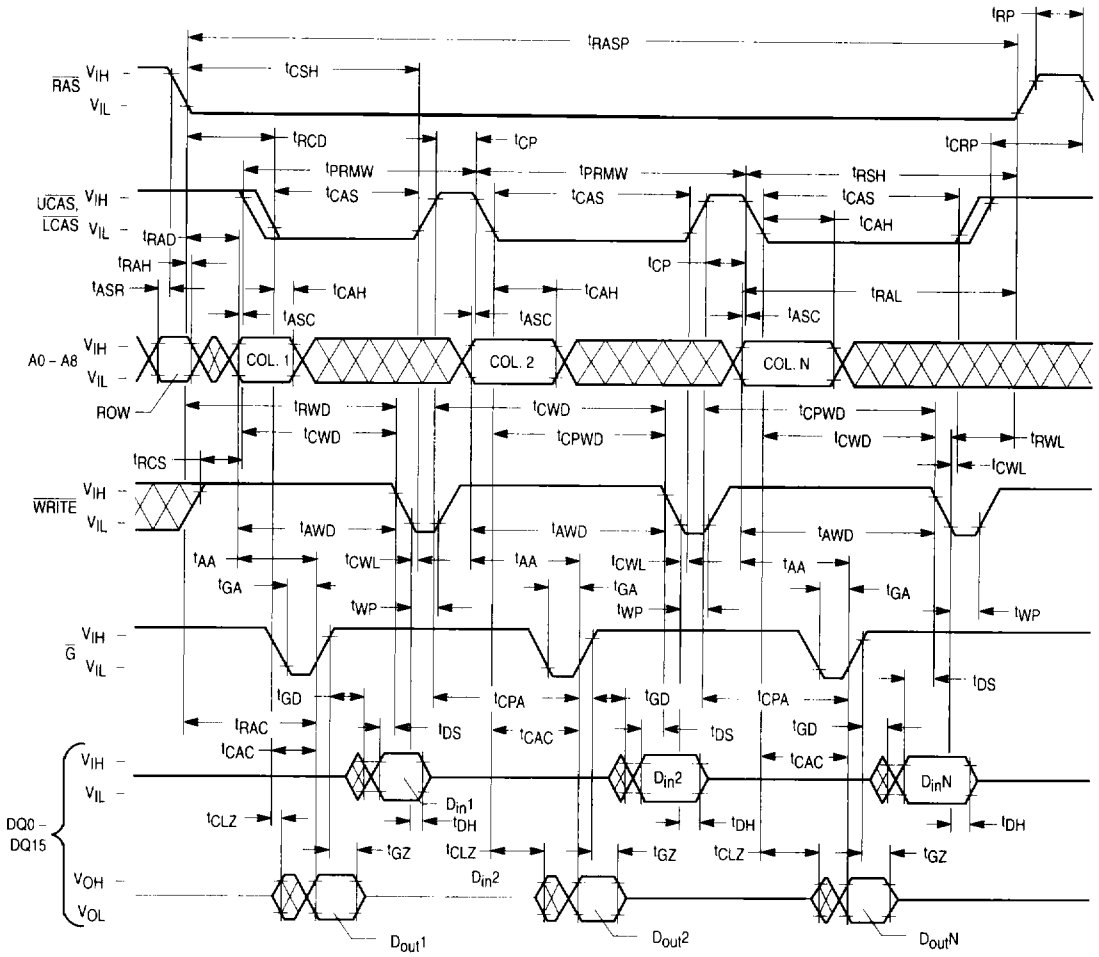
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



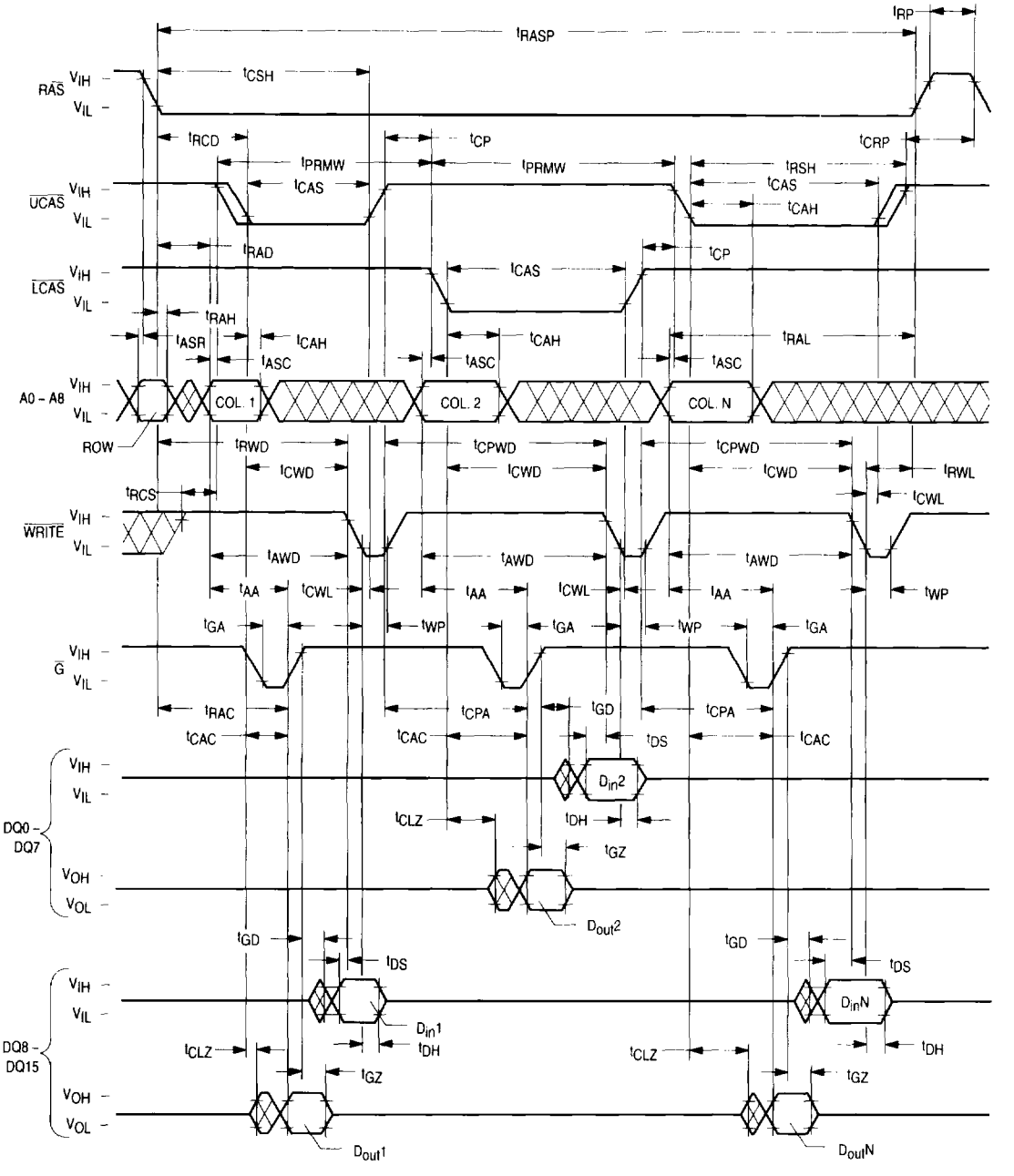
FAST PAGE MODE BYTE WRITE CYCLE (EARLY WRITE)



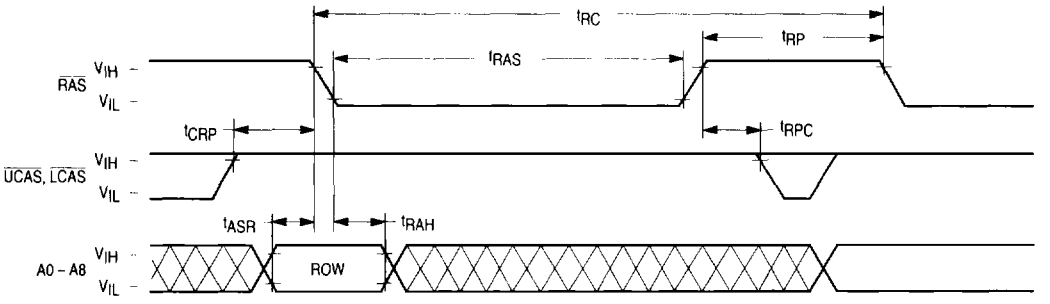
FAST PAGE MODE READ–MODIFY–WRITE CYCLE



FAST PAGE MODE BYTE READ–MODIFY–WRITE CYCLE

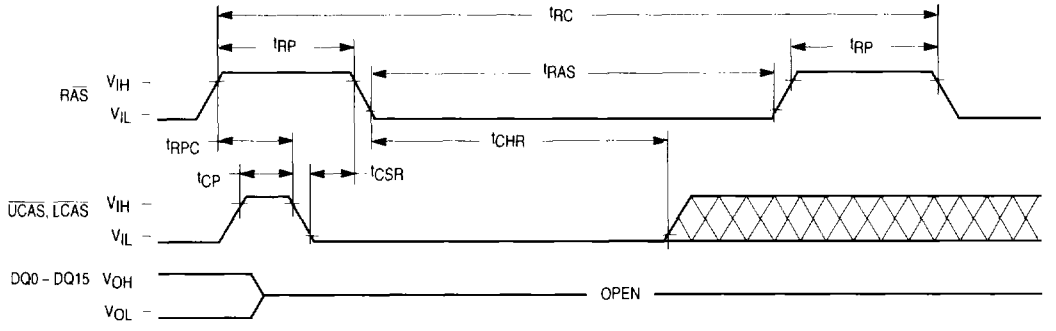


$\overline{RAS}$-ONLY REFRESH CYCLE



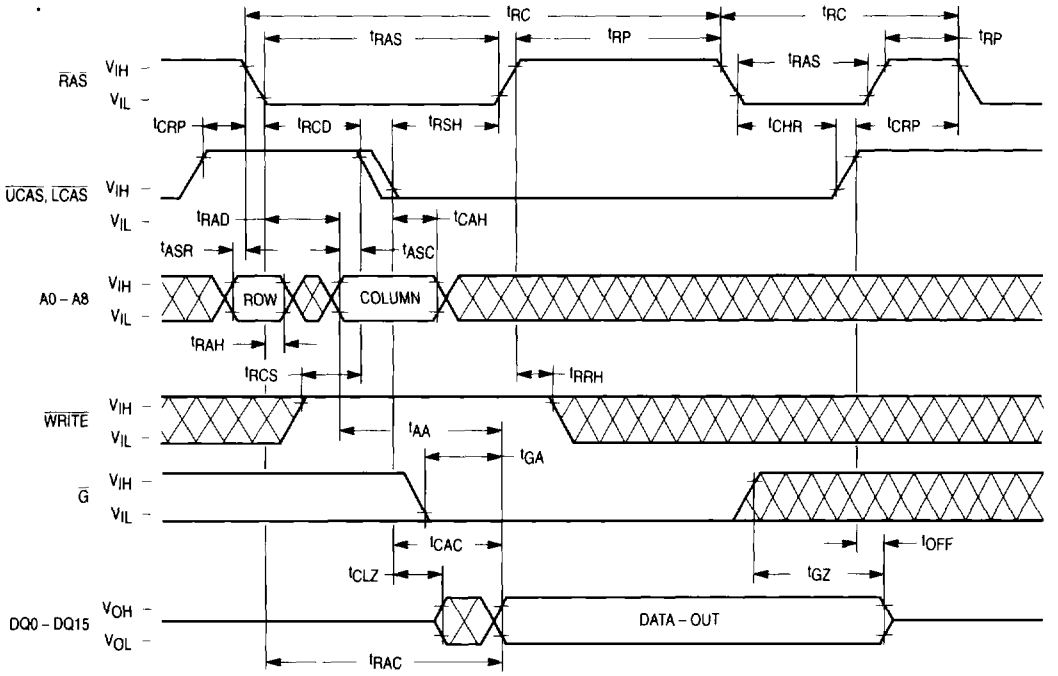
NOTE: $\overline{WRITE}$, $\overline{G}$ = "H" or "L"

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

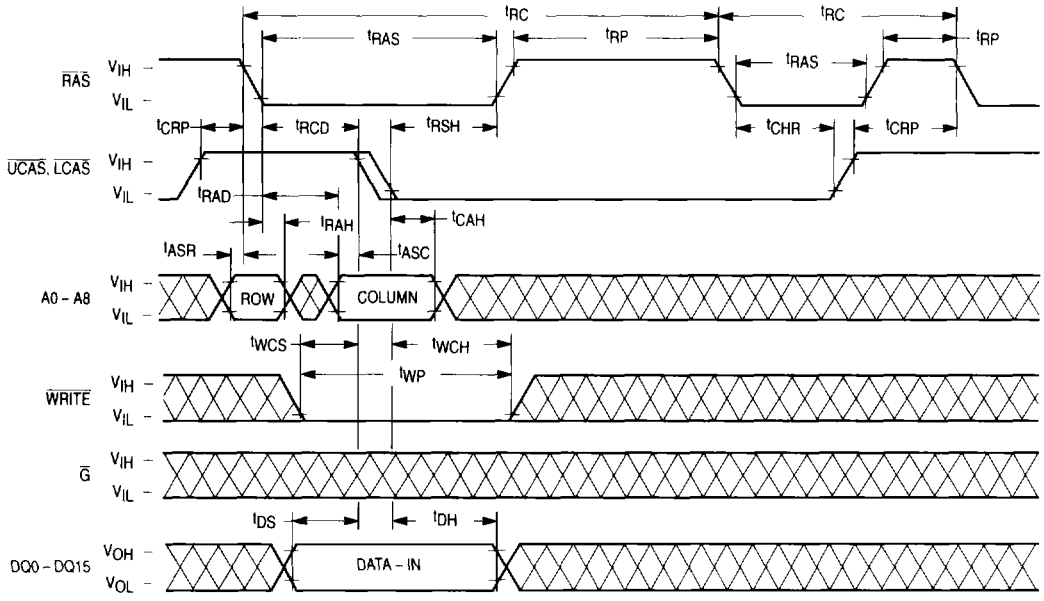


NOTE: $\overline{WRITE}$, $\overline{G}$, A0 – A8= "H" or "L"
$\overline{CAS}$ before RAS refresh is performed when either UCAS or LCAS meets this timing.

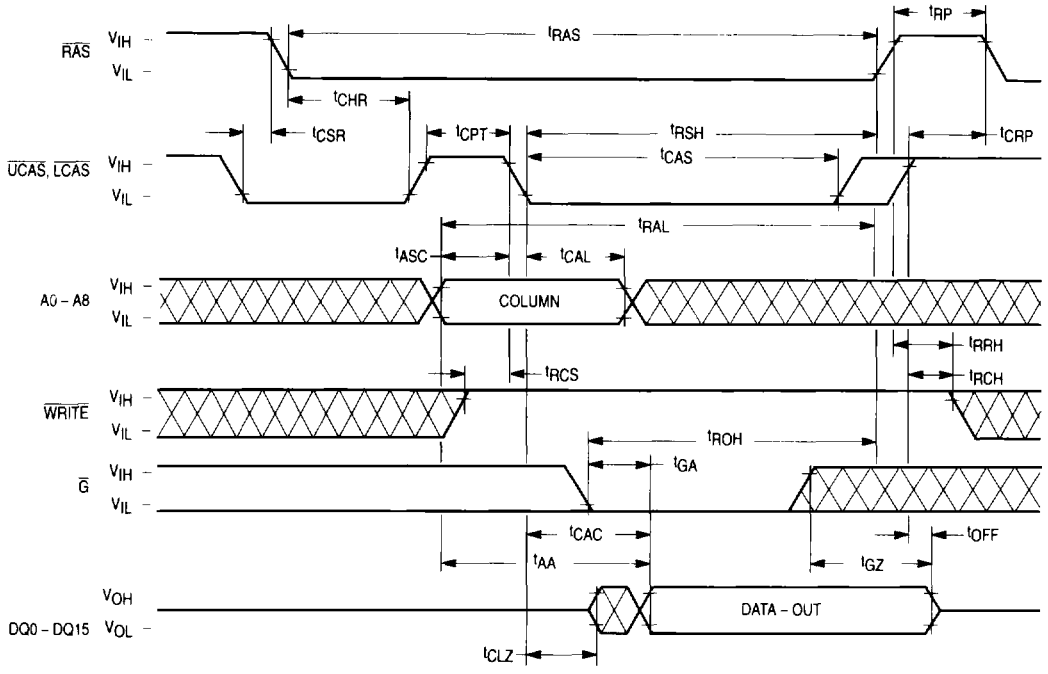
HIDDEN REFRESH CYCLE (READ)



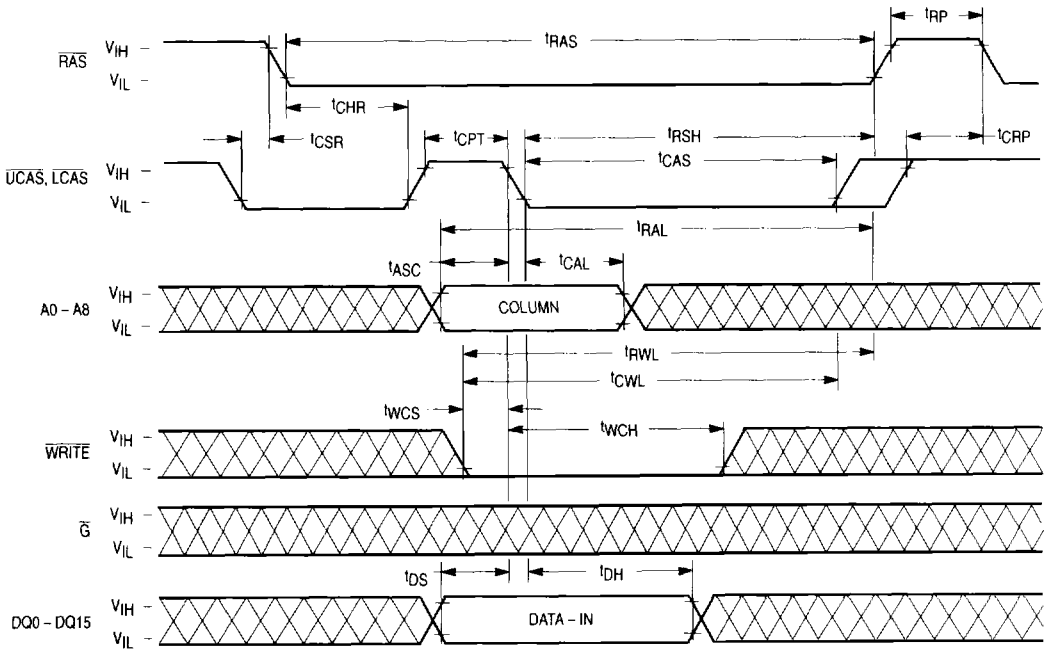
HIDDEN REFRESH CYCLE (WRITE)



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST READ CYCLE

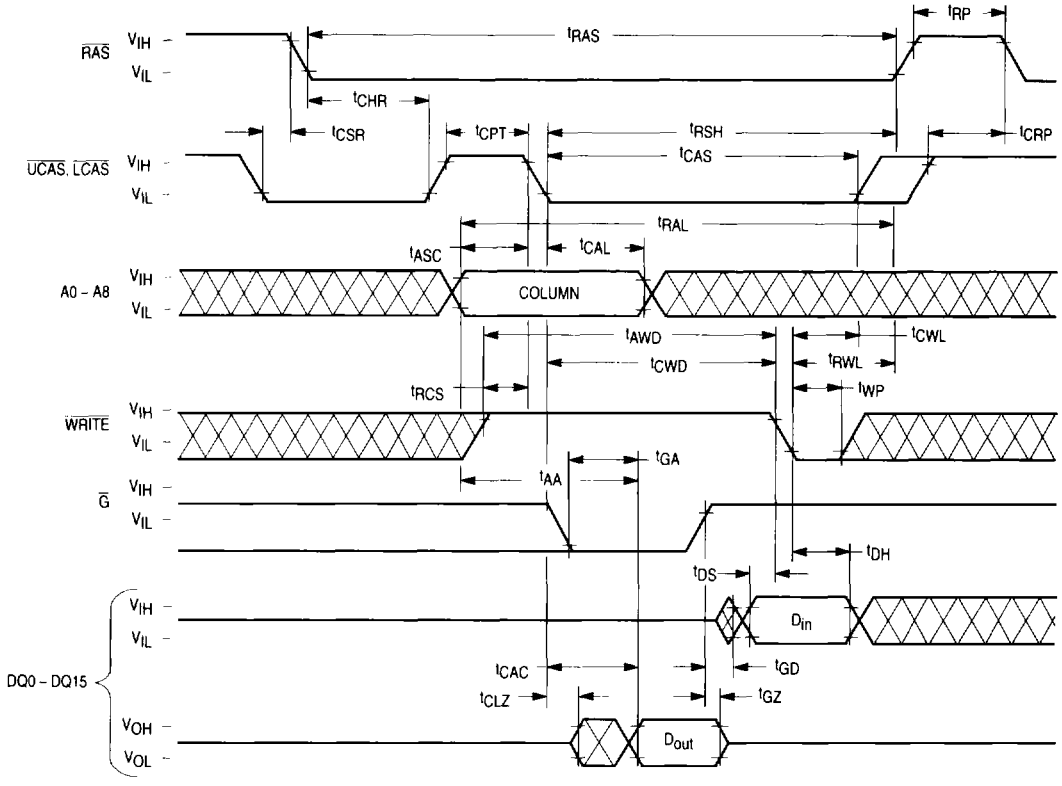


$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST WRITE CYCLE



2

CAS BEFORE RAS REFRESH COUNTER TEST READ–MODIFY–WRITE CYCLE



ORDERING INFORMATION
(Order by Full Part Number)

54260B
5L4260B

MCM	5S4260B	X	XX	XX

- MCM: Motorola Memory Prefix
- 5S4260B: Part Number
- X: Package (J = 400 mil SOJ, T = 400 mil TSOP)
- XX: Speed (70 = 70 ns, 80 = 80 ns, 10 = 100 ns)
- XX: Shipping Method (Blank = Rails or Tray, R = Tape and Reel)

Full Part Numbers —			
	MCM54260BJ70	MCM5L4260BJ70	MCM5S4260BJ70
	MCM54260BJ80	MCM5L4260BJ80	MCM5S4260BJ80
	MCM54260BJ10	MCM5L4260BJ100	MCM5S4260BJ10
	MCM54260BT70	MCM5L4260BT70	MCM5S4260BT70
	MCM54260BT80	MCM5L4260BT80	MCM5S4260BT80
	MCM54260BT10	MCM5L4260BT10	MCM5S4260BT10
	MCM54260BJ70R	MCM5L4260BJ70R	MCM5S4260BJ70R
	MCM54260BJ80R	MCM5L4260BJ80R	MCM5S4260BJ80R
	MCM54260BJ10R	MCM5L4260BJ10R	MCM5S4260BJ10R
	MCM54260BT70R	MCM5L4260BT70R	MCM5S4260BT70R
	MCM54260BT80R	MCM5L4260BT80R	MCM5S4260BT80R
	MCM54260BT10R	MCM5L4260BT10R	MCM5S4260BT10R