

# WIDE DRAM

# 2 MEG x 8 DRAM

5.0V FAST-PAGE-MODE (MT4C2M8B1/2)  
3.0/3.3V, FAST-PAGE-MODE (MT4LC2M8B1/2)

## FEATURES

- Industry-standard x8 pinouts, timing, functions and packages
- Address entry: 11 row-addresses, 10 column-addresses (32ms);
- 2,048-cycle refresh (4,096-cycle refresh available as MT4(L)C2M8A1/2)
- High-performance CMOS silicon-gate process
- Single +5V only or 3.0/3.3V only  $\pm 10\%$  power supply
- Low power, 5mW standby; 400mW active, typical (5V)
- All device pins are TTL-compatible
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- Optional FAST-PAGE-MODE access cycle
- NONPERSISTENT MASKED WRITE access cycle (MT4C2M8B2 only)

## OPTIONS

- Timing
  - 60ns access
  - 70ns access
  - 80ns access
- Power Supply
  - 5V  $\pm 10\%$  only
  - 3.0/3.3V  $\pm 10\%$  only
- MASKED WRITE
  - Not available
  - Available
- Packages
  - Plastic 28-pin SOJ (400 mil)
  - Plastic 28-pin TSOP (400 mil)
  - Plastic 32-pin SOJ (400 mil)
  - Plastic 32-pin TSOP (400 mil)
- Part Number Example: MT4C2M8B1DJ-6

## MARKING

-6  
-7  
-8

4C  
4LC

B1  
B2

DJ  
TG  
DL  
TL

## PART DESCRIPTION

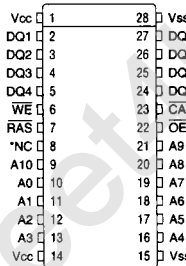
MT4C2M8B1	5.0V, NONMASKED WRITE
MT4C2M8B2	5.0V, MASKED WRITE
MT4LC2M8B1	3.0V/3.3V, NONMASKED WRITE
MT4LC2M8B2	3.0V/3.3V, MASKED WRITE

## GENERAL DESCRIPTION

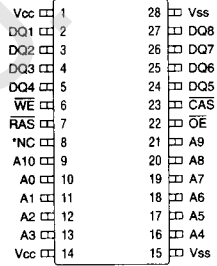
The MT4C2M8B1/2 and MT4LC2M8B1/2 are randomly accessed solid-state memories containing 16,777,216 bits organized in a x8 configuration. The MT4C2M8B1/2 and the MT4LC2M8B1/2 are the same DRAM versions except that the MT4LC2M8B1/2 are low voltage versions of the

### PIN ASSIGNMENT (Top View)

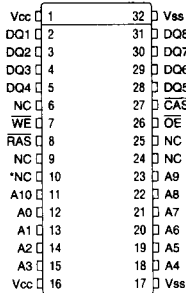
#### 28-Pin SOJ (DC-4)



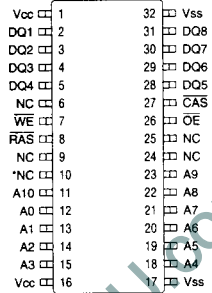
#### 28-Pin TSOP (DD-3)



#### 32-Pin SOJ (DC-5)



#### 32-Pin TSOP (DD-4)



\*A11 on 12 row-address version

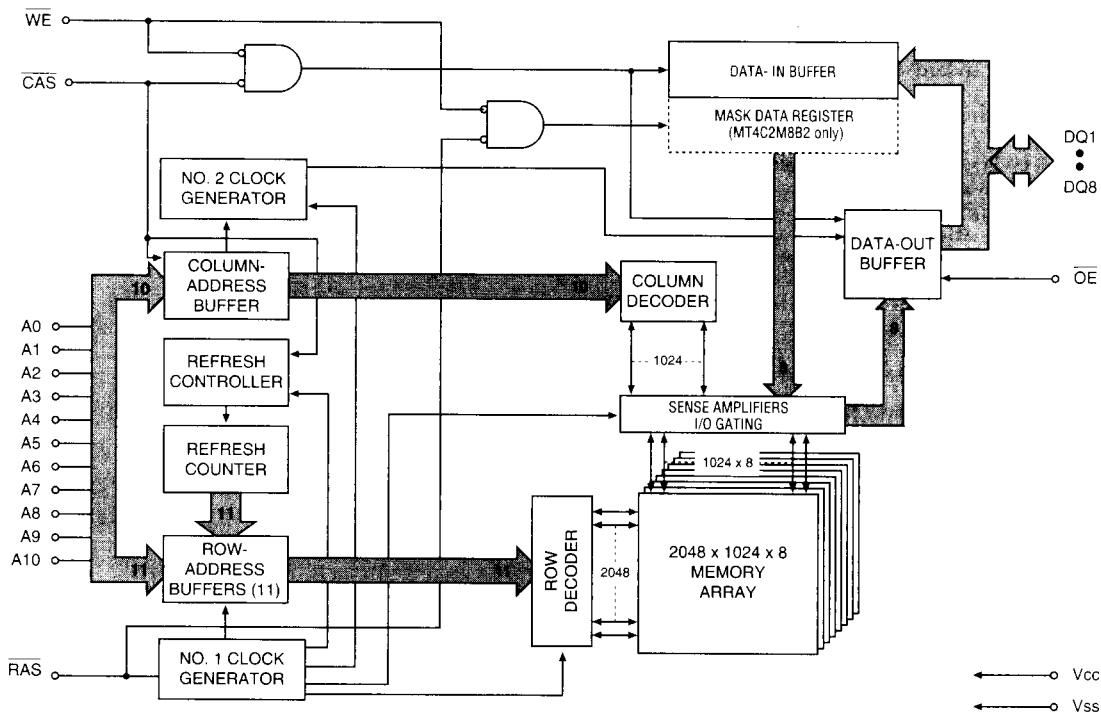
MT4C2M8B1/2. The MT4LC2M8B1/2 are designed to operate in either a 3.0V  $\pm 10\%$  or a 3.3V  $\pm 10\%$  memory system. All further references made to the MT4C2M8B1/2 also apply to the MT4LC2M8B1/2, unless specifically stated otherwise. Each byte is uniquely addressed through the 21 address bits during READ or WRITE cycles. The address is entered first by RAS latching 11 bits (A0-A10) and then CAS latching 10 bits (A0-A10).

The MT4C2M8B2 has NONPERSISTENT MASKED WRITE, allowing it to perform WRITE-PER-BIT accesses.

WIDE DRAM

**FUNCTIONAL BLOCK DIAGRAM**  
2048 ROWS

**WIDE DRAM**



**PIN DESCRIPTIONS**

28-PIN DEVICE PIN NUMBERS	32-PIN DEVICE PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
7	8	$\overline{\text{RAS}}$	Input	Row-Address Strobe: $\overline{\text{RAS}}$ is used to clock-in the 11 row-address bits and strobe the $\overline{\text{WE}}$ and DQs in the MASKED WRITE mode (MT4C2M8B2 only).
23	27	$\overline{\text{CAS}}$	Input	Column-Address Strobe: $\overline{\text{CAS}}$ is used to clock-in the 10 column-address bits, enable the DRAM output buffers and strobe the data inputs on WRITE cycles.
6	7	$\overline{\text{WE}}$	Input	Write Enable: $\overline{\text{WE}}$ is used to select a READ ( $\overline{\text{WE}}$ = HIGH) or WRITE ( $\overline{\text{WE}}$ = LOW) cycle. $\overline{\text{WE}}$ also serves as a mask enable ( $\overline{\text{WE}}$ = LOW) at the falling edge of $\overline{\text{RAS}}$ in a MASKED WRITE cycle (MT4C2M8B2).
22	26	$\overline{\text{OE}}$	Input	Output Enable: $\overline{\text{OE}}$ enables the output buffers when taken LOW during a READ access cycle. $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ must be LOW and $\overline{\text{WE}}$ must be HIGH before $\overline{\text{OE}}$ will control the output buffers. Otherwise, the output buffers are in a High-Z state.
10-13, 16-21, 9	12-15, 18-23, 11	A0-A10	Input	Address Inputs: These inputs are multiplexed and clocked by $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ to select one byte out of the 2 Meg available words.
2-5, 24-27	2-5, 28-31	DQ1-DQ8	Input	Data I/O: Includes inputs, outputs or High-Z and/or output masked data input (for MASKED WRITE cycle only).
8	6, 9, 24, 25, 10	NC	-	No Connect: These pins should be either left unconnected or tied to ground.
1, 14	1, 16	Vcc	Supply	Power Supply: +5V $\pm$ 10% (C), 2.7V to 3.6V (LC)
15, 28	17, 32	Vss	Supply	Ground



## FUNCTIONAL DESCRIPTION

Each bit is uniquely addressed through the 21 address bits during READ or WRITE cycles. First,  $\overline{RAS}$  is used to latch 11 bits (A0-A10) then,  $\overline{CAS}$  latches 10 bits (A0-A9).

The  $\overline{CAS}$  control also determines whether the cycle will be a refresh cycle ( $\overline{RAS}$ -ONLY) or an active cycle (READ, WRITE or READ-WRITE) once  $\overline{RAS}$  goes LOW.

READ or WRITE cycles are selected by  $\overline{WE}$ . A logic HIGH on  $\overline{WE}$  dictates READ mode while a logic LOW on  $\overline{WE}$  dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of  $\overline{WE}$  or  $\overline{CAS}$ , whichever occurs first. Taking  $\overline{WE}$  LOW will initiate a WRITE cycle, selecting DQ1 through DQ8. If  $\overline{WE}$  goes LOW prior to  $\overline{CAS}$  going LOW, the output pin(s) remain open (High-Z) until the next  $\overline{CAS}$  cycle. If  $\overline{WE}$  goes LOW after  $\overline{CAS}$  goes LOW and data reaches the output pins, data-out (Q) is activated and retains the selected cell data as long as  $\overline{CAS}$  and  $\overline{OE}$  remain LOW (regardless of  $\overline{WE}$  or  $\overline{RAS}$ ). This late  $\overline{WE}$  pulse results in a READ-WRITE cycle.

The eight data inputs and eight data outputs are routed through eight pins using common I/O and pin direction is controlled by  $\overline{OE}$  and  $\overline{WE}$ .

FAST-PAGE-MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row-address-defined (A0-A11) page boundary. The FAST-PAGE-MODE cycle is always initiated with a row-address strobed-in by  $\overline{RAS}$  followed by a column-address strobed-in by  $\overline{CAS}$ .  $\overline{CAS}$  may be toggled-in by holding  $\overline{RAS}$  LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning  $\overline{RAS}$  HIGH terminates the FAST-PAGE-MODE operation.

Returning  $\overline{RAS}$  and  $\overline{CAS}$  HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is also preconditioned for the next cycle during the  $\overline{RAS}$  HIGH time. Memory cell data is retained in its correct

state by maintaining power and executing any  $\overline{RAS}$  cycle (READ, WRITE) or  $\overline{RAS}$  REFRESH cycle ( $\overline{RAS}$ -ONLY, CBR, or HIDDEN) so that all 2,048 combinations of  $\overline{RAS}$  addresses (A0-A10) are executed at least every 32ms, regardless of sequence. The CBR REFRESH cycle will also invoke the refresh counter and controller for row-address control.

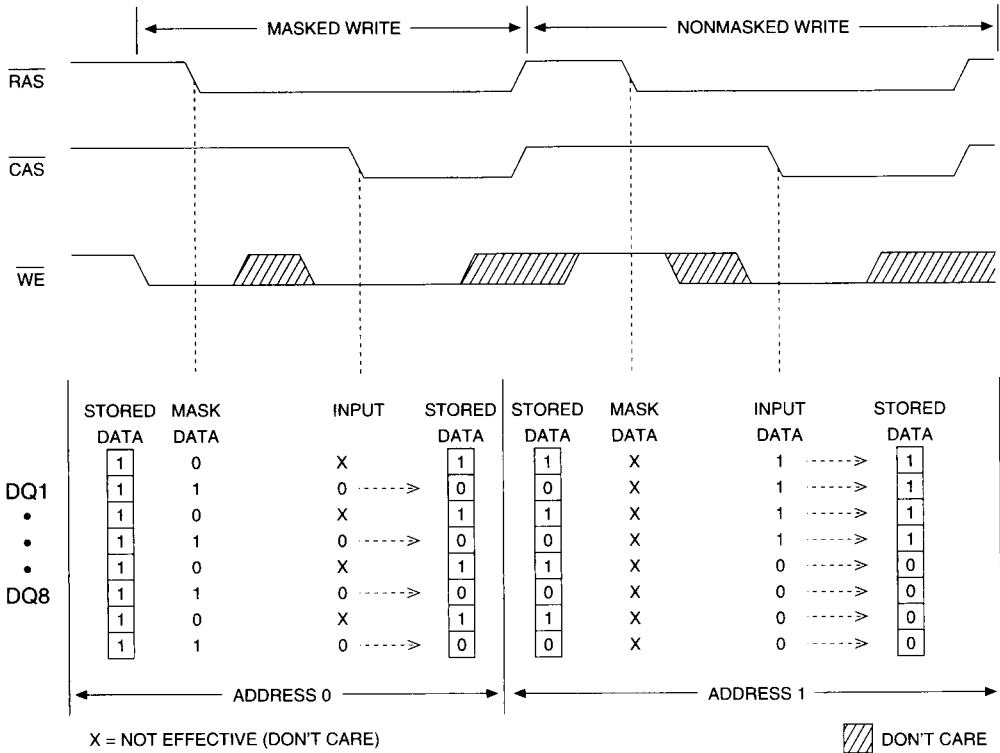
## MASKED WRITE ACCESS CYCLE (MT4C2M8B2 ONLY)

Every WRITE access cycle can be a MASKED WRITE, depending on the state of  $\overline{WE}$  at  $\overline{RAS}$  time. A MASKED WRITE is selected when  $\overline{WE}$  is LOW at  $\overline{RAS}$  time and mask data is supplied on the DQ pins.

The mask data present on the DQ1-DQ8 inputs at  $\overline{RAS}$  time will be written to an internal mask data register and will then act as an individual write enable for each of the corresponding DQ inputs. If a LOW (logic "0") is written to a mask data register bit, the input port for that bit is disabled during the subsequent WRITE operation and no new data will be written to that DRAM cell location. A HIGH (logic "1") on a mask data register bit enables the input port and allows normal WRITE operations to proceed. At  $\overline{CAS}$  time, the bits present on the DQ1-DQ8 inputs will be written to the DRAM (if the mask data bit was HIGH) or ignored (if the mask data bit was LOW).

In NONPERSISTENT MASKED WRITES, new mask data must be supplied each time a MASKED WRITE cycle is initiated.

Figure 1 illustrates the MT4C2M8B2 MASKED WRITE operation (Note:  $\overline{RAS}$  or  $\overline{CAS}$  time refers to the time at which  $\overline{RAS}$  or  $\overline{CAS}$  transition from HIGH to LOW).



**Figure 1**  
**MT4C2M8B2 MASKED WRITE EXAMPLE**

**TRUTH TABLE**

FUNCTION		RAS	CAS	WE	OE	ADDRESSES		DQs	NOTES
						r	c		
Standby		H	H→X	X	X	X	X	High-Z	
READ		L	L	H	L	ROW	COL	Data-Out	
EARLY-WRITE		L	L	L	X	ROW	COL	Data-In	1
READ-WRITE		L	L	H→L	L→H	ROW	COL	Data-Out, Data-In	1
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	L	ROW	COL	Data-Out	
	2nd Cycle	L	H→L	H	L	n/a	COL	Data-Out	
FAST-PAGE-MODE WRITE	1st Cycle	L	H→L	L	X	ROW	COL	Data-In	1
	2nd Cycle	L	H→L	L	X	n/a	COL	Data-In	1
FAST-PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data-Out, Data-In	1
	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data-Out, Data-In	1
HIDDEN REFRESH	READ	L→H→L	L	H	L	ROW	COL	Data-Out	
	WRITE	L→H→L	L	L	X	ROW	COL	Data-In	1, 2
RAS-ONLY REFRESH		L	H	X	X	ROW	n/a	High-Z	
CBR REFRESH		H→L	L	H	X	X	X	High-Z	

**NOTE:** 1. Data-in will be dependent on the mask provided (MT4C2M8B2 only). Refer to Figure 1.  
 2. EARLY WRITE only.

**WIDE DRAM**

**ABSOLUTE MAXIMUM RATINGS\***

Voltage on V <sub>CC</sub> supply relative to V <sub>SS</sub> (5V) .....	-1V to +7V
Voltage on V <sub>CC</sub> supply relative to V <sub>SS</sub> (3V) ....	-1V to +4.6V
Operating Temperature, T <sub>A</sub> (ambient) .....	0°C to +70°C
Storage Temperature (plastic) .....	-55°C to +150°C
Power Dissipation .....	1W
Short Circuit Output Current .....	50mA

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**DC OPERATING SPECIFICATIONS FOR 5V VERSION**

(Notes: 1, 3, 4, 6, 7, 30) (0°C ≤ T<sub>A</sub> ≤ 70°C; V<sub>CC</sub> = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V <sub>CC</sub>	4.5	5.5	V	1, 30
Input High (Logic 1) Voltage, all inputs	V <sub>IH</sub>	2.4	V <sub>CC</sub> +1	V	1
Input Low (Logic 0) Voltage, all inputs	V <sub>IL</sub>	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any input 0V ≤ V <sub>IN</sub> ≤ V <sub>CC</sub> (All other pins not under test = 0V)	I <sub>I</sub>	-2	2	μA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V <sub>OUT</sub> ≤ 5.5V)	I <sub>OZ</sub>	-10	10	μA	
OUTPUT LEVELS	V <sub>OH</sub>	2.4		V	
Output High Voltage (I <sub>OUT</sub> = -2.5mA)					
Output Low Voltage (I <sub>OUT</sub> = 2.1mA)	V <sub>OL</sub>		0.4	V	

**DC OPERATING SPECIFICATIONS FOR 3.0/3.3V VERSION**

(Notes: 1, 3, 4, 6, 7, 31) (0°C ≤ T<sub>A</sub> ≤ 70°C; V<sub>CC</sub> = 2.7V to 3.6V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V <sub>CC</sub>	2.7	3.6	V	1, 31
Input High (Logic 1) Voltage, all inputs	V <sub>IH</sub>	2.0	V <sub>CC</sub> +1	V	1
Input Low (Logic 0) Voltage, all inputs	V <sub>IL</sub>	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any input 0V ≤ V <sub>IN</sub> ≤ V <sub>CC</sub> (All other pins not under test = 0V)	I <sub>I</sub>	-2	2	μA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V <sub>OUT</sub> ≤ 3.6V)	I <sub>OZ</sub>	-10	10	μA	
OUTPUT LEVELS	V <sub>OH</sub>	2.4		V	
Output High Voltage (I <sub>OUT</sub> = -2mA)					
Output Low Voltage (I <sub>OUT</sub> = 2mA)	V <sub>OL</sub>		0.4	V	

**WIDE DRAM**



MT4(L)C2M8B1/2  
2 MEG x 8 WIDE DRAM

WIDE DRAM

**DC OPERATING SPECIFICATIONS FOR 5V VERSION**

(Notes: 1, 3, 4, 6, 7, 30) ( $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$ ;  $V_{CC} = 5\text{V} \pm 10\%$ )

PARAMETER/CONDITION	SYMBOL	MAX			UNITS	NOTES
		-6	-7	-8		
STANDBY CURRENT: TTL ( $\overline{\text{RAS}} = \overline{\text{CAS}} = V_{IH}$ )	Icc1	2	2	2	mA	
STANDBY CURRENT: CMOS ( $\overline{\text{RAS}} = \overline{\text{CAS}} = V_{CC} - 0.2\text{V}$ )	Icc2	1	1	1	mA	25
OPERATING CURRENT: Random READ/WRITE Average power supply current ( $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , Address Cycling: $t'RC = t'RC$ [MIN])	Icc3	140	130	120	mA	3, 4, 32
OPERATING CURRENT: FAST-PAGE-MODE Average power supply current ( $\text{RAS} = V_{IL}$ , $\overline{\text{CAS}}$ , Address Cycling: $t'PC = t'PC$ [MIN]; $t'CP$ , $t'ASC = 10\text{ns}$ )	Icc4	100	90	80	mA	3, 4, 32
REFRESH CURRENT: $\overline{\text{RAS}}$ -ONLY Average power supply current ( $\overline{\text{RAS}}$ Cycling, $\overline{\text{CAS}} = V_{IH}$ : $t'RC = t'RC$ [MIN])	Icc5	140	130	120	mA	3, 32
REFRESH CURRENT: CBR Average power supply current ( $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , Address Cycling: $t'RC = t'RC$ [MIN])	Icc6	140	130	120	mA	3

**DC OPERATING SPECIFICATIONS FOR 3.0/3.3V VERSION**

(Notes: 1, 3, 4, 6, 7, 31) ( $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$ ;  $V_{CC} = 2.7\text{V}$  to  $3.6\text{V}$ )

PARAMETER/CONDITION	SYMBOL	MAX			UNITS	NOTES
		-6	-7	-8		
STANDBY CURRENT: TTL ( $\overline{\text{RAS}} = \overline{\text{CAS}} = V_{IH}$ )	Icc1	2	2	2	mA	
STANDBY CURRENT: CMOS ( $\overline{\text{RAS}} = \overline{\text{CAS}} = V_{CC} - 0.2\text{V}$ )	Icc2	1	1	1	$\mu\text{A}$	25
OPERATING CURRENT: Random READ/WRITE Average power supply current ( $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , Address Cycling: $t'RC = t'RC$ [MIN])	Icc3	140	130	120	mA	3, 4, 32
OPERATING CURRENT: FAST-PAGE-MODE Average power supply current ( $\text{RAS} = V_{IL}$ , $\overline{\text{CAS}}$ , Address Cycling: $t'PC = t'PC$ [MIN]; $t'CP$ , $t'ASC = 10\text{ns}$ )	Icc4	100	90	80	mA	3, 4, 32
REFRESH CURRENT: $\overline{\text{RAS}}$ -ONLY Average power supply current ( $\overline{\text{RAS}}$ Cycling, $\overline{\text{CAS}} = V_{IH}$ : $t'RC = t'RC$ [MIN])	Icc5	140	130	120	mA	3, 32
REFRESH CURRENT: CBR Average power supply current ( $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , Address Cycling: $t'RC = t'RC$ [MIN])	Icc6	140	130	120	mA	3



## CAPACITANCE

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A10	C <sub>i1</sub>	5	pF	2
Input Capacitance: $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , $\overline{\text{WE}}$ , $\overline{\text{OE}}$	C <sub>i2</sub>	7	pF	2
Input/Output Capacitance: DQ	C <sub>i0</sub>	7	pF	2

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ( $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ )

AC CHARACTERISTICS	SYM	-6		-7		-8		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
Random READ or WRITE cycle time	<sup>t</sup> RC	110		130		150		ns	
READ-WRITE cycle time	<sup>t</sup> RWC	155		180		200		ns	
FAST-PAGE-MODE READ or WRITE cycle time	<sup>t</sup> PC	35		40		45		ns	
FAST-PAGE-MODE READ-WRITE cycle time	<sup>t</sup> PRWC	85		95		100		ns	
Access time from $\overline{\text{RAS}}$	<sup>t</sup> RAC		60		70		80	ns	14
Access time from $\overline{\text{CAS}}$	<sup>t</sup> CAC		15		20		20	ns	15
Output Enable	<sup>t</sup> OE		15		15		15	ns	
Access time from column-address	<sup>t</sup> AA		30		35		40	ns	
Access time from $\overline{\text{CAS}}$ precharge	<sup>t</sup> CPA		35		40		45	ns	
$\overline{\text{RAS}}$ pulse width	<sup>t</sup> RAS	60	100,000	70	100,000	80	100,000	ns	
$\overline{\text{RAS}}$ pulse width (FAST-PAGE-MODE)	<sup>t</sup> RASP	60	100,000	70	100,000	80	100,000	ns	
$\overline{\text{RAS}}$ hold time	<sup>t</sup> RSH	15		20		20		ns	
$\overline{\text{RAS}}$ precharge time	<sup>t</sup> RP	40		50		60		ns	
$\overline{\text{CAS}}$ pulse width	<sup>t</sup> CAS	15	100,000	20	100,000	20	100,000	ns	
$\overline{\text{CAS}}$ hold time	<sup>t</sup> CSH	60		70		80		ns	
$\overline{\text{CAS}}$ precharge time	<sup>t</sup> CPN	10		10		10		ns	16
$\overline{\text{CAS}}$ precharge time (FAST-PAGE-MODE)	<sup>t</sup> CP	10		10		10		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	<sup>t</sup> RCD	15	45	20	50	20	60	ns	17
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	<sup>t</sup> CRP	5		5		5		ns	
Row-address setup time	<sup>t</sup> ASR	0		0		0		ns	
Row-address hold time	<sup>t</sup> RAH	10		10		10		ns	
$\overline{\text{RAS}}$ to column- address delay time	<sup>t</sup> RAD	15	30	15	35	15	40	ns	18
Column-address setup time	<sup>t</sup> ASC	0		0		0		ns	
Column-address hold time	<sup>t</sup> CAH	10		15		15		ns	
Column-address hold time (referenced to $\overline{\text{RAS}}$ )	<sup>t</sup> AR	50		55		60		ns	
Column-address to $\overline{\text{RAS}}$ lead time	<sup>t</sup> RAL	30		35		40		ns	
Read command setup time	<sup>t</sup> RCS	0		0		0		ns	26
Read command hold time (referenced to $\overline{\text{CAS}}$ )	<sup>t</sup> RCH	0		0		0		ns	19, 26
Read command hold time (referenced to $\overline{\text{RAS}}$ )	<sup>t</sup> RRH	0		0		0		ns	19
$\overline{\text{CAS}}$ to output in Low-Z	<sup>t</sup> CLZ	3		3		3		ns	33
Output buffer turn-off delay	<sup>t</sup> OFF	3	15	3	20	3	20	ns	20, 29, 33

**WIDE DRAM**

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS**

 (Notes: 6, 7, 8, 9, 10, 11, 12, 13) ( $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ )

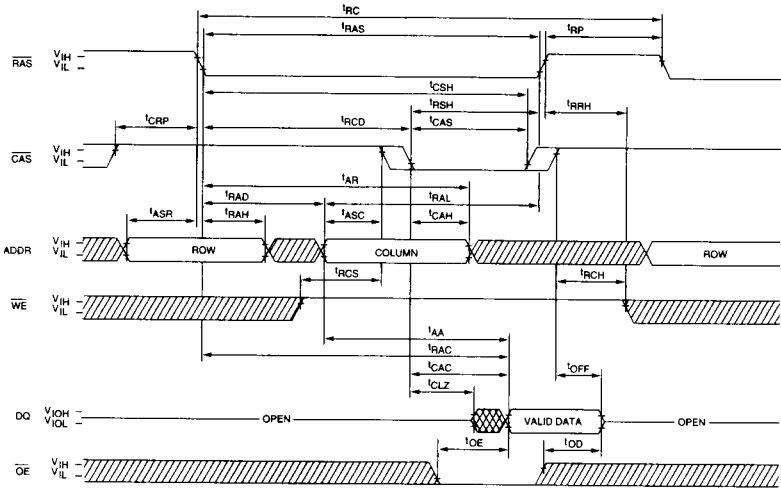
AC CHARACTERISTICS		-6		-7		-8		UNITS	NOTES
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX		
WE command setup time	t <sub>WCS</sub>	0		0		0		ns	21, 29
Write command hold time	t <sub>WCH</sub>	10		15		15		ns	26
Write command hold time (referenced to RAS)	t <sub>WCR</sub>	45		55		60		ns	26
Write command pulse width	t <sub>WP</sub>	10		15		15		ns	26
Write command to RAS lead time	t <sub>RWL</sub>	15		20		20		ns	26
Write command to CAS lead time	t <sub>CWL</sub>	15		20		20		ns	26
Data-in setup time	t <sub>DS</sub>	0		0		0		ns	22
Data-in hold time	t <sub>DH</sub>	10		15		15		ns	22
Data-in hold time (referenced to RAS)	t <sub>DHR</sub>	45		55		60		ns	
RAS to WE delay time	t <sub>RWD</sub>	85		95		105		ns	21
Column-address to WE delay time	t <sub>AWD</sub>	55		60		65		ns	21
CAS to WE delay time	t <sub>CWD</sub>	40		45		45		ns	21
Transition time (rise or fall)	t <sub>T</sub>	3	50	3	50	3	50	ns	9, 10
Refresh period (2,048 cycles)	t <sub>REF</sub>		32		32		32	ms	
RAS to CAS precharge time	t <sub>RPC</sub>	0		0		0		ns	
CAS setup time (CBR REFRESH)	t <sub>CSR</sub>	5		5		5		ns	5
CAS hold time (CBR REFRESH)	t <sub>CHR</sub>	15		15		15		ns	5
WE hold time (MASKED WRITE and CBR REFRESH)	t <sub>WRH</sub>	15		15		15		ns	26
WE setup time (CBR REFRESH)	t <sub>WRP</sub>	10		10		10		ns	26
WE setup time (MASKED WRITE)	t <sub>WRS</sub>	10		10		10		ns	26
OE setup prior to RAS during HIDDEN REFRESH cycle	t <sub>ORD</sub>	0		0		0		ns	
Output disable	t <sub>OD</sub>	3	15	3	15	3	15	ns	29, 33
OE hold time from WE during READ-MODIFY-WRITE cycle	t <sub>OEH</sub>	15		15		15		ns	28

**WIDE DRAM**

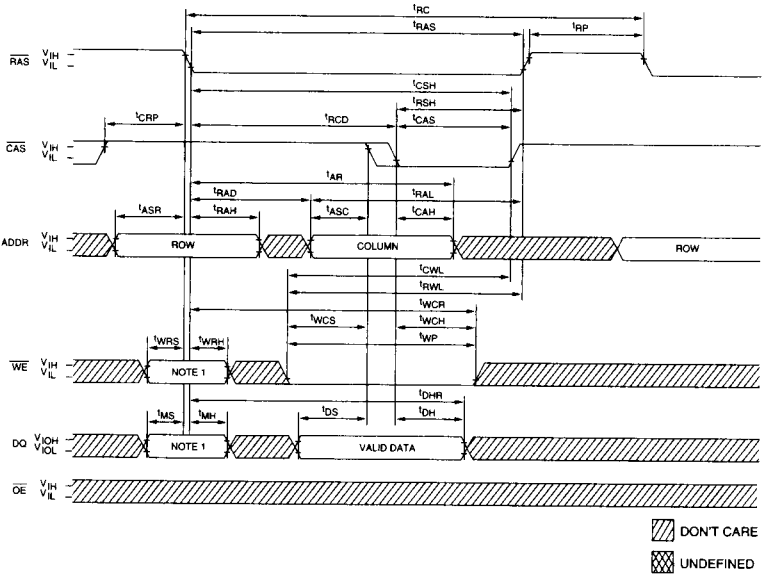
## NOTES



1. All voltages referenced to  $V_{SS}$ .
2. This parameter is sampled.  $V_{CC} = 5V \pm 10\%$ ;  $f = 1 \text{ MHz}$ .
3.  $I_{CC}$  is dependent on cycle rates.
4.  $I_{CC}$  is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ( $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ ) is assured.
7. An initial pause of  $100\mu\text{s}$  is required after power-up followed by eight  $\overline{\text{RAS}}$  refresh cycles ( $\overline{\text{RAS}}$ -ONLY or CBR) before proper device operation is assured. The eight  $\overline{\text{RAS}}$  cycle wake-ups should be repeated any time the  $\overline{\text{REF}}$  refresh requirement is exceeded.
8. AC characteristics assume  $T = 5\text{ns}$ .
9.  $V_{IH}$  (MIN) and  $V_{IL}$  (MAX) are reference levels for measuring timing of input signals. Transition times are measured between  $V_{IH}$  and  $V_{IL}$  (or between  $V_{IL}$  and  $V_{IH}$ ).
10. In addition to meeting the transition rate specification, all input signals must transit between  $V_{IH}$  and  $V_{IL}$  (or between  $V_{IL}$  and  $V_{IH}$ ) in a monotonic manner.
11. If  $\overline{\text{CAS}} = V_{IH}$ , data output is high impedance.
12. If  $\overline{\text{CAS}} = V_{IL}$ , data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to one TTL gate and  $50\text{pF}$ .
14. Assumes that  ${}^t\text{RCD} < {}^t\text{RCD}(\text{MAX})$ . If  ${}^t\text{RCD}$  is greater than the maximum recommended value shown in this table,  ${}^t\text{RAC}$  will increase by the amount that  ${}^t\text{RCD}$  exceeds the value shown.
15. Assumes that  ${}^t\text{RCD} \geq {}^t\text{RCD}(\text{MAX})$ .
16. If  $\overline{\text{CAS}}$  is LOW at the falling edge of  $\overline{\text{RAS}}$ , Q will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer,  $\overline{\text{CAS}}$  must be pulsed HIGH for  ${}^t\text{CPN}$ .
17. Operation within the  ${}^t\text{RCD}(\text{MAX})$  limit ensures that  ${}^t\text{RAC}(\text{MAX})$  can be met.  ${}^t\text{RCD}(\text{MAX})$  is specified as a reference point only; if  ${}^t\text{RCD}$  is greater than the specified  ${}^t\text{RCD}(\text{MAX})$  limit, access time is controlled exclusively by  ${}^t\text{CAC}$ .
18. Operation within the  ${}^t\text{RAD}$  limit ensures that  ${}^t\text{RCD}(\text{MAX})$  can be met.  ${}^t\text{RAD}(\text{MAX})$  is specified as a reference point only; if  ${}^t\text{RAD}$  is greater than the specified  ${}^t\text{RAD}(\text{MAX})$  limit, access time is controlled exclusively by  ${}^t\text{AA}$ .
19. Either  ${}^t\text{RCH}$  or  ${}^t\text{RRH}$  must be satisfied for a READ cycle.
20.  ${}^t\text{OFF}(\text{MAX})$  defines the time at which the output achieves the open circuit condition; it is not a reference to  $V_{OH}$  or  $V_{OL}$ .
21.  ${}^t\text{WCS}$ ,  ${}^t\text{RWD}$ ,  ${}^t\text{AWD}$  and  ${}^t\text{CWD}$  are restrictive operating parameters in LATE-WRITE and READ-MODIFY-WRITE cycles only. If  ${}^t\text{WCS} \geq {}^t\text{WCS}(\text{MIN})$ , the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If  ${}^t\text{RWD} \geq {}^t\text{RWD}(\text{MIN})$ ,  ${}^t\text{AWD} \geq {}^t\text{AWD}(\text{MIN})$  and  ${}^t\text{CWD} \geq {}^t\text{CWD}(\text{MIN})$ , the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data-out is indeterminate.  $\overline{\text{OE}}$  held HIGH and  $\overline{\text{WE}}$  taken LOW after  $\overline{\text{CAS}}$  goes LOW results in a LATE-WRITE ( $\overline{\text{OE}}$ -controlled) cycle.
22. These parameters are referenced to  $\overline{\text{CAS}}$  leading edge in EARLY-WRITE cycles and  $\overline{\text{WE}}$  leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
23. During a READ cycle, if  $\overline{\text{OE}}$  is LOW then taken HIGH before  $\overline{\text{CAS}}$  goes HIGH, Q goes open. If  $\overline{\text{OE}}$  is tied permanently LOW, LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case,  $\overline{\text{WE}} = \text{LOW}$  and  $\overline{\text{OE}} = \text{HIGH}$ .
25. All other inputs at  $V_{CC} - 0.2V$ .
26. Write command is defined as  $\overline{\text{WE}}$  going LOW.
27. MT4C2M8B2 only.
28. LATE-WRITE and READ-MODIFY-WRITE cycles must have both  ${}^t\text{OD}$  and  ${}^t\text{OE}$  met ( $\overline{\text{OE}}$  HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. If  $\overline{\text{OE}}$  is taken back LOW while  $\overline{\text{CAS}}$  remains LOW, the DQs will remain open.
29. The DQs open during READ cycles once  ${}^t\text{OD}$  or  ${}^t\text{OFF}$  occur. If  $\overline{\text{CAS}}$  goes HIGH before  $\overline{\text{OE}}$ , the DQs will open regardless of the state of  $\overline{\text{OE}}$ . If  $\overline{\text{CAS}}$  stays LOW while  $\overline{\text{OE}}$  is brought HIGH, the DQs will open. If  $\overline{\text{OE}}$  is brought back LOW ( $\overline{\text{CAS}}$  still LOW), the DQs will provide the previously read data.
30. The 5V version is restricted to operate between 4.5 V and 5.5V only.
31. The 3.0/3.3V version is restricted to operate between 2.7 V and 3.6V only. The -6 speed version is only valid for  $V_{CC} = 3.0V$  to 3.6V, whereas the -7 and -8 speed versions are valid for  $V_{CC} = 2.7V$  to 3.6V.
32. Column-address changed once while  $\overline{\text{RAS}} = V_{IL}$  and  $\overline{\text{CAS}} = V_{IH}$ .
33. The 3ns minimum is a parameter guaranteed by design.

READ CYCLE



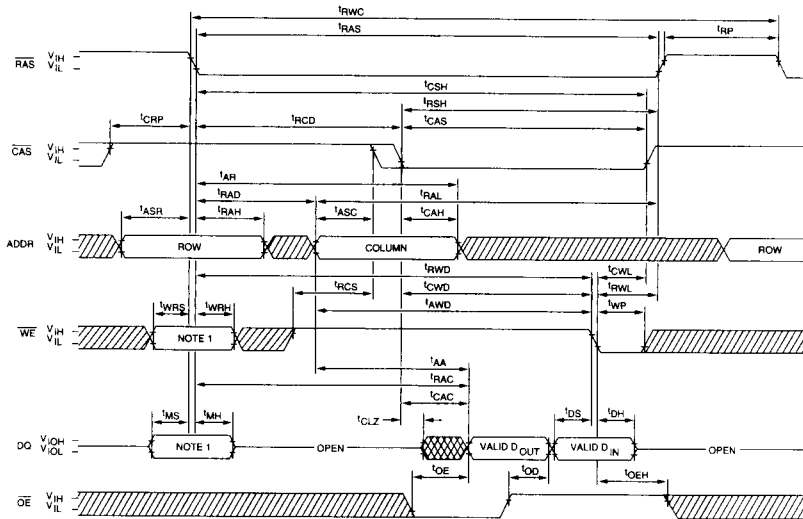
EARLY-WRITE CYCLE



 DONT CARE  
 UNDEFINED

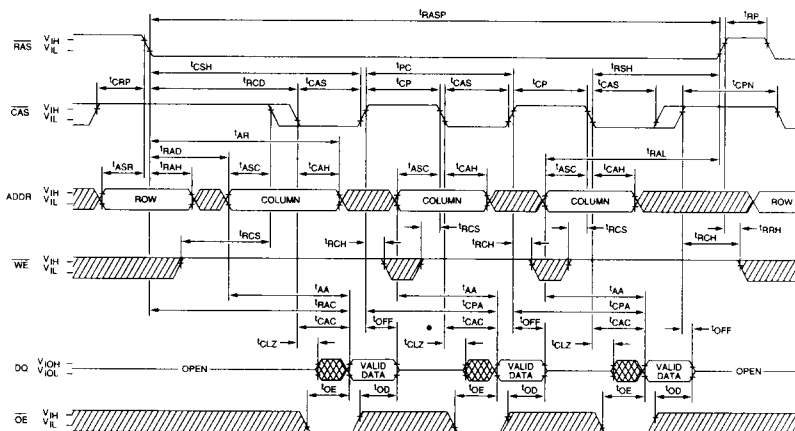
**NOTE:** 1. Applies to MT4C2M8B2 only;  $\overline{WE}$  and DQ inputs on MT4C2M8B1 are "don't care" at  $\overline{RAS}$  time.  $\overline{WE}$  selects between normal WRITE and MASKED WRITE at  $\overline{RAS}$  time. The DQ inputs are "don't care" for a normal WRITE ( $\overline{WE}$  HIGH at  $\overline{RAS}$  time). The DQ inputs provide the mask data at  $\overline{RAS}$  time for a MASKED WRITE,  $\overline{WE}$  LOW at  $\overline{RAS}$  time.

**READ-WRITE CYCLE  
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)**



**WIDE DRAM**

**FAST-PAGE-MODE READ CYCLE**

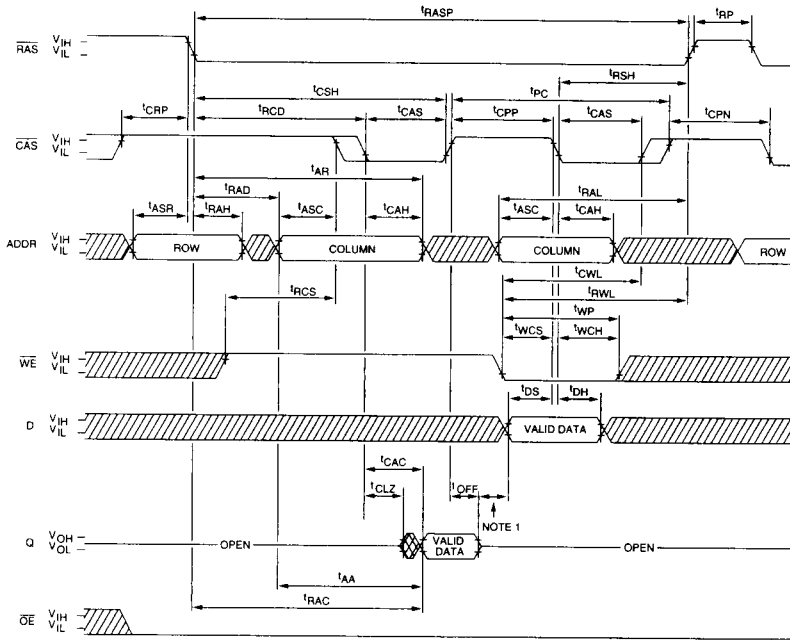


DON'T CARE  
 UNDEFINED

**NOTE:** 1. Applies to MT4C2M8B2 only;  $\overline{WE}$  and DQ inputs on MT4C2M8B1 are "don't care" at RAS time.  $\overline{WE}$  selects between normal WRITE and MASKED WRITE at RAS time. The DQ inputs are "don't care" for a normal WRITE ( $\overline{WE}$  HIGH at RAS time). The DQ inputs provide the mask data at RAS time for a MASKED WRITE,  $\overline{WE}$  LOW at RAS time.

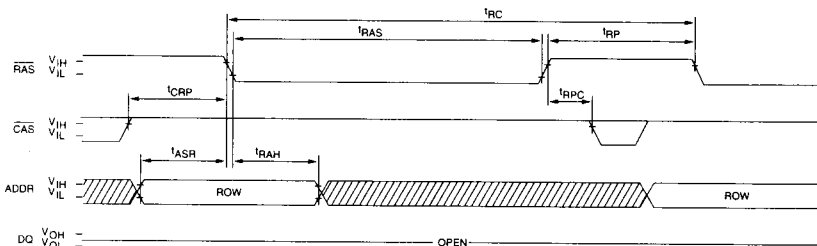


**FAST-PAGE-MODE READ-EARLY-WRITE CYCLE  
(Pseudo READ-MODIFY-WRITE)**



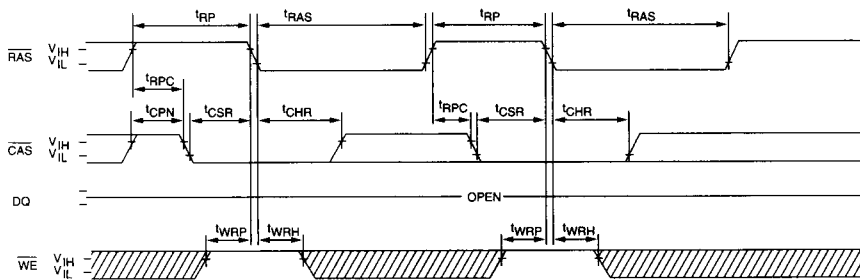
**NOTE:** 1. Do not drive data prior to High-Z; that is completion of  $t_{OFF}$ .  $t_{CPP}$  is equal to  $t_{OFF} + t_{DS(MIN)}$  + guardband between data-out and driving new data-in.

**RAS-ONLY REFRESH CYCLE  
( $\overline{OE}$  and  $\overline{WE}$  = DON'T CARE)**



DON'T CARE  
 UNDEFINED

**CBR REFRESH CYCLE**  
(A0-A10;  $\overline{OE}$  = DON'T CARE)



**HIDDEN REFRESH CYCLE**<sup>24</sup>  
( $\overline{WE}$  = HIGH;  $\overline{OE}$  = LOW)

