FIFO

1K x 9 FIFO

WITH PROGRAMMABLE FLAGS

FEATURES

- Very high speed: 15, 20, 25 and 35ns access
- High-performance, low-power CMOS process
- Single +5V ±10% supply
- Low power: 5mW typical (standby); 350mW typical (active)
- TTL compatible inputs and outputs
- Asynchronous READ and WRITE
- Two fully configurable Almost-Full and Almost-Empty Flags
- Programmable Half-Full Flag or Full/Empty Flag option eliminates external counter requirement
- Register loading via the input or output pins
- Auto-retransmit capability in SINGLE DEVICE mode
- Fully expandable by width and depth
- Pin- and function-compatible with standard higher- and lower-density FIFOs

OPTIONS

	MARKING
• Timing	
15ns access time	-15
20ns access time	-20
25ns access time	-25
35ns access time	-35
• Packages	
Plastic DIP (300 mil)	None
PLCC	EJ

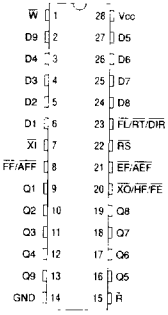
NOTE: Available in ceramic packages tested to meet military specifications. Please refer to Micron's *Military Data Book*.

• Temperature	
Industrial (-40°C to +85°C)	IT
Automotive (-40°C to +125°C)	AT

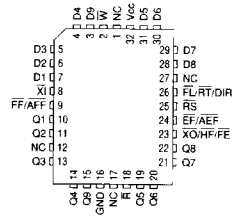
- Part Number Example: MT52C9012EJ-20

PIN ASSIGNMENT (Top View)

28-Pin DIP
(SA-4)



32-Pin PLCC
(SC-1)



GENERAL DESCRIPTION

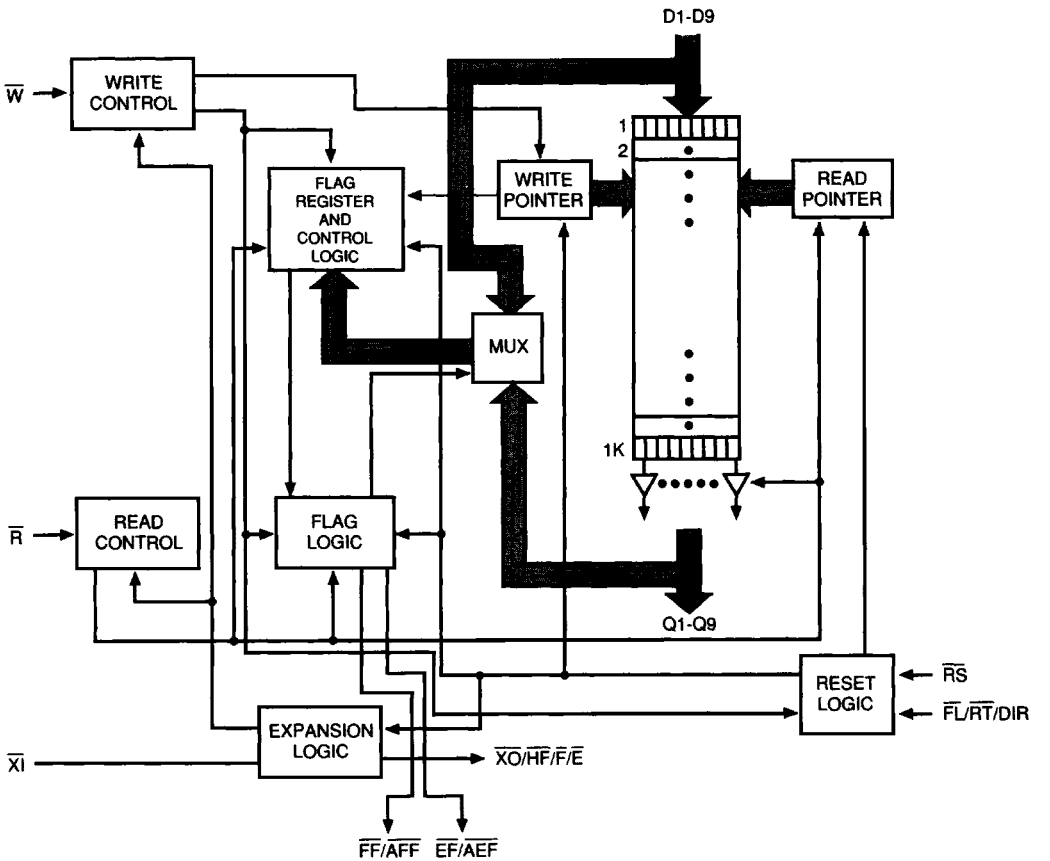
The Micron FIFO family employs high-speed, low-power CMOS designs using a true dual-port, six-transistor memory cell with resistor loads.

Micron FIFOs are written and read in a first-in-first-out sequence. Dual read and write pointers handle the internal addressing, so no external address generation is required. Information may be written to, and read from, the FIFO asynchronously and independently at the input and output ports. This allows information to be transferred independently in and out of the FIFO at varying data rates.

When not configured, the MT52C9012 defaults to a standard FIFO with empty ($\overline{EF}$), full ($\overline{FF}$) and half-full ($\overline{HF}$) flag pins. The MT52C9012 can be configured for programmable flags by loading the internal flag registers (as described under "Register Load Mode" on page 7-45). In CONFIGURED mode, up to three flags are provided. The first two are the almost-empty flag ($\overline{AEF}$) and the almost-full flag ($\overline{AFF}$) with independently programmable offsets. The third one is either an $\overline{HF}$ or a full and empty ($\overline{FE}$) flag, depending on the bit configuration of the registers. A retransmit pin allows data to be re-sent on the receiver's request when the FIFO is in the STAND ALONE mode.

The depth and/or width of the FIFO can be expanded by cascading multiple devices. Also, the MT52C9012 is speed, function and pin compatible with higher and lower density FIFOs from Micron. This upward compatibility with 2K FIFOs provides a single-chip depth-expansion solution.

FUNCTIONAL BLOCK DIAGRAM



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PIN DESCRIPTIONS

LCC PIN NUMBER(S)	DIP PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
25	22	$\overline{RS}$	Input	Reset: This pin is used to reset the device and load internal flag registers. During device reset, all internal pointers and registers are cleared.
2	1	$\overline{W}$	Input	Write: A LOW on this pin loads data into the device. The internal write pointer is incremented after the rising edge of the write input.
18	15	$\overline{R}$	Input	Read: A LOW on this pin puts the oldest valid data byte in the memory array on the output bus. The internal read pointer is incremented at the rising edge of the read signal. Outputs are in High-Z when this pin is HIGH.
8	7	$\overline{XI}$	Input	Expansion-In: This pin is used for DEPTH EXPANSION mode. In SINGLE DEVICE mode, it should be grounded. In EXPANDED mode, it should be connected to Expansion-Out ($\overline{XO}$) of the previous device in the daisy chain.
26	23	$\overline{FL}/\overline{RT}$/DIR	Input	First Load/Retransmit/Direction: When in SINGLE DEVICE mode, this pin can be used to initiate a reread of the previously read data. When in REGISTER LOAD mode, the pin is used for register loading direction. When it is LOW, registers are loaded through the data output pins. When it is HIGH, registers are loaded through the data input pins. In DEPTH EXPANSION mode, this pin should be tied LOW if the device is the first one in the chain and tied HIGH if it is not the first one.
7, 6, 5, 4, 31, 30, 29, 28, 3	6, 5, 4, 3, 27, 26, 25, 24, 2	D1-D9	Input	Data Inputs: Data on these lines are stored in the memory array or flag registers during array WRITE or register programming, respectively.
24	21	$\overline{EF}/\overline{AEF}$	Output	Empty Flag/Almost-Empty Flag: This output pin indicates the FIFO status. When in NONCONFIGURED mode, this pin is an Empty Flag output. When in CONFIGURED mode, it is an Almost-Empty Flag output. This pin is active LOW.
9	8	$\overline{FF}/\overline{AFF}$	Output	Full Flag/Almost-Full Flags: This output pin indicates the FIFO status. When in NONCONFIGURED mode, this pin is a Full Flag output. When in CONFIGURED mode, it is an Almost-Full Flag output. This pin is active LOW.
23	20	$\overline{XO}/\overline{HF}/\overline{FE}$	Output	Expansion Out/Half-Full/Full/Empty: This pin's function is determined by its operation mode. When in SINGLE DEVICE mode, this pin is either HF Flag or a Full/Empty Flag, depending on the state of the most significant bit of Almost-Full Flag Register. The pin is an $\overline{XO}$ output when the part is in DEPTH EXPANSION mode. This pin defaults to $\overline{XO}/\overline{HF}$ in NONCONFIGURED mode.
10, 11, 13, 14, 19, 20, 21, 22,15	9, 10, 11, 12, 16, 17, 18, 19, 13	Q1-Q9	I/O	Data Output: These pins may be used for data retrieval. The pins become inputs during register loading with DIR input LOW. The outputs are disabled (High-Z) during device idle ($\overline{R}$ = HIGH).
32	28	Vcc	Supply	Power Supply: +5V ±10%
16	14	GND	Supply	Ground

FUNCTIONAL DESCRIPTION

The MT52C9012 uses a dual port SRAM memory cell array with separate read and write pointers. This results in a flexible-length FIFO buffer memory with independent, asynchronous READ and WRITE capabilities and with no fall-through or bubble-through time constraints.

Note: *For multiple-function pins, the function that is not being discussed will be surrounded by parentheses. For example, the $\overline{XO}/\overline{HF}/(\overline{FE})$ pin will be shown as $(\overline{XO})/\overline{HF}/(\overline{FE})$ when discussing half-full flags.*

RESET

After Vcc is stable, reset ($\overline{RS}$) must be taken LOW with both $\overline{R}$ and $\overline{W}$ HIGH to initialize the read and write pointers and flags. This also clears all internal registers. During the reset pulse, the state of the $\overline{XI}$ pin will determine if the FIFO will operate in the STAND ALONE or DEPTH EXPANSION mode. The STAND ALONE mode is entered if $\overline{XI}$ is tied LOW. If $\overline{XI}$ is connected to $\overline{XO}/(\overline{HF})$ of another FIFO, the DEPTH EXPANSION mode is selected.

WRITING THE FIFO

Data is written into the FIFO when the write strobe ($\overline{W}$) pin is taken LOW and if the FIFO is not full. The WRITE cycle is initiated by the falling edge of $\overline{W}$. Data on the D1-D9 pins are latched on the rising edge. If the location to be written is the final empty location in the FIFO, $\overline{FF}$ will be asserted (LOW) after the falling edge of $\overline{W}$. While $\overline{FF}$ is asserted, all writes are inhibited, and previously stored data is unaffected. The first WRITE to an empty FIFO will cause $\overline{EF}$ to go HIGH after the rising edge of $\overline{W}$. When operating in the DEPTH EXPANSION mode, the last location write to a FIFO will cause $\overline{XO}/(\overline{HF})$ to pulse LOW. This will enable writes to the next FIFO in the chain.

READING THE FIFO

Information is read from the FIFO when the read strobe ($\overline{R}$) pin is taken LOW and FIFO is not empty ($\overline{EF}$ is HIGH). The data-out (Q1-Q9) pins will go active (Low-Z) ^tRLZ after the falling edge of $\overline{R}$. Valid data will appear ^tA after the falling edge of $\overline{R}$. After the last available data word is read, $\overline{EF}$ will go LOW upon the falling edge of $\overline{R}$. While $\overline{EF}$ is asserted LOW, any attempted reads will be inhibited and the outputs will stay inactive (High-Z). When the FIFO is full and a READ is initiated, the $\overline{FF}$ will go HIGH after the rising edge of $\overline{R}$. When operating in the EXPANDED mode, the last location read from a FIFO will cause $\overline{XO}/(\overline{HF})$ to pulse LOW. This will enable further reads from the next FIFO in the chain.

RETRANSMIT

In the STAND ALONE mode, the MT52C9012 allows the receiving device to request that data read earlier from the FIFO be repeated, when less than 1,024 writes have been performed between resets. When the $(\overline{FL})/\overline{RT}/(DIR)$ pin is taken LOW, the read pointer is reset to the first location while the write pointer is not affected. The receiver may start reading the data from the beginning of the FIFO ^tRTR after $(\overline{FL})/\overline{RT}/(DIR)$ is taken HIGH. Some or all flags may be affected depending on the location of the read and write pointers before and after the retransmit.

DATA FLOW-THROUGH

Data flow-through is a method of writing and reading the FIFO at its full and empty boundaries, respectively. By holding $\overline{W}$ LOW when the FIFO is full, a WRITE can be initiated from the next ensuing READ pulse. This is referred to as a FLOW-THROUGH WRITE. FLOW-THROUGH WRITEs are initiated from the rising edge of $\overline{R}$. When the FIFO is empty, a FLOW-THROUGH READ can be done by holding $\overline{R}$ LOW and letting the next WRITE initiate the READ. Flow-through reads are initiated from the rising edge of $\overline{W}$, and access time is measured from the rising edge of the empty flag.

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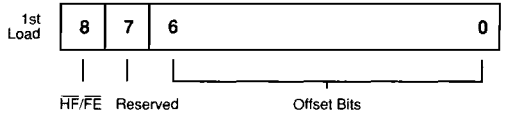
REGISTER LOAD MODE

This mode of operation is used to reset the device and program the internal flag registers. This yields an almost full and an almost-empty flag (DIP package pins 8 and 21 respectively) and a half-full or $\overline{F}/\overline{E}$ flag (DIP package pin 20).

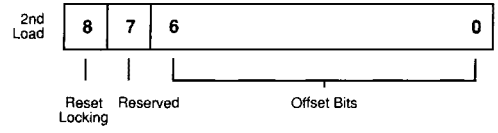
Two 9-bit internal registers have been provided for flag configuration. One is the almost-full flag register (AFFR) and the other is the almost-empty flag register (AEFR). Bit configurations of the two registers are shown below.

REGISTER SET FOR MT52C9012

Almost Full Flag Register (AFFR)



Almost Empty Flag Register (AEFR)



Note that bits 0-6 are used for setting the offset value. The offset value ranges from 1 to 127 increments. Each increment value corresponds to 2 words. This provides a maximum offset of 254 words.

Bit 7 is reserved for future offset expansion. Bit 8 of the AFFR is used for configuration of $\overline{HF}/\overline{FE}$ pin. When this bit is set LOW, the HF/$\overline{FE}$ pin is configured as an $\overline{HF}$ flag output. When it is set HIGH, the HF/$\overline{FE}$ is configured as an $\overline{F}/\overline{E}$ flag output.

Bit 8 of the AEFR is used for reset locking. When this bit is set LOW, subsequent device RESET or REGISTER LOADING cycles reset the device. When the bit is programmed HIGH, subsequent RESET cycles are ignored. In this mode, the flag registers can be reconfigured without device reset. The part can be reset by cycling power to the device or by writing zero (0) into bit 8 of the AEFR register followed by a DEVICE RESET or REGISTER LOAD.

Flag registers are loaded by bringing $\overline{RS}$ LOW followed by the $\overline{R}$ input. The $\overline{R}$ pin should be brought LOW ^tRS after the $\overline{RS}$ becomes LOW. The registers may be loaded via the input pins or the output pins depending on the status of the DIR control input. Data is latched into the registers at the rising edge of the $\overline{W}$ control pin. The first WRITE loads the AFFR while the second WRITE loads the AEFR. This loading order is fixed.

BIDIRECTIONAL APPLICATIONS

Applications requiring data buffering between two systems (each system capable of READ and WRITE operations) can be achieved by using two MT52C9012s. Care must be taken to assure that the appropriate flag is monitored by each system (i.e. $\overline{FF}$ is monitored on the device where $\overline{W}$ is used; $\overline{EF}$ is monitored on the device where $\overline{R}$ is used). Both depth expansion and width expansion may be used in this mode.

FLAG TIMING

A total of three flag outputs are provided in either CONFIGURED or NONCONFIGURED mode. In the NONCONFIGURED mode, the three flags are $\overline{HF}$, $\overline{EF}$ and $\overline{FF}$. The $\overline{HF}$ flag goes active when more than half the FIFO is full. The flag goes inactive when the FIFO is half full or less.

The full and empty flags are asserted when the last byte is written to or read out of the FIFO, respectively. They are deasserted when the first byte is loaded into an empty FIFO or read out of a full FIFO, respectively. All three flag outputs are active LOW.

When the device is programmed, the $\overline{AFF}$ and $\overline{AEF}$ go active after a READ/WRITE cycle initiation of the location corresponding to the programmed offset value. For example, if the AEFR is programmed with a 10-byte offset (loading a Hex value of 05), the $\overline{AEF}$ flag goes active while reading the 10th location before the FIFO is empty. The flag goes inactive when there are 10 or more bytes left in the FIFO. The assertion timing and deassertion timing of the $\overline{AFF}$ are the same.

The third flag in the PROGRAM mode is either $\overline{HF}$ or $\overline{F}/\overline{E}$ flag depending on the state of the highest bit of the AFFR. If the device is programmed for $\overline{HF}$ flag, it functions like the $\overline{HF}$ flag in NONPROGRAMMED mode. If the device is configured for $\overline{F}/\overline{E}$ flag, the pin will be active (LOW) when the FIFO is either empty or full. The condition of the FIFO is determined by the state of $\overline{F}/\overline{E}$ together with states of $\overline{AFF}$ and $\overline{AEF}$ (example: if $\overline{F}/\overline{E}$ is LOW and $\overline{AFF}$ is LOW but $\overline{AEF}$ is HIGH, the FIFO is full).

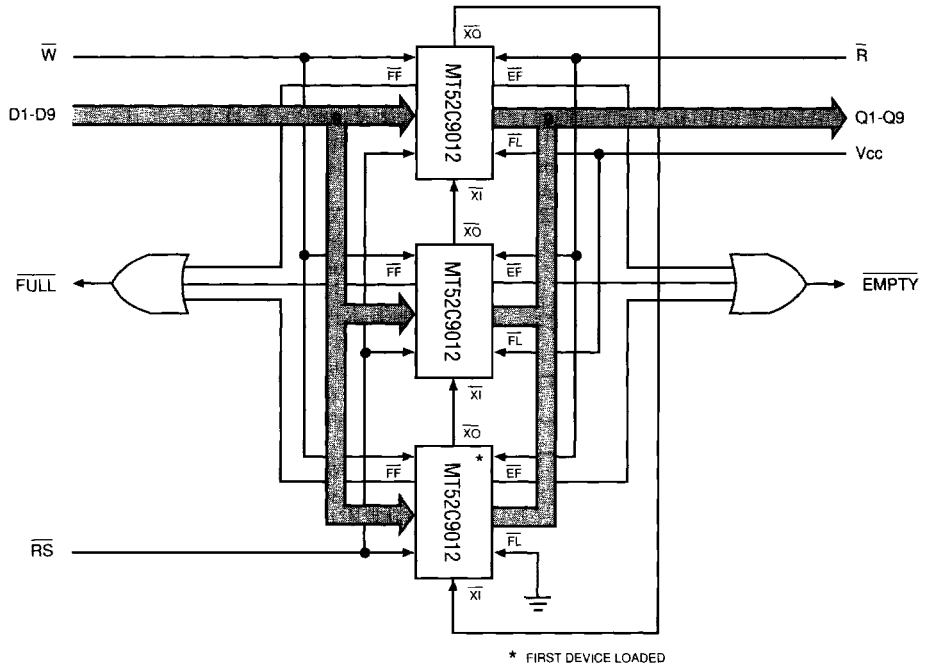


Figure 1
DEPTH EXPANSION

WIDTH EXPANSION

The FIFO word width can be expanded, in increments of 9 bits, using either the STAND ALONE or groups of EXPANDED DEPTH mode FIFOs. Expanded width operation is achieved by tying devices together with all control lines ($\overline{W}$, $\overline{R}$, etc.) in common. The flags are monitored from one device or one expanded-depth group (Figure 1), when expanding depth and width.

DEPTH EXPANSION

Multiple MT52C9012s may be cascaded to expand the depth of the FIFO buffer. Three pins are used to expand the memory depth, $\overline{XI}$, $\overline{XO}$/($\overline{HF}$/$\overline{FE}$) and $\overline{FL}$/($\overline{RT}$/DIR). Figure 1 illustrates a typical three-device expansion. The DEPTH EXPANSION mode is entered by tying the $\overline{XO}$/($\overline{HF}$/$\overline{FE}$) pin of each device to the $\overline{XI}$ pin of the next device in the chain. The first device to be loaded will have its $\overline{FL}$/($\overline{RT}$/DIR) pin grounded. The remaining devices in the chain will have $\overline{FL}$/($\overline{RT}$/DIR) tied HIGH. Upon a reset, reads and writes to all FIFOs are disabled, except the first load device. When the last physical location of the first device is written, the $\overline{XO}$/($\overline{HF}$) pin will pulse LOW on the falling edge of $\overline{W}$. This will "pass" the write pointer to the next device in the chain, enabling writes to that device and disabling writes to the first MT52C9012. The writes will continue to go to the second device until last location write. Then it will "pass" the write pointer to the third device. The full condition of the entire FIFO array is signaled when all the $\overline{FF}$/($\overline{AFF}$) pins are LOW.

On the last physical READ of the first device, its $\overline{XO}$ ($\overline{HF}$) will pulse again. On the falling edge of $\overline{R}$, the read pointer is "passed" to the second device. The read pointer will, in effect, "chase" the write pointer through the extended FIFO array. The read pointer never overtakes the write pointer. On the last READ, an empty condition is signaled by all of the $\overline{EF}$ pins being LOW. This inhibits further reads. While in the DEPTH EXPANSION mode, the half-full flag and retransmit functions are not available.

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TRUTH TABLE 1
SINGLE-DEVICE CONFIGURATION/WIDTH-EXPANSION MODE

	INPUTS			INTERNAL STATUS		OUTPUTS		
MODE	$\overline{RS}$	$\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$
RESET	0	X	0	Location Zero	Location Zero	0	1	1
RETRANSMIT	1	0	0	Location Zero	Unchanged	1	X	X
READ/WRITE	1	1	0	Increment (1)	Increment (1)	X	X	X

NOTE: 1. Pointer will increment if flag is HIGH.

TRUTH TABLE 2
DEPTH-EXPANSION/COMPOUND-EXPANSION MODE

	INPUTS			INTERNAL STATUS		OUTPUTS	
MODE	$\overline{RS}$	$\overline{FL}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
RESET First Device	0	0	(1)	Location Zero	Location Zero	0	1
RESET All Other Devices	0	1	(1)	Location Zero	Location Zero	0	1
READ/WRITE	1	X	(1)	X	X	X	X

NOTE: 1. XI is connected to $\overline{XO}$ of previous device.
2. $\overline{RS}$ = Reset Input; $\overline{FL}/\overline{RT}$/DIR = First Load/Retransmit; $\overline{EF}$ = Empty Flag Outpu; $\overline{FF}$ = Full Flag Output; $\overline{XI}$ = Expansion Input; $\overline{HF}$ = Half-Full Flag Output.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -0.5V to +7V
Operating Temperature T_A (ambient) ..... 0°C to 70°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA
Voltage on any pin relative to V_{SS} ..... -1V to V_{CC} +1V

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.0	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-0.5	0.8	V	1, 2

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DC ELECTRICAL CHARACTERISTICS

(0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

			MAX					
DESCRIPTION	CONDITIONS	SYMBOL	-15	-20	-25	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{W}, \overline{R} \le V_{IL}$; V_{CC} = MAX f = MAX = 1/^tRC Outputs Open	I_{CC}	140	130	120	110	mA	3
Power Supply Current: Standby	$\overline{W}, \overline{R} \ge V_{IH}$; V_{CC} = MAX f = MAX = 1/^tRC Outputs Open	I_{SB1}	15	15	15	15	mA	
	$\overline{W}, \overline{R} \ge V_{CC}$ -0.2; V_{CC} = MAX $V_{IN} \le V_{SS}$ +0.2 or $V_{IN} \ge V_{CC}$ -0.2; f = 0	I_{SB2}	5	5	5	5	mA	

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	I_{LI}	-10	10	µA	
Output Leakage Current	Output(s) Disabled 0V ≤ V_{OUT} ≤ V_{CC}	I_{LO}	-10	10	µA	
Output High Voltage	I_{OH} = -2.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

CAPACITANCE

(V_{IN} = 0V; V_{OUT} = 0V)

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	8	pF	4
Output Capacitance	V_{CC} = 5V	C_O	8	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Applicable for configured and nonconfigured modes) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-15		-20		-25		-35			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
READ Cycle											
Shift frequency	^tRF		40		33.3		28.5		22.2	MHz	
READ cycle time	^tRC	25		30		35		45		ns	
Access time	^tA		15		20		25		35	ns	6
READ recovery time	^tRR	10		10		10		10		ns	
READ pulse width	^tRPW	15		20		25		35		ns	
READ LOW to Low-Z	^tRLZ	3		3		3		3		ns	7
READ HIGH to High-Z	^tRHZ		15		15		18		20	ns	7
Data HOLD from $\overline{R}$ HIGH	^tOH	5		5		5		5		ns	
WRITE Cycle											
WRITE cycle time	^tWC	25		30		35		45		ns	
WRITE pulse width	^tWPW	15		20		25		35		ns	6
WRITE recovery time	^tWR	10		10		10		10		ns	
WRITE HIGH to Low-Z	^tWLZ	5		5		5		5		ns	5, 7
Data setup time	^tDS	10		12		15		18		ns	
Data hold time	^tDH	0		0		0		0		ns	
RETRANSMIT Cycle											
RESTRANSMIT cycle time	^tRTC	25		30		35		45		ns	
RESTRANSMIT pulse width	^tRT	15		20		25		35		ns	
RESTRANSMIT recovery time	^tRTR	10		10		10		12		ns	
RESTRANSMIT setup time	^tRTS	15		20		25		35		ns	
RESET Cycle											
RESET cycle time (no register programming)	^tRSC	25		30		35		45		ns	
RESET pulse width	^tRSP	15		20		25		35		ns	6
RESET recovery time	^tRSR	10		10		10		10		ns	
$\overline{RS}$ LOW to $\overline{R}$ LOW	^tRS	15		20		25		35		ns	
RESET and register programming cycle time	^tRSPC	85		100		115		145		ns	
$\overline{R}$ LOW to DIR valid (register load cycle)	^tRDV	5		5		5		5		ns	
$\overline{R}$ LOW to register load	^tRW	10		10		10		10		ns	
$\overline{W}$ HIGH to $\overline{RS}$ LOW	^tWRS	0		0		0		0		ns	
$\overline{R}$ HIGH to $\overline{RS}$ LOW	^tRRS	0		0		0		0		ns	

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Applicable for configured mode only) (T_A = 0°C to 70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-15		-20		-25		-35			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Expansion Mode Timing											
R/W to XO LOW	tXOL		15		20		25		35	ns	
R/W to XO HIGH	tXOH		15		20		25		35	ns	
XI pulse width	tXIP	15		20		25		35		ns	
XI setup time to R/W	tXIS	10		12		15		15		ns	
XI recovery time	tXIR	10		10		10		10		ns	
Flags Timing											
W HIGH to Flags Valid	tWFV		15		15		15		15	ns	
RS to AEF, EF LOW	tEFL		25		30		35		45	ns	
R LOW to EF LOW	tREF		20		20		25		30	ns	
W HIGH to EF HIGH	tWEF		20		20		25		30	ns	
R HIGH after EF HIGH	tRPE	15		20		25		35		ns	5
RS to AFF, HF, FF HIGH	tHFH, tFFH		25		30		35		45	ns	
R HIGH to FF HIGH	tRFF		15		20		25		30	ns	
W LOW to FF LOW	tWFF		20		20		25		30	ns	
W HIGH after FF HIGH	tWPF	15		20		25		35		ns	5
W LOW to HF LOW	tWHF		25		30		35		45	ns	
R HIGH to HF HIGH	tRHF		25		30		35		45	ns	
R HIGH to AFF HIGH	tRAFF		25		30		35		45	ns	
W LOW to AFF LOW	tWAFF		25		30		35		45	ns	
R LOW to AEF LOW	tRAEF		25		30		35		45	ns	
W HIGH to AEF HIGH	tWAEF		25		30		35		45	ns	

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AC TEST CONDITIONS

Input pulse level	0 to 3.0V
Input rise and fall times	5ns
Input timing reference level	1.5V
Output reference level	1.5V
Output load	See Figure 2

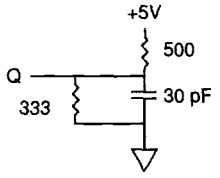
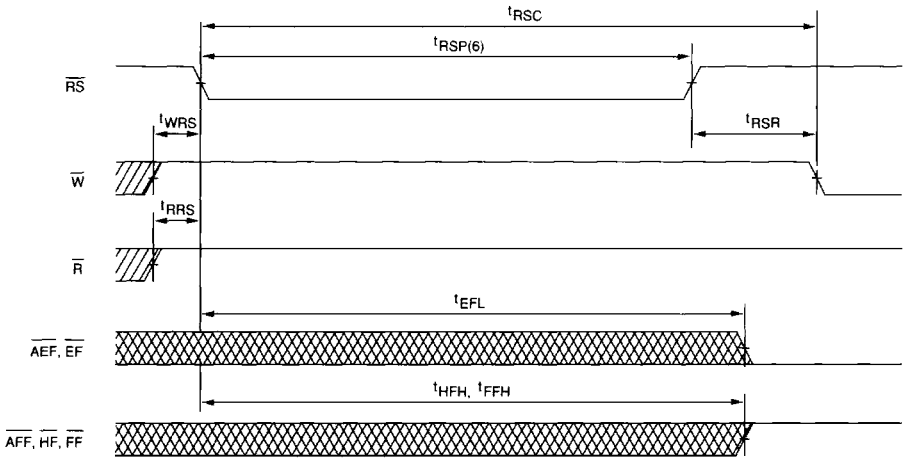


Figure 2
OUTPUT LOAD EQUIVALENT

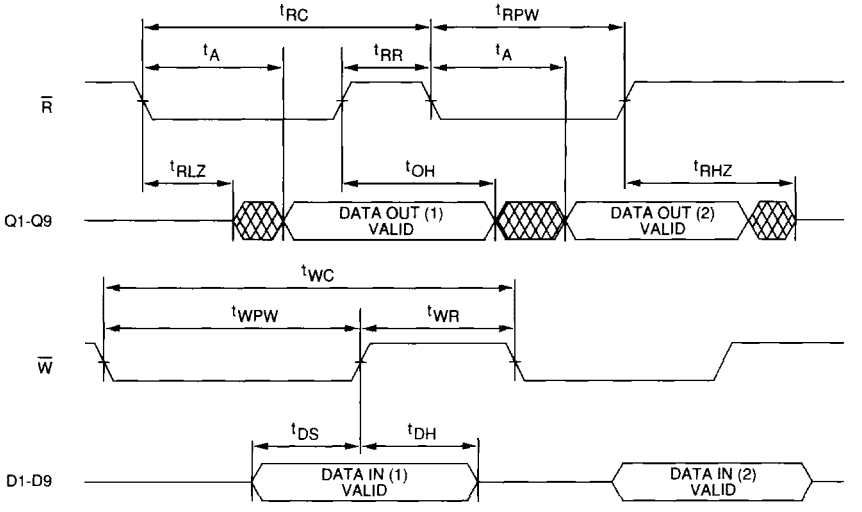
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < tRC/2.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Data flow-through data mode only.
6. Pulse widths less than minimum are not allowed.
7. Values guaranteed by design, not currently tested.
8. R and DIR signals must go inactive (HIGH) coincident with RS going inactive (HIGH).
9. DIR must become valid before W goes active (LOW).

RESET
(WITH NO REGISTER PROGRAMMING)



ASYNCHRONOUS READ AND WRITE

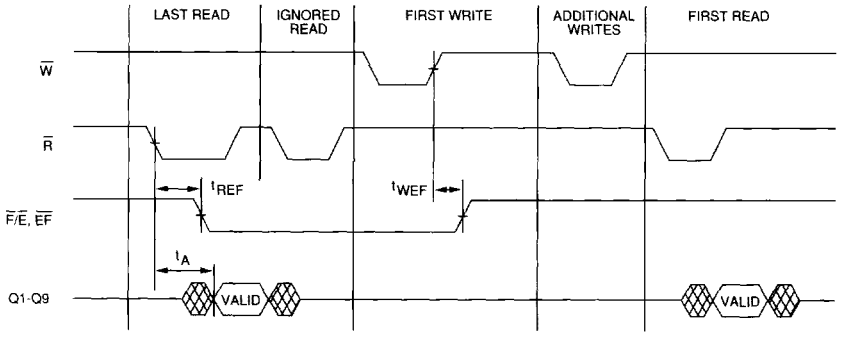


DON'T CARE

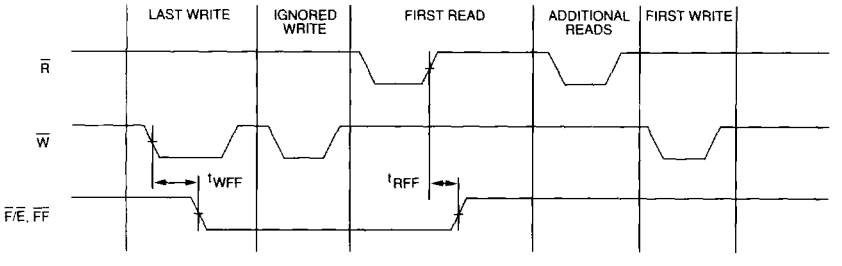
UNDEFINED

FIFO

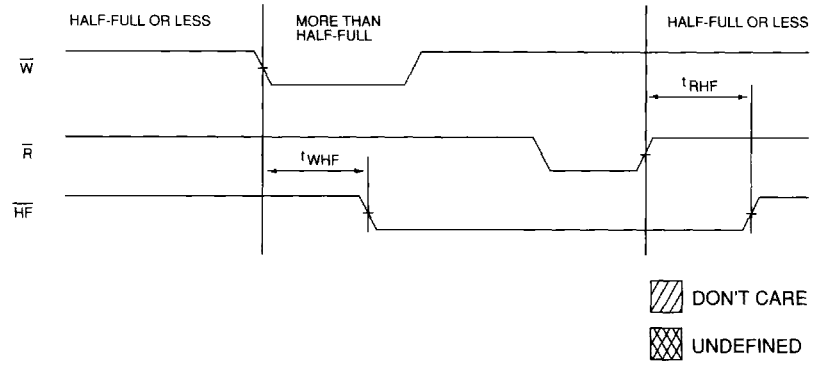
EMPTY FLAG



FULL FLAG

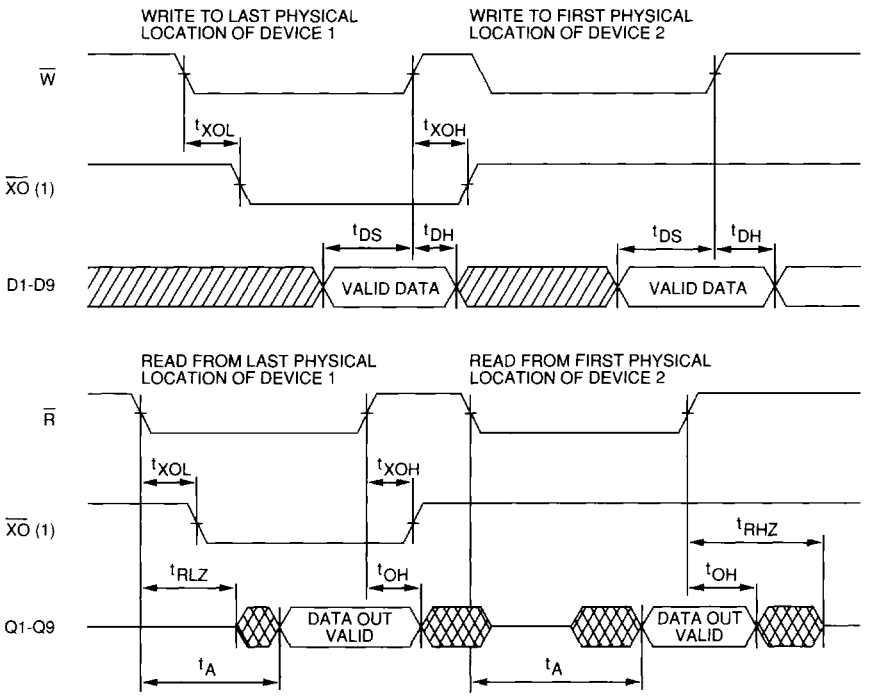


HALF-FULL FLAG
(FOR CONFIGURED AND NONCONFIGURED MODES)



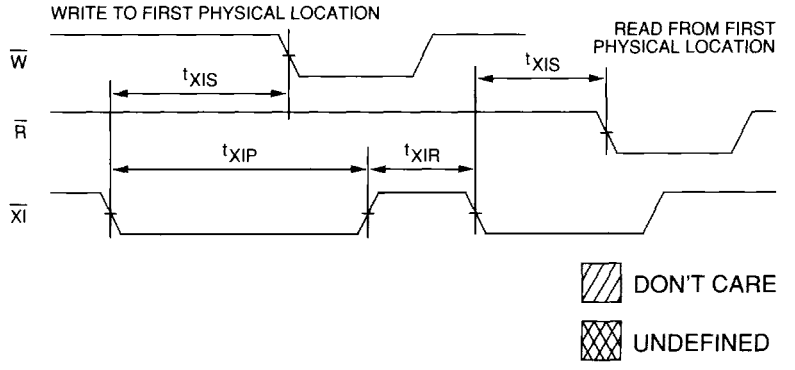
FIFO

EXPANSION MODE ($\overline{XO}$)



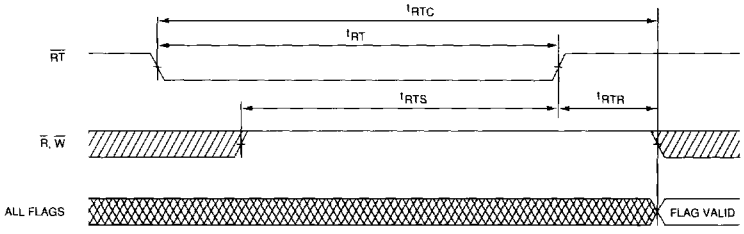
NOTE: 1. $\overline{XO}$ of the Device 1 is connected to $\overline{XI}$ of Device 2.

EXPANSION MODE ($\overline{XI}$)

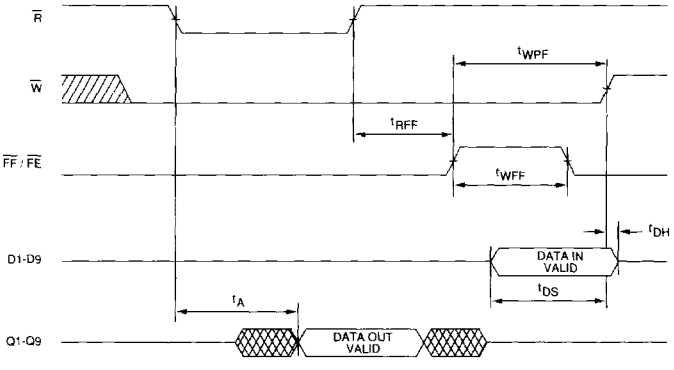


FIFO

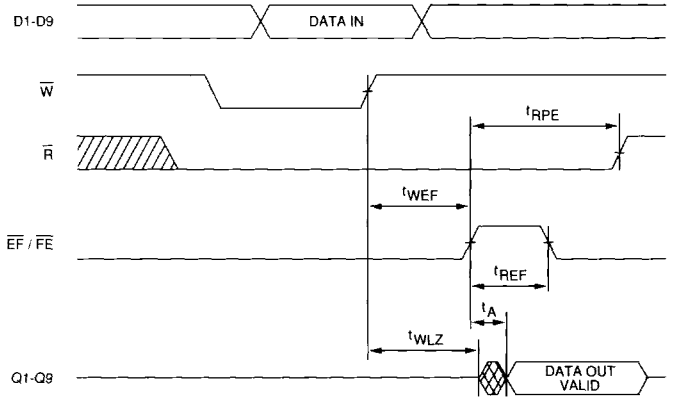
RETRANSMIT

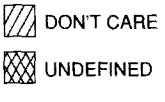


WRITE FLOW-THROUGH



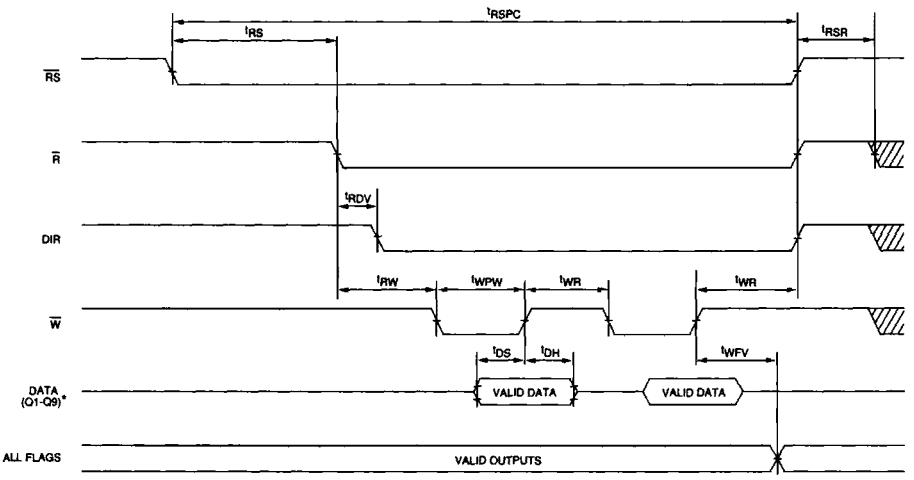
READ FLOW-THROUGH





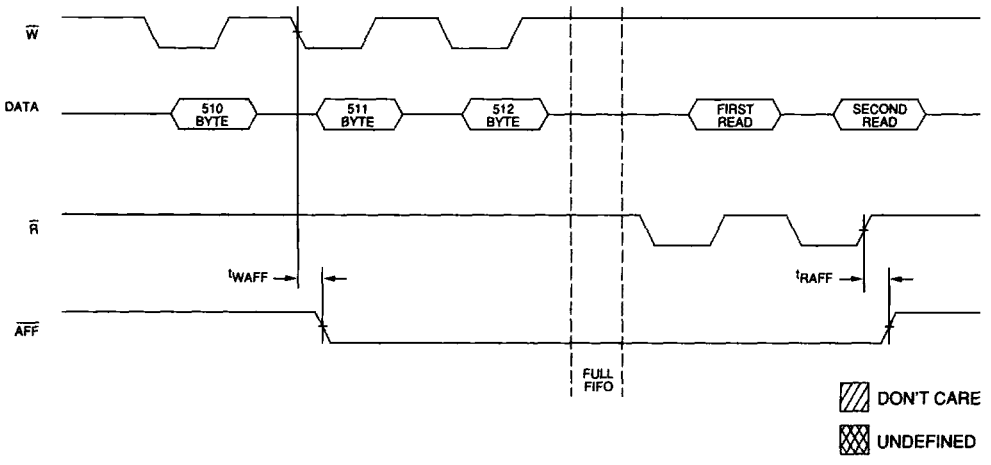
FIFO

RESET/REGISTER PROGRAMMING CYCLE TIME [8, 9]



* When DIR = LOW, data is loaded from Q1-Q8; when DIR = HIGH, data is loaded from D1-D9.

ALMOST-FULL FLAG (2-BYTE OFFSET)



FIFO

ALMOST-EMPTY FLAG (10-BYTE OFFSET)