PA84 • PA84A • PA84S

FEATURES

- **HIGH SLEW RATE — 200V/μs**
- **FAST SETTLING TIME — .1% in 1μs (PA84S)**
- **FULLY PROTECTED INPUT — Up to ±150v**
- **LOW BIAS CURRENT, LOW NOISE — FET Input**
- **WIDE SUPPLY RANGE — ±15V to ±150V**

APPLICATIONS

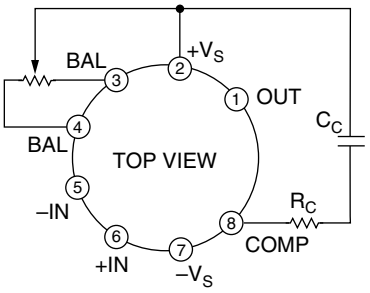
- **HIGH VOLTAGE INSTRUMENTATION**
- **ELECTROSTATIC TRANSDUCERS & DEFLECTION**
- **PROGRAMMABLE POWER SUPPLIES UP TO 290V**
- **ANALOG SIMULATORS**

DESCRIPTION

The PA84 is a high voltage operational amplifier designed for output voltage swings up to ±145V with a dual supply or 290V with a single supply. Two versions are available. The new PA84S, fast settling amplifier can absorb differential input overvoltages up to ±50V while the established PA84 and PA84A can handle differential input overvoltages of up to ±300V. Both versions are protected against common mode transients and overvoltages up to the supply rails. High accuracy is achieved with a cascode input circuit configuration. All internal biasing is referenced to a zener diode fed by a FET constant current source. As a result, the PA84 features an unprecedented supply range and excellent supply rejection. The output stage is biased-on for linear operation. External phase compensation allows for user flexibility in obtaining the maximum slew rate. Fixed current limits protect these amplifiers against shorts to common at supply voltages up to 150V. For operation into inductive loads, two external flyback pulse protection diodes are recommended. With the exception of PA84S, a built-in thermal shutoff circuit prevents destructive overheating. However, a heatsink may be necessary to maintain the proper case temperature under normal operating conditions.

This hybrid integrated circuit utilizes a beryllia (BeO) substrate, thick film resistors, ceramic capacitors and semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8-pin TO-3 package is hermetically sealed and electrically isolated. The use of compressible thermal isolation washers and/or improper mounting torque will void the product warranty. Please see “General Operating Considerations”.

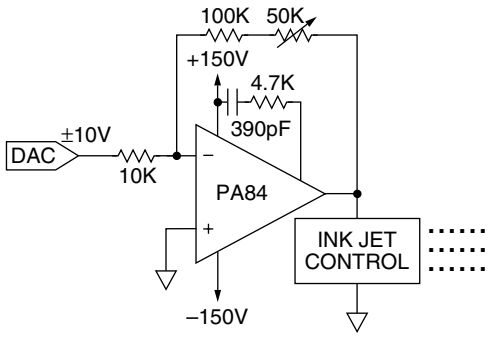
EXTERNAL CONNECTION



PHASE COMPENSATION

GAIN	C_C	R_C
1	10nF	200Ω
10	500pF	2KΩ
100	50pF	20KΩ
1000	none	none

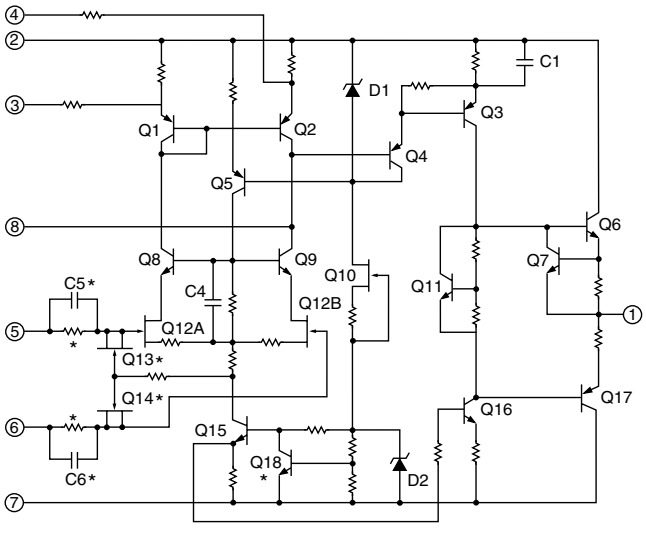
NOTES:
1. Phase Compensation required for safe operation.
2. Input offset trimpot optional. Recommended value 100KΩ.



TYPICAL APPLICATION

The PA84 is ideally suited to driving ink jet control units (often a piezo electric device) which require precise pulse shape control to deposit crisp clear date or lot code information on product containers. The external compensation network has been optimized to match the gain setting of the circuit and the complex impedance of the ink jet control unit. The combination of speed and high voltage capabilities of the PA84 form ink droplets of uniform volume at high production rates to enhance the value of the printer.

EQUIVALENT SCHEMATIC



* NOTE: Not used for PA84S

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	300V
OUTPUT CURRENT, within SOA	Internally Limited
POWER DISSIPATION, internal at T_C = 25°C[2]	17.5W
INPUT VOLTAGE, differential PA84/PA84A[1]	±300V
INPUT VOLTAGE, differential PA84S	±50V
INPUT VOLTAGE, common mode[1]	$\pm V_S$
TEMPERATURE, pins for 10s max (solder)	300°C
TEMPERATURE, junction[2]	200°C
TEMPERATURE RANGE, storage	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–55 to +125°C

SPECIFICATIONS

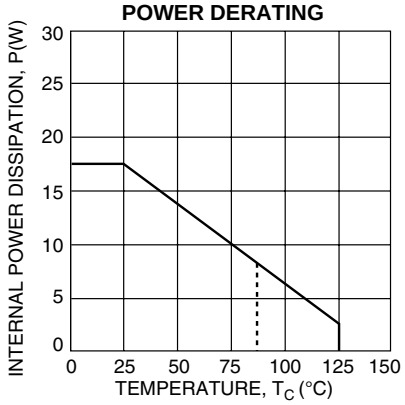
		PA84/PA84S			PA84A			
PARAMETER	**TEST CONDITIONS[3]**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT								
OFFSET VOLTAGE, initial	T_C = 25°C		±1.5	±3		±.5	±1	mV
OFFSET VOLTAGE, vs. temperature	T_C = –25° to +85°C		±10	±25		±5	±10	µV/°C
OFFSET VOLTAGE, vs. supply	T_C = 25°C		±.5			±.2		µV/V
OFFSET VOLTAGE, vs. time	T_C = 25°C		±75			*		µV/√kh
BIAS CURRENT, initial[4]	T_C = 25°C		5	50		3	10	pA
BIAS CURRENT, vs. supply	T_C = 25°C		.01			*		pA/V
OFFSET CURRENT, initial[4]	T_C = 25°C		±2.5	±50		±1.5	±10	pA
OFFSET CURRENT, vs. supply	T_C = 25°C		±.01			*		pA/V
INPUT IMPEDANCE, DC	T_C = 25°C		10^{11}			*		Ω
INPUT CAPACITANCE	T_C = –25° to +85°C		6			*		pF
COMMON MODE VOLTAGE RANGE[5]	T_C = –25° to +85°C	$\pm V_S$–10	$\pm V_S$–8.5		*	*		V
COMMON MODE REJECTION, DC	T_C = –25° to +85°C		130			*		dB
GAIN								
OPEN LOOP GAIN at 10Hz	T_C = 25°C, R_L = ∞		120			*		dB
OPEN LOOP GAIN at 10Hz.	T_C = 25°C, R_L = 3.5KΩ	100	118		*	*		dB
GAIN BANDWIDTH PRODUCT@ 1MHz	T_C = 25°C, R_L = 3.5KΩ, R_C = 20KΩ		75			*		MHz
POWER BANDWIDTH, high gain	T_C = 25°C, R_L = 3.5KΩ, R_C = 20KΩ		250		180	*		kHz
POWER BANDWIDTH, low gain	T_C = 25°C, R_L = 3.5KΩ, R_C = 20KΩ		120			*		kHz
OUTPUT								
VOLTAGE SWING[5]	T_C = 25°C, I_O = ±40mA	$\pm V_S$–7	$\pm V_S$–3		*	*		V
VOLTAGE SWING[5]	T_C = –25° to +85°C, I_O = ±15mA	$\pm V_S$–5	$\pm V_S$–2		*	*		V
CURRENT, peak	T_C = 25°C	40			*			mA
CURRENT, short circuit	T_C = 25°C		50			*		mA
SLEW RATE, high gain	T_C = 25°C, R_L = 3.5KΩ, R_C = 20KΩ		200		150	*		V/µs
SLEW RATE, low gain	T_C = 25°C, R_L = 3.5KΩ, R_C = 2KΩ		125			*		V/µs
SETTLING TIME .01% at gain = 100	T_C = 25°C, R_L = 3.5KΩ **PA84S**		2					µs
SETTLING TIME .1% at gain = 100	R_C = 20KΩ, V_{IN} = 2V step **ONLY**		1					µs
SETTLING TIME .01% at gain = 100	T_C = 25°C, R_L = 3.5KΩ **PA84/84A**		20			20		µs
SETTLING TIME .1% at gain = 100	R_C = 20KΩ, V_{IN} = 2V step		12			12		µs
POWER SUPPLY								
VOLTAGE	T_C = –55°C to +125°C	±15		±150	*		*	V
CURRENT, quiescent	T_C = 25°C		5.5	7.5		*	*	mA
THERMAL								
RESISTANCE, AC, junction to case[6]	T_C = –55°C to +125°C, F > 60Hz		3.8			*		°C/W
RESISTANCE, DC, junction to case	T_C = –55°C to +125°C, F < 60Hz		6	6.5		*	*	°C/W
RESISTANCE, case to air	T_C = –55°C to +125°C		30			*		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	–25		+85	*		*	°C

NOTES: * The specification of PA84A is identical to the specification for PA84/PA84S in applicable column to the left.

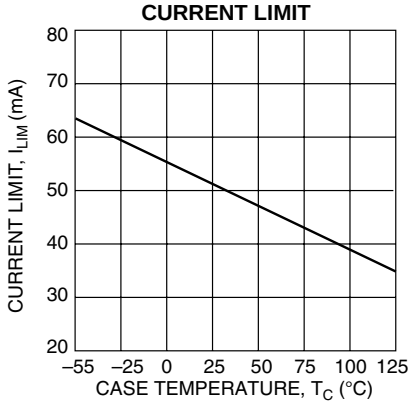
1. Signal slew rates at pins 5 and 6 must be limited to less than 1V/ns to avoid damage. When faster waveforms are unavoidable, resistors in series with those pins, limiting current to 150mA will protect the amplifier from damage.
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.
3. The power supply voltage for all tests is ±150V, unless otherwise noted as a test condition.
4. Doubles for every 10°C of temperature increase.
5. $+V_S$ and $-V_S$ denote the positive and negative power supply rail respectively.
6. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.

CAUTION The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

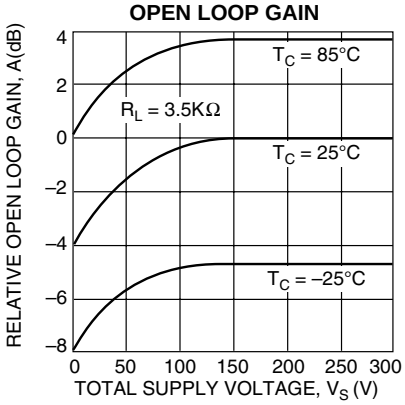
POWER DERATING



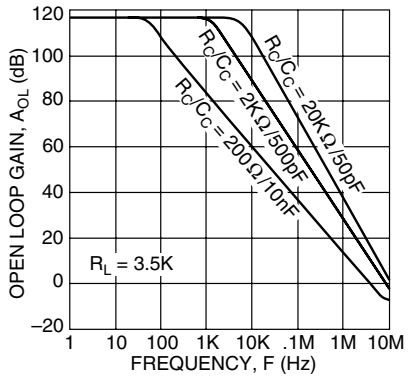
CURRENT LIMIT



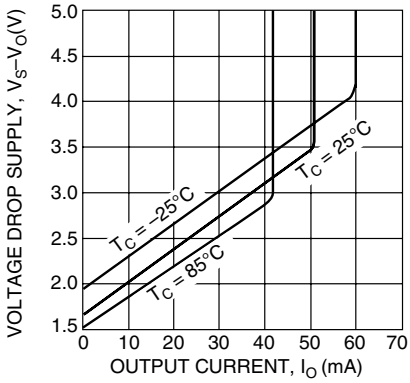
OPEN LOOP GAIN



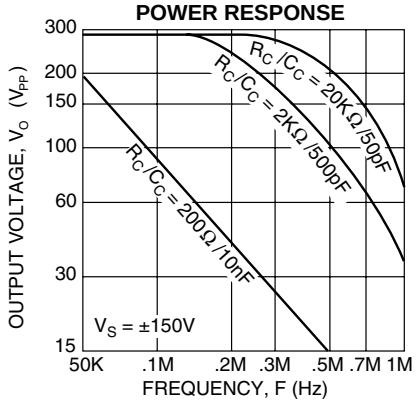
SMALL SIGNAL RESPONSE



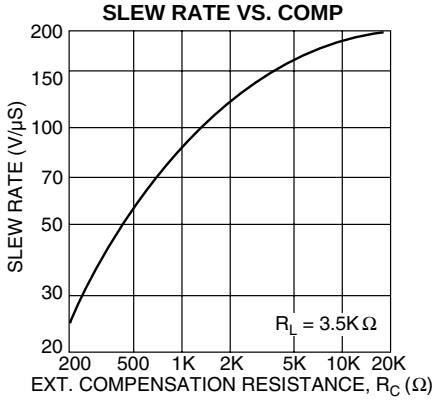
OUTPUT VOLTAGE SWING



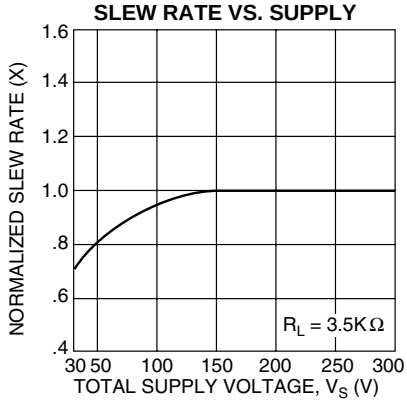
POWER RESPONSE



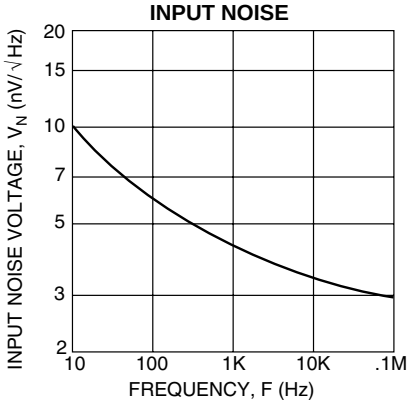
SLEW RATE VS. COMP



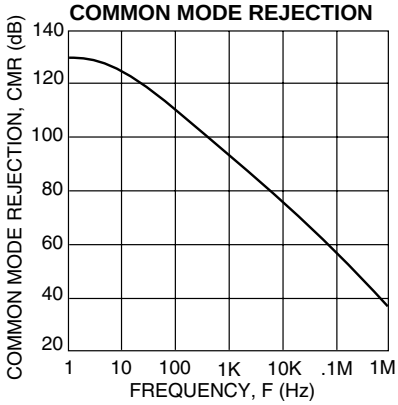
SLEW RATE VS. SUPPLY



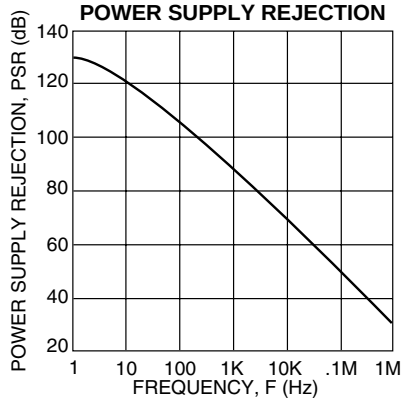
INPUT NOISE



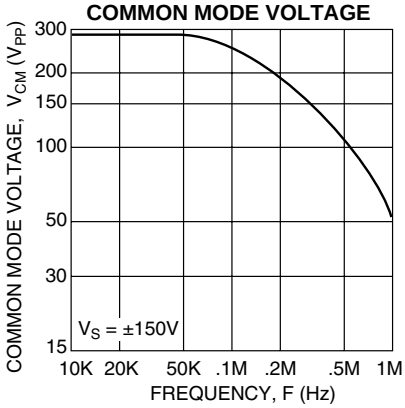
COMMON MODE REJECTION



POWER SUPPLY REJECTION



COMMON MODE VOLTAGE



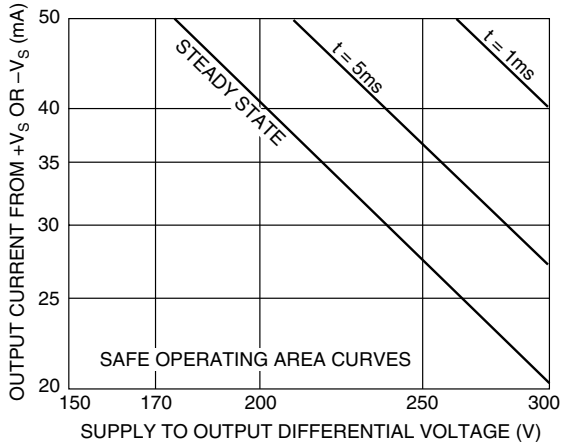
GENERAL

Please read the "General Operating Considerations" section, which covers stability, supplies, heatsinking, mounting, current limit, SOA interpretation, and specification interpretation. Additional information can be found in the application notes. For information on the package outline, heatsinks, and mounting hardware, consult the "Accessory and Package Mechanical Data" section of the handbook.

SAFE OPERATING AREA (SOA)

The bipolar output stage of this high voltage operational amplifier has two output limitations:

1. The internal current limit which limits maximum available output current.
2. The second breakdown effect, which occurs whenever the simultaneous collector current and collector-emitter voltage exceeds specified limits.



The SOA curves combine the effect of these limits. For a given application, the direction and magnitude of the output current should be calculated or measured and checked against the SOA curves. This is simple for resistive loads but more complex for reactive and EMF generating loads. However, the following guidelines may save extensive analytical efforts:

1. The following capacitive and inductive loads are safe:

$\pm V_S$	C(MAX)	L(MAX)
150V	1.2µF	.7H
125V	6.0µF	25H
100V	12µF	90H
75V	ALL	ALL

2. Short circuits to ground are safe with dual supplies up to ±150V or single supplies up to 150V.
3. Short circuits to the supply rails are safe with total supply voltages up to 150V (i.e. ±75V).

THERMAL SHUTDOWN PROTECTION

PA84S does not have this feature.

The thermal protection circuit shuts off the amplifier when the substrate temperature exceeds approximately 150°C. This allows heatsink selection to be based on normal operating conditions while protecting the amplifier against excessive junction temperatures during temporary fault conditions.

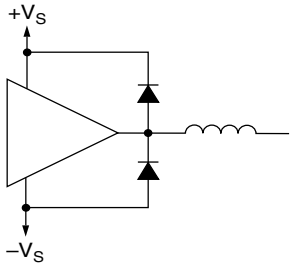
Thermal protection is a fairly slow-acting circuit and therefore does not protect the amplifier against transient SOA violations (areas outside of the T_C = 25°C boundary). It is designed to protect against short-term fault conditions that result in high power dissipation within the amplifier. If the conditions that cause thermal shutdown are not removed, the amplifier will oscillate in and out of shutdown. This will result in high peak power stresses, will destroy signal integrity, and reduce the reliability of the device.

OUTPUT PROTECTION

Two external diodes as shown in Figure 2, are required to protect these amplifiers against flyback (kickback) pulses exceeding the supply voltages of the amplifier when driving inductive loads. For component selection, these external diodes must be very quick, such as ultra fast recovery diodes with no more than 200 nanoseconds of reverse recovery time. Be sure the diode voltage rating is greater than the total of both supplies. The diode will turn on to divert the flyback energy into the supply rails thus protecting the output transistors from destruction due to reverse bias.

A note of caution about the supply. The energy of the flyback pulse must be absorbed by the power supply. As a result, a transient will be superimposed on the supply voltage, the magnitude of the transient being a function of its transient impedance and current sinking capability. If the supply voltage plus transient exceeds the maximum supply rating or if the AC impedance of the supply is unknown, it is best to clamp the output and the supply with a zener diode to absorb the transient.

FIGURE 1. PROTECTIVE, INDUCTIVE LOAD



STABILITY

Due to its large bandwidth the PA84 is more likely to oscillate than lower bandwidth Power Operational Amplifiers such as the PA83 or PA08. To prevent oscillations, a reasonable phase margin must be maintained by:

1. Selection of the proper phase compensation capacitor and resistor. Use the values given in the table under external connections and interpolate if necessary. The phase margin can be increased by using a large capacitor and a smaller resistor than the slew rate optimized values listed in the table. The compensation capacitor may be connected to common (in lieu of $+V_S$) if the positive supply is properly bypassed to common. Because the voltage at pin 8 is only a few volts below the positive supply, this ground connection requires the use of a high voltage capacitor.
2. Keeping the external sumpoint stray capacitance to ground at a minimum and the sumpoint load resistance (input and feedback resistors in parallel) below 500Ω. Larger sumpoint load resistance can be used with increased phase compensation (see 1 above).
3. Connecting the amplifier case to a local AC common thus preventing it from acting as an antenna.

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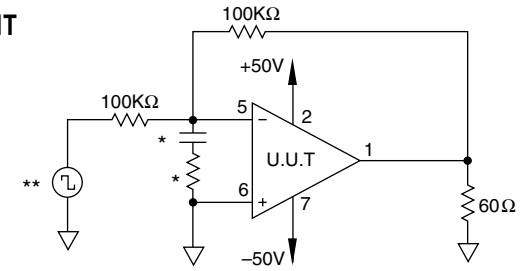
SG	PARAMETER	SYMBOL	TEMP.	POWER	TEST CONDITIONS	MIN	MAX	UNITS
1	Quiescent Current	I_Q	25°C	±150V	V_{IN} = 0, A_V = 100		7.5	mA
1	Input Offset Voltage	V_{OS}	25°C	±150V	V_{IN} = 0, A_V = 100		3	mV
1	Input Offset Voltage	V_{OS}	25°C	±15V	V_{IN} = 0, A_V = 100		5.7	mV
1	Input Bias Current, +IN	$+I_B$	25°C	±150V	V_{IN} = 0		50	pA
1	Input Bias Current, –IN	$–I_B$	25°C	±150V	V_{IN} = 0		50	pA
1	Input Offset Current	I_{OS}	25°C	±150V	V_{IN} = 0		50	pA
3	Quiescent Current	I_Q	–55°C	±150V	V_{IN} = 0, A_V = 100		9.5	mA
3	Input Offset Voltage	V_{OS}	–55°C	±150V	V_{IN} = 0, A_V = 100		5	mV
3	Input Offset Voltage	V_{OS}	–55°C	±15V	V_{IN} = 0, A_V = 100		7.7	mV
3	Input Bias Current, +IN	$+I_B$	–55°C	±150V	V_{IN} = 0		50	pA
3	Input BiasCurrent, –IN	$–I_B$	–55°C	±150V	V_{IN} = 0		50	pA
3	Input Offset Current	I_{OS}	–55°C	±150V	V_{IN} = 0		50	pA
2	Quiescent Current	I_Q	125°C	±150V	V_{IN} = 0, A_V = 100		9.5	mA
2	Input Offset Voltage	V_{OS}	125°C	±150V	V_{IN} = 0, A_V = 100		5.5	mV
2	Input Offset Voltage	V_{OS}	125°C	±15V	V_{IN} = 0, A_V = 100		8.2	mV
2	Input Bias Current, +IN	$+I_B$	125°C	±150V	V_{IN} = 0		10	nA
2	Input Bias Current, –IN	$–I_B$	125°C	±150V	V_{IN} = 0		10	nA
2	Input Offset Current	I_{OS}	125°C	±150V	V_{IN} = 0		10	nA
4	Output Voltage, I_O = 40mA	V_O	25°C	±47V	R_L = 1K	40		V
4	Output Voltage, I_O = 28.6mA	V_O	25°C	±150V	R_L = 5K	143		V
4	Output Voltage, I_O = 15mA	V_O	25°C	± 80V	R_L = 5K	75		V
4	Current Limits	I_{CL}	25°C	± 20V	R_L = 100Ω	36	70	mA
4	Stability/Noise	E_N	25°C	±150V	R_L = 5K, A_V = 1, C_L = 10nF		1	mV
4	Slew Rate	SR	25°C	±150V	R_L = 5K, C_C = 50pF	100	600	V/µs
4	Open Loop Gain	A_{OL}	25°C	±150V	R_L = 5k, F = 10Hz	100		dB
4	Common Mode Rejection	CMR	25°C	±32.5V	R_L = 5k, F = DC, V_{CM} = ±22.5V	90		dB
6	Output Voltage, I_O = 40mA	V_O	–55°C	±47V	R_L = 1K	40		V
6	Output Voltage, I_O = 28.6mA	V_O	–55°C	±150V	R_L = 5K	143		V
6	Output Voltage, I_O = 15mA	V_O	–55°C	±80V	R_L = 5K	75		V
6	Stability/Noise	E_N	–55°C	±150V	R_L = 5K, A_V = 1, C_L = 10nF		1	mV
6	Slew Rate	SR	–55°C	±150V	R_L = 5K, C_C = 50pF	100	600	V/µs
6	Open Loop Gain	A_{OL}	–55°C	±150V	R_L = 5K, F = 10Hz	100		dB
6	Common Mode Rejection	CMR	-55°C	±32.5V	R_L = 5k, F = DC, V_{CM} = ±22.5V	90		dB
5	Output Voltage, I_O = 30mA	V_O	125°C	±37V	R_L = 1K	30		V
5	Output Voltage, I_O = 28.6mA	V_O	125°C	±150V	R_L = 5K	143		V
5	Output Voltage, I_O = 15mA	V_O	125°C	±80V	R_L = 5K	75		V
5	Stability/Noise	E_N	125°C	±150V	R_L = 5 , A_V = 1, C_L = 10nF		1	mV
5	Slew Rate	SR	125°C	±150V	R_L = 5K, C_C = 50pF	100	600	V/µs
5	Open Loop Gain	A_{OL}	125°C	±150V	R_L = 5K, F = 10Hz	100		dB
5	Common Mode Rejection	CMR	125°C	±32.5V	R_L = 5k, F = DC, V_{CM} = ±22.5V	90		dB

BURN IN CIRCUIT



* These components are used to stabilize device due to poor high frequency characteristics of burn in board.

** Input signals are calculated to result in internal power dissipation of approximately 2.1W at case temperature = 125°C.

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