Pletronics, Inc.
19013 36th Ave. W, Suite H • Lynnwood, WA 98036 USA
Manufacturer of High Quality Frequency Control Products

Differential PECL Series

- Differential PECL Output, Some with Enable/ Disable Function
- Available in 9 Different Package/Configurations, See Next Pages

Standard Specifications

Overall Frequency Stability	± 50 PPM, ± 25 PPM, ± 20 PPM over Operating Temperature Range
Operating Temperature Range	0 to +80°C is standard, but can be extended to - 40 to +85°C
Storage Temperature Range	- 55 to +125°C
Supply Voltage (Vcc)	3.3 volts ± 5% standard, but 5.0 volts or 2.5 volts also available. See Test Cirucit 5.
Supply Current (Icc)	< 250 MHz = 90 mA maximum, 250 MHz and above = 100 mA maximum
Output High Level	2.275 V minimum referenced to Ground, Vcc = 3.300V, 0.975 V minimum referenced to termination voltage, - 1.025 V minimum referenced to Vcc
Output Low Level	1.680 V maximum referenced to Ground, Vcc = 3.300V, 0.380 V maximum referenced to termination voltage, - 1.620 V maximum referenced to Vcc
Output Symmetry	45/55% referenced to 50% of amplitude
Output Rise & Fall (Tr & Tf)	1.0 nS maximum when Vth is 10% and 90% of waveform
Jitter	1 pS RMS maximum measured from 12 kHz to 20 MHz from Fnominal
E/D Internal Pullup	50 kohm minimum to Vcc
V disable	0.3 Vcc maximum referenced to Ground
V enable	0.7 Vcc minumum referenced to Ground

PE7745D only Output Enable / Disable

High Level Input Current	-20 uA maximum at Enable / Disable Pin = 0.7 Vcc
Low Level Input Current	-200 uA maximum at Enable / Disable Pin = 0 V
Output Enable Time	200 nS maximum at output enable or 1 mS maximum at output enabled and stable
Output Disable Time	200 nS maximum at output disable

Vcc Supply Current disabled < 1 mA. Both outputs are high impedance when disabled.

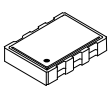
All other models Output Enable/Disable (E/D)

Output Enable Time	100 nS maximum
Output Disable Time	100 nS maximum
When Disabled	Q Output = Logic Low, QN Output = Logic High. Both Outputs are active

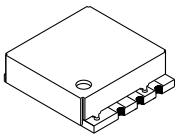
Note 1: PECL and ECL are identical circuits.
ECL has the most positive pin as ground and is ideally terminated by 50 ohms to - 2.00 V
PECL has the most negative pin as ground and is ideally terminated by 50 ohms to the most (positive voltage less 2.00 V)

Mechanical: See Next Pages

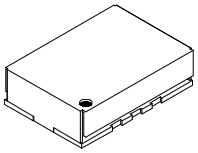
D Package



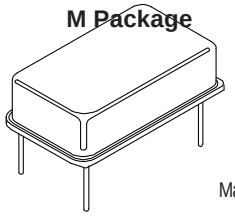
J Package Replacement



B Package



M Package



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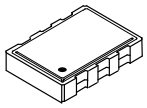
PE7745D PECL Series

- Differential PECL Output with Enable/ Disable Function
- 6 Pad 7x5mm Leadless Surface Mount Ceramic Clock Oscillator



40.00 MHz – 250.00 MHz

Part Numbering Guide

Portions of the part number that appear after the frequency may not be marked on part (C of C provided)

PE77 45 D V- 80.0M - XXX (Internal Code or blank)

Packaging
Tray or
16mm tape,
8mm pitch

Model
PE77 = E/D on pin 1
PE73 = E/D on pin 2

Frequency Stability
45 = ± 50 PPM
44 = ± 25 PPM
20 = ± 20 PPM

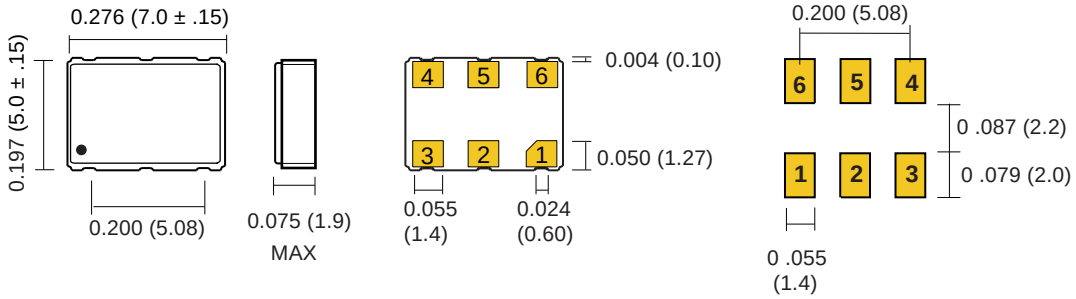
Frequency in MHz

Special Specifications (choose all that apply)
E: Extended Operating Temperature Range (- 40 to +85°C)
F: 47.5 /52.5% Symmetry at 50% of Vcc
V: Supply Voltage of 3.3 volts ± 10%
W: Supply Voltage of 2.5 volts ± 5%
Y: Supply Voltage of 5.0 volts ± 10%

Consult factory for available frequencies and specs. Not all options available for all frequencies. A special part number may be assigned.
Frequency Stability is inclusive of frequency shifts due to calibration, temperature, supply voltage, shock, vibration and load

Mechanical: inches (mm) not to scale Solder Pads

Due to part size and factory abilities, part marking may vary from lot to lot and may contain our part number or an internal code.



Lead Free

PE7745D

PIN	SIGNAL
1	E/D
2	N.C.
3	GND
4	Q OUT
5	QN OUT
6	Vcc

Preferred

PE7345D

PIN	SIGNAL
1	N.C.
2	E/D
3	GND
4	Q OUT
5	QN OUT
6	Vcc

See page 6 for Layout Guidelines

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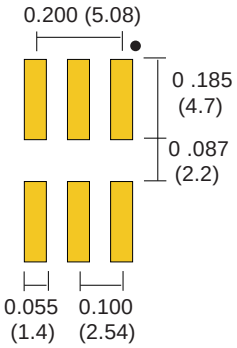
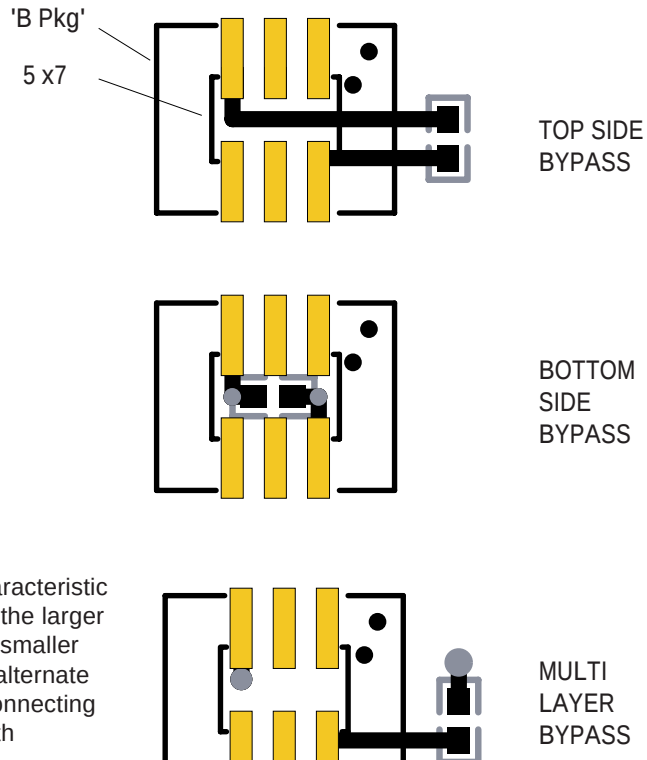
PECL and LVDS Layout Guidelines

SUGGESTED PCB LAYOUTS

Solder Pad Layout which accommodates all PECL surface mount devices



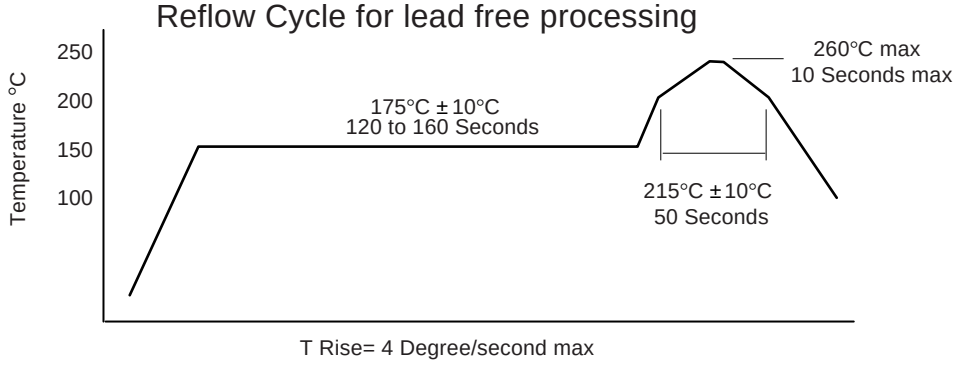


The output line should be designed with proper characteristic impedance. Pletronics recommends laying out for the larger 'B package' with pads long enough to accept the smaller 5 x 7mm device. This permits the best option for alternate sources of device. Pletronics also recommends connecting Pin 1 and Pin 2 together on the models with Q & QN OUT on pins 4 & 5. This allows having E/D on either pin 1 or pin 2.

For Optimum Jitter Performance, Pletronics recommends:

- A ground plane under the device with any other signals below the ground plane
- Minimize other RF signals near device
- No large transient signals (both current and voltage) should be routed under the device
- Do not layout near a large magnetic field such as a high frequency switching power supply
- Do not place near piezoelectric buzzers or mechanical fans

Reflow Cycle for lead free processing



T Rise= 4 Degree/second max

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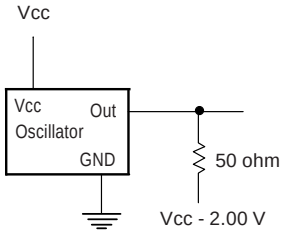
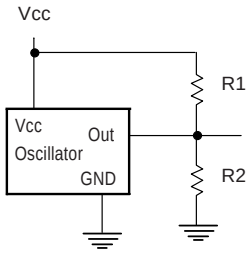
PECL and LVDS Layout Guidelines Continued

PECL Terminations:

Suggested Terminations for 50 ohm impedance matched termination

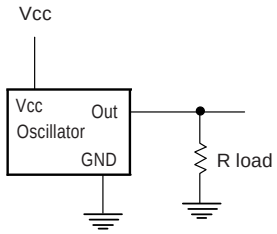




Thevenin Equivalent Termination

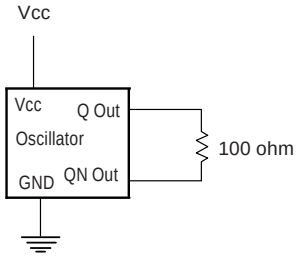
Vcc	R1	R2
5.0 V	82 ohm	130 ohm
3.3 V	130 ohm	82 ohm
2.5 V	249 ohm	61.9 ohm

Simple termination for NON impedance matched termination



Vcc	R load
5.0 V	274 ohm
3.3 V	147 ohm
2.5 V	86.6 ohm

LVDS Terminations:



Design PCB traces for 50 ohm characteristic impedance

Mixed System Power Supply:

PECL To use multiple supply voltages requires level translation. Direct circuit connection is not valid.

ECL Mixed supply voltages are allowed. No translation is necessary. (ECL is returned to the most positive supply and this is common to all circuits)

LVDS Mixed supply voltages are allowed. LVDS signal levels are power supply independent. 3.3 V LVDS oscillators properly interface 2.5 V Logic Arrays for example.

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