N-Channel 150-V (D-S) MOSFET

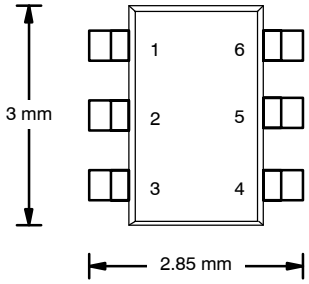
PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
150	0.375 @ V_{GS} = 10 V	1.5
	0.400 @ V_{GS} = 6.0 V	1.4

FEATURES

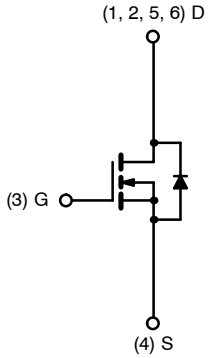
- TrenchFET® Power MOSFET
- PWM Optimized for Fast Switching In Small Footprint
- 100% R_g Tested

APPLICATIONS

- Primary Side Switch for Low Power DC/DC Converters



Ordering Information: Si3440DV-T1



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C UNLESS OTHERWISE NOTED)					
Parameter		Symbol	5 secs	Steady State	Unit
Drain-Source Voltage		V_{DS}	150		V
Gate-Source Voltage		V_{GS}	±20		
Continuous Drain Current (T_J = 175°C)[a]	T_A = 25°C	I_D	1.5	1.2	A
	T_A = 85°C		1.1	0.8	
Pulsed Drain Current		I_{DM}	6		
Single Avalanche Current	L = 0.1 mH	I_{AS}	4		
Single Avalanche Energy (Duty Cycle ≤ 1%)		E_{AS}	0.8		mJ
Continuous Source Current (Diode Conduction)[a]		I_S	1.7	1.0	A
Maximum Power Dissipation[a]	T_A = 25°C	P_D	2.0	1.14	W
	T_A = 85°C		1.0	0.59	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150		°C

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient[a]	t ≤ 5 sec	R_{thJA}	45	62.5	°C/W
	Steady State		90	110	
Maximum Junction-to-Foot (Drain)	Steady State	R_{thJF}	25	30	

Notes
a. Surface Mounted on 1" x 1" FR4 Board.

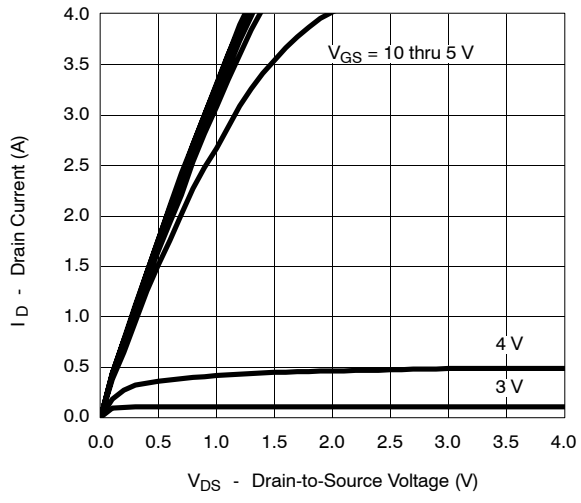
SPECIFICATIONS (T_J = 25°C UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA	2		4	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 150 V, V_{GS} = 0 V			1	μA
		V_{DS} = 150 V, V_{GS} = 0 V, T_J = 85°C			5	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} ≥ 5 V, V_{GS} = 10 V	4			A
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 1.5 A		0.310	0.375	Ω
		V_{GS} = 6.0 V, I_D = 1.4 A		0.330	0.400	
Forward Transconductance[a]	g_{fs}	V_{DS} = 15 V, I_D = 1.5 A		4.1		S
Diode Forward Voltage[a]	V_{SD}	I_S = 1.7 A, V_{GS} = 0 V		0.8	1.2	V
Dynamic[b]						
Total Gate Charge	Q_g	V_{DS} = 75 V, V_{GS} = 10 V, I_D = 1.5 A		5.4	8	nC
Gate-Source Charge	Q_{gs}			1.1		
Gate-Drain Charge	Q_{gd}			1.9		
Gate Resistance	R_g	f = 1 MHz	4	9	15	Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 75 V, R_L = 75 Ω I_D ≅ 1 A, V_{GEN} = 10 V, R_G = 6 Ω		8	15	ns
Rise Time	t_r			10	15	
Turn-Off Delay Time	$t_{d(off)}$			20	30	
Fall Time	t_f			15	25	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = 1.7 A, di/dt = 100 A/μs		40	60	ns

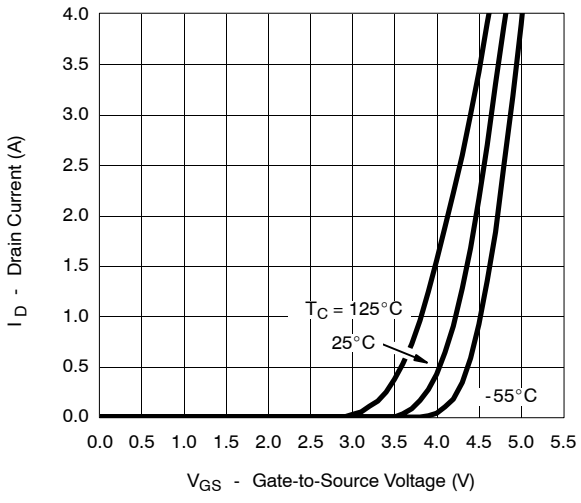
Notes
a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

Output Characteristics

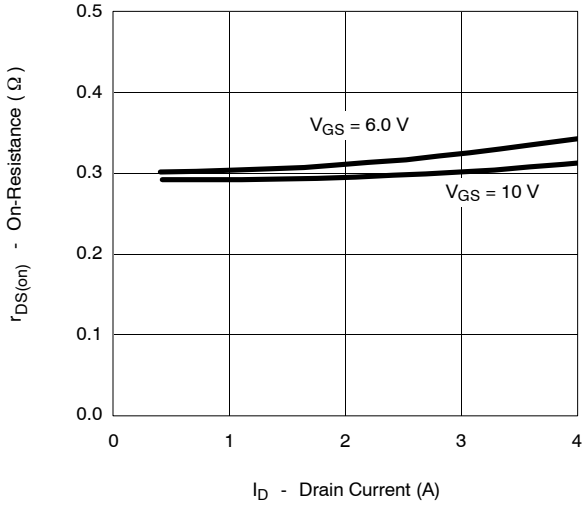


Transfer Characteristics

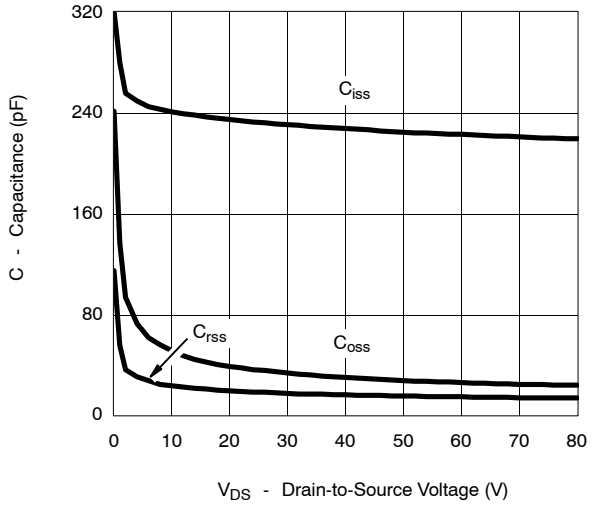


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

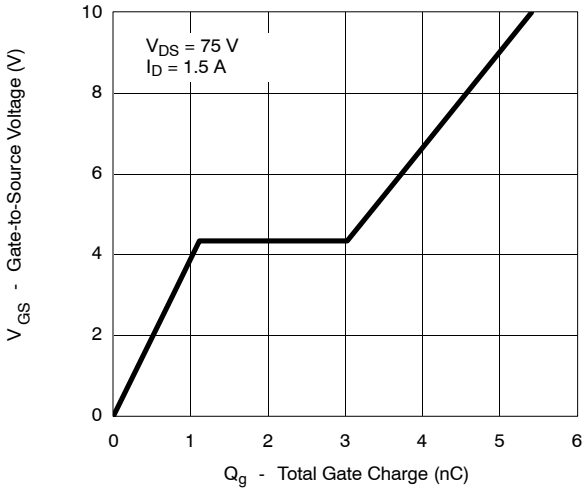
On-Resistance vs. Drain Current



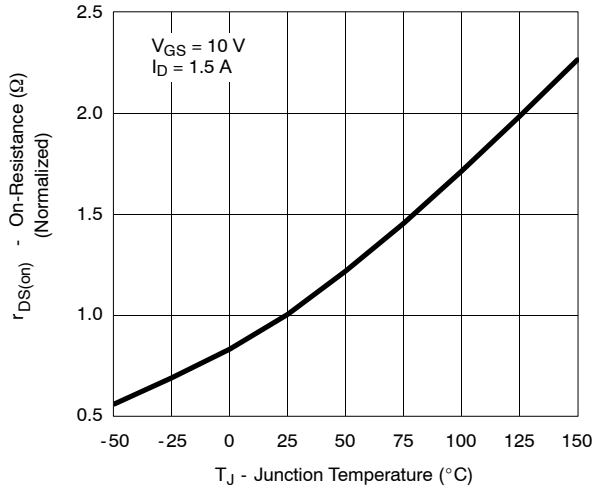
Capacitance



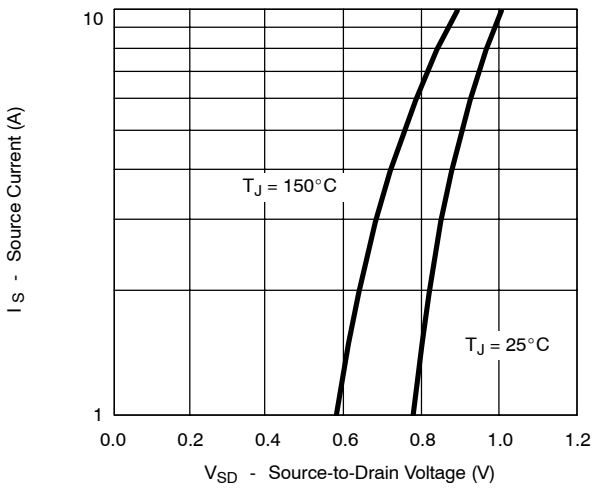
Gate Charge



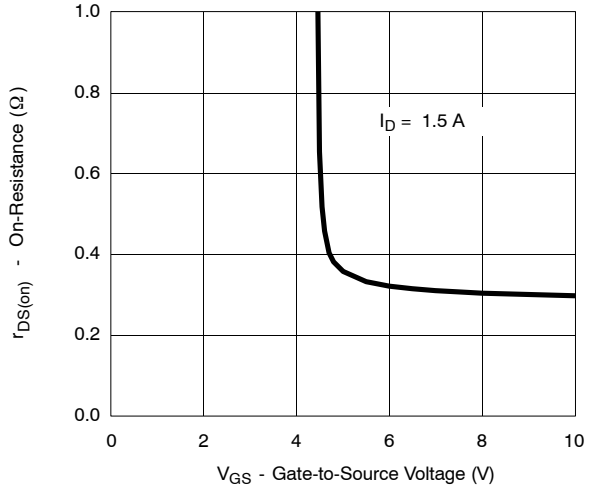
On-Resistance vs. Junction Temperature



Source-Drain Diode Forward Voltage

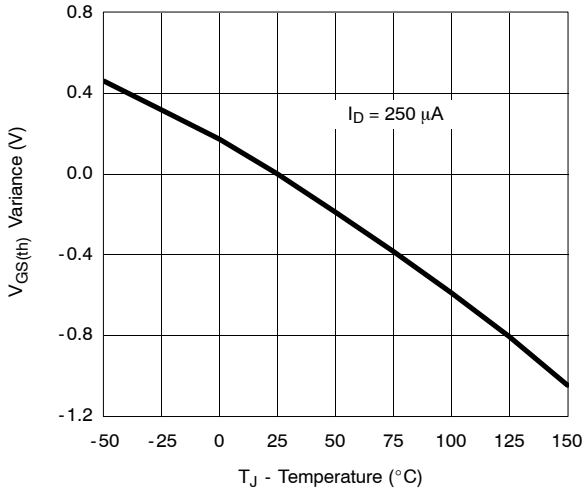


On-Resistance vs. Gate-to-Source Voltage

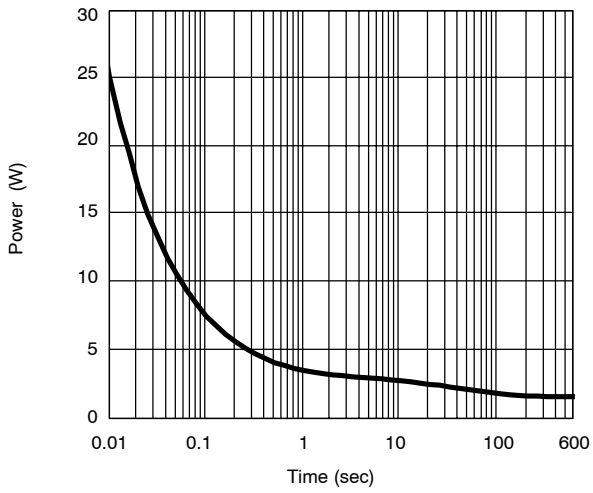


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

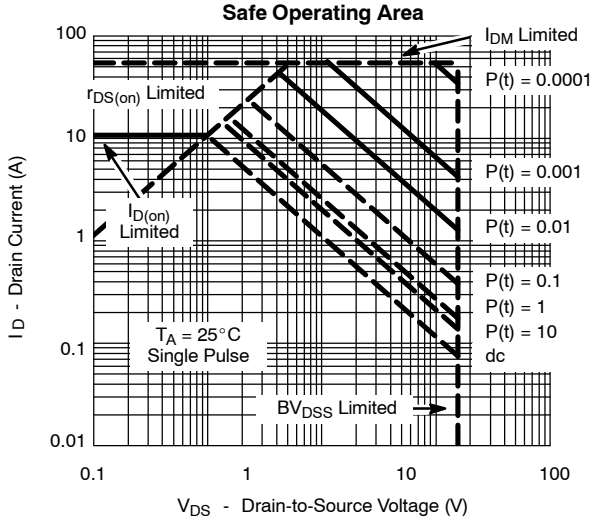
Threshold Voltage



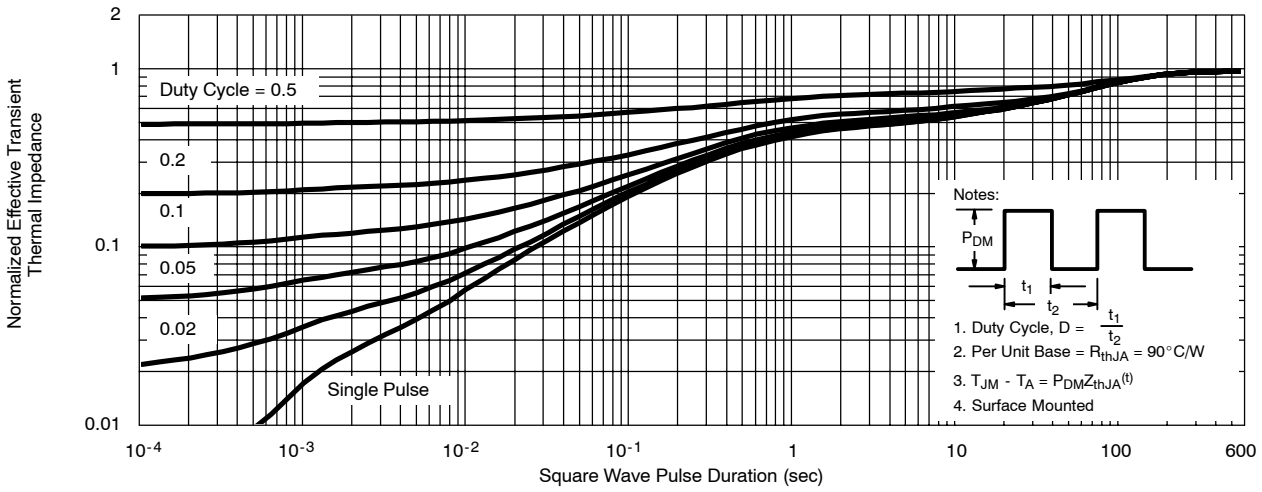
Single Pulse Power



Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient



TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)