

SRM20256LT_{10/12}

CMOS 256K-BIT STATIC RAM

• Industrial Temperature Range

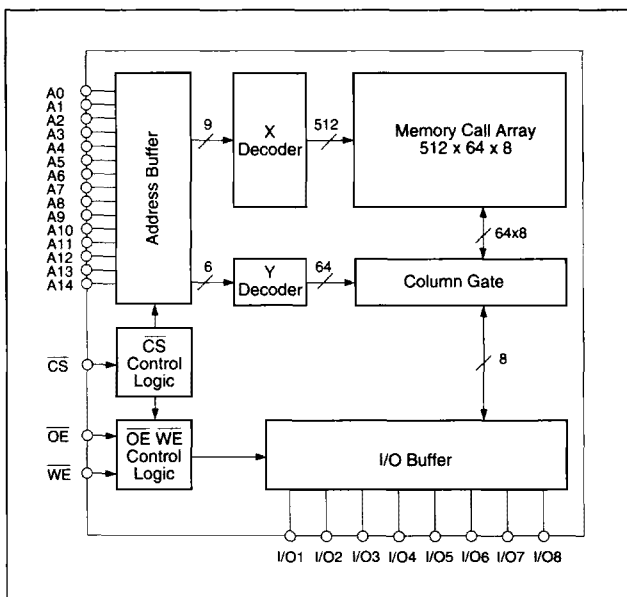
■ DESCRIPTION

The SRM20256LT_{10/12} is a 32,768 word x 8 bits asynchronous, static, random access memory fabricated using an advanced CMOS technology. Its very low standby power feature makes it ideal for applications requiring non-volatile storage with back-up batteries. And - 40 to 85°C operating temperature range makes it ideal for industrial use. The asynchronous and static nature of the memory requires no external clock or refresh circuit. Input and output ports are TTL compatible and the three-state output allows easy expansion of memory capacity.

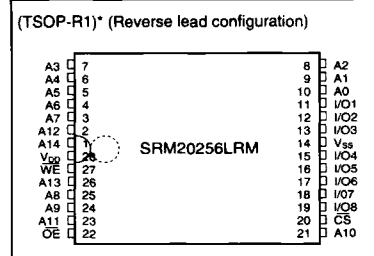
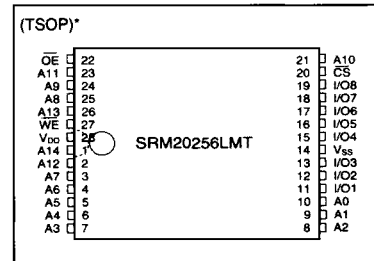
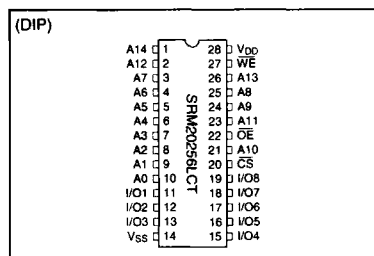
■ FEATURES

- Industrial temperature range - 40 to 85°C
- Fast access time SRM20256LT₁₀ 100ns (Max)
..... SRM20256LT₁₂ 120ns (Max)
- Low supply current Standby : 2μA (Typ)
..... Operation: 13mA/1MHz (Typ)
- Completely static No clock required
- Single power supply 5V ± 10%
- TTL compatible inputs and outputs
- 3-state output
- Battery back-up operation
- Package SRM20256LCT_{10/12} 28-pin DIP (plastic)
..... SRM20256LMT_{10/12} 28-pin TSOP (plastic)
..... SRM20256LTMT_{10/12} 28-pin TSOP (plastic)
..... SRM20256LRMT_{10/12} 28-pin RTSOP (plastic)

■ BLOCK DIAGRAM



■ PIN CONFIGURATION



■ PIN DESCRIPTION

- A0 to A14 Address Input
- WE Write enable
- OE Output Enable
- CS Chip Select
- I/O1 to 8 Data I/O
- VDD Power Supply (+5V)
- VSS Power Supply (0V)

■ ABSOLUTE MAXIMUM RATINGS

(V_{SS}=0V)

Parameter	Symbol	Ratings	Unit
Supply voltage	V _{DD}	-0.5 to 7.0	V
Input voltage *	V _I	-0.5 to 7.0	V
Input/Output voltage*	V _{I/O}	-0.5* to V _{DD} +0.3	V
Power dissipation	P _D	1.0	W
Operating temperature	T _{opr}	-40 to 85	°C
Storage temperature	T _{stg}	-65 to 150	°C
Soldering temperature and time	T _{sol}	260°C, 10s (at lead)	—

* V_I, V_{I/O} (Min) = -1.0V when pulse width is less than or equal to 50 ns

■ RECOMMENDED DC OPERATING CONDITIONS

(V_{SS}=0V, T_a = -40 to 85°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{DD}	4.5	5.0	5.5	V
	V _{SS}	0	0	0	V
Input Voltage	V _{IH}	2.2	3.5	V _{DD} + 0.3	V
	V _{IL}	-0.3 *	—	0.8	V

* V_{IL} (Min) = -1.0V when pulse width is less than or equal to 50ns

■ ELECTRICAL CHARACTERISTICS

● DC Electrical Characteristics

(V_{DD} = 5V ± 10%, V_{SS} = 0V, T_a = -40 to 85°C)

Parameter	Symbol	Conditions	SRM20256LT10			SRM20256LT12			Unit
			Min	Typ*	Max	Min	Typ*	Max	
Input leakage current	I _{LI}	V _I = 0 to V _{DD}	-1	—	1	-1	—	1	μA
Standby supply current	I _{DDS}	$\overline{CS} = V_{IH}$	—	1.5	3.0	—	1.5	3.0	mA
	I _{DDS1}	$\overline{CS} \geq V_{DD} - 0.2V$	—	2	200	—	2	200	μA
Average operating current	I _{DDA}	V _I =V _{IL} , V _{IH} , I _{I/O} = 0mA, t _{cyc} =Min	—	40	70	—	37	70	mA
	I _{DDA1}	V _I =V _{IL} , V _{IH} , I _{I/O} = 0mA, t _{cyc} =1μs	—	13	—	—	13	—	mA
Operating supply current	I _{DDO}	V _I =V _{IL} , V _{IH} , I _{I/O} = 0mA	—	35	65	—	35	65	mA
Output leakage current	I _{LO}	$\overline{CS} = V_{IH}$, or $\overline{WE} = V_{IL}$, or $\overline{OE} = V_{IH}$, V _{I/O} = 0 to V _{DD}	-1	—	1	-1	—	1	μA
High level output voltage	V _{OH}	I _{OH} =-1.0mA	2.4	V _{DD} -0.1	—	2.4	V _{DD} -0.1	—	V
Low level output voltage	V _{OL}	I _{OL} =2.1mA	—	0.2	0.4	—	0.2	0.4	V

● Terminal Capacitance

(f = 1MHz, T_a = 25°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Address capacitance	C _{ADD}	V _{ADD} = 0V	—	—	10	pF
Input capacitance	C _I	V _I = 0V	—	—	10	pF
I/O capacitance	C _{I/O}	V _{I/O} = 0V	—	—	10	pF

● AC Electrical Characteristics

O Read Cycle

(V_{DD} = 5V ± 10%, V_{SS} = 0V, T_a = -40 to 85°C)

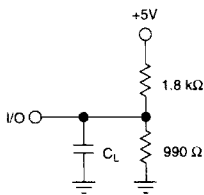
Parameter	Symbol	Conditions	SRM2264L10		SRM2264L12		Unit
			Min	Max	Min	Max	
Read cycle time	t _{RC}	*1	100	—	120	—	ns
Address access time	t _{ACC}		—	100	—	120	ns
CS access time	t _{ACS}		—	100	—	120	ns
OE access time	t _{OE}		—	50	—	60	ns
CS output set time	t _{CLZ}	*2	10	—	10	—	ns
CS output floating time	t _{CHZ}		—	35	—	40	ns
OE output set time	t _{OLZ}		5	—	5	—	ns
OE output floating time	t _{OHZ}		—	35	—	40	ns
Output hold time	t _{OH}	*1	10	—	10	—	ns

O Write Cycle(V_{DD} = 5V ± 10%, V_{SS} = 0V, T_a = -40 to 85°C)

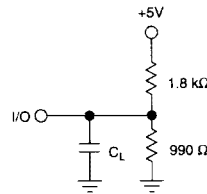
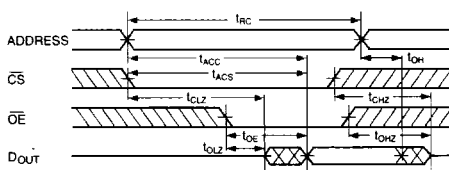
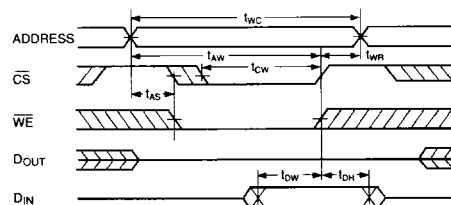
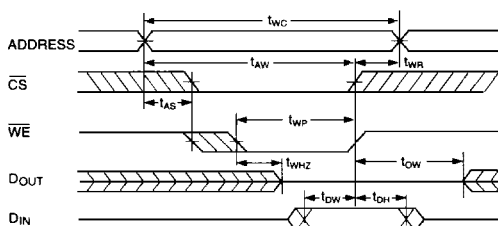
Parameter	Symbol	Conditions	SRM20256LC10		SRM20256LC12		Unit
			Min	Max	Min	Max	
Write cycle time	t _{WC}	*1	100	—	120	—	ns
Chip select time	t _{CW}		80	—	85	—	ns
Address valid to end of write	t _{AW}		80	—	85	—	ns
Address setup time	t _{AS}		0	—	0	—	ns
Write pulse width	t _{WP}		75	—	80	—	ns
Address hold time	t _{WR}		5	—	5	—	ns
Input data set time	t _{DW}		45	—	50	—	ns
Input data hold time	t _{DH}		0	—	0	—	ns
Write to output floating	t _{WHZ}	*2	—	35	—	40	ns
Output active from end of write	t _{OW}		5	—	5	—	ns

***1 Test conditions**

1. Input pulse level: 0.6V to 2.4V
2. t_r = t_f = 5ns
3. Input and output timing reference levels: 1.5V
4. Output load C_L = 100pF

C_L = 100pF (Includes Jig Capacitance)***2 Test conditions**

1. Input pulse level : 0.6V to 2.4V
2. t_r = t_f = 5ns
3. Input timing reference levels: 1.5V
4. Output timing reference levels: ±200mV (the level displaced from stable output voltage level)
5. Output load C_L = 5pF

C_L = 5pF (Includes Jig Capacitance)**● Timing Chart****Read Cycle****Write Cycle (1) (CS Control)****Write Cycle (2) (WE Control)****Note:**

1. During read cycle time, $\overline{WE}$ is to be "H" level.
2. Write cycle time is controlled by CS. Output Buffer is in high impedance state, whether $\overline{OE}$ is "H" or "L".
3. Write cycle time that is controlled by WE, Output Buffer is in high impedance state.

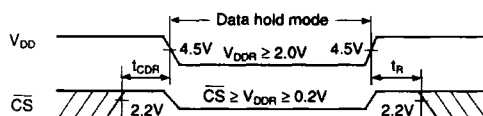
■ DATA RETENTION CHARACTERISTICS WITH LOW VOLTAGE POWER SUPPLY

(V_{SS} = 0V, T_a = -40 to 85°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data retention supply voltage	V _{DDR}		2.0	—	5.5	V
Data retention supply current	I _{DDR}	V _{DD} = 3V, CS ≥ V _{DDR} - 0.2V	—	1	100	μA
Chip select data hold time	t _{CDR}		0	—	—	ns
Operation recovery time	t _R		t _{RC} *	—	—	ns

* t_{RC} = Read cycle time

Data retention timing



■ FUNCTIONS

● Truth Table

CS	OE	WE	A0 to A14	DATA I/O	MODE	I _{DD}
H	—	—	—	Hi-Z	Standby	I _{DD} S, I _{DD} S1
L	X	L	Stable	D _{IN}	Write	I _{DD} A, I _{DD} A1
L	L	H	Stable	D _{OUT}	Read	I _{DD} A, I _{DD} A1
L	H	H	Stable	Hi-Z	Output disable	I _{DD} A, I _{DD} A1

X : "H" or "L"

● Reading Data

Data can be read out if an address is set while $\overline{\text{CS}}$ = "L", $\overline{\text{OE}}$ = "L", and $\overline{\text{WE}}$ = "H". When $\overline{\text{OE}}$ = "H", Data I/O terminals are in high impedance state; that makes it easy to circuit design and bus control.

● Writing Data

There are the following three ways of writing data into the memory.

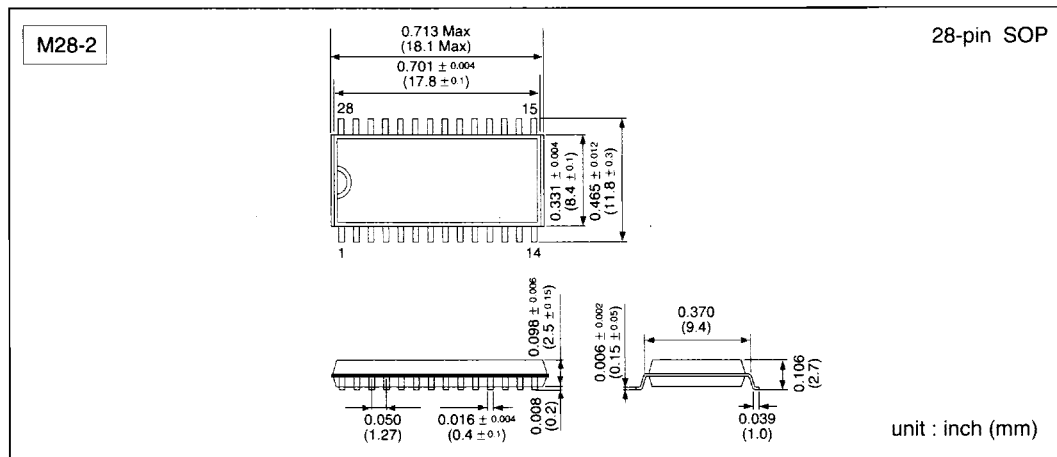
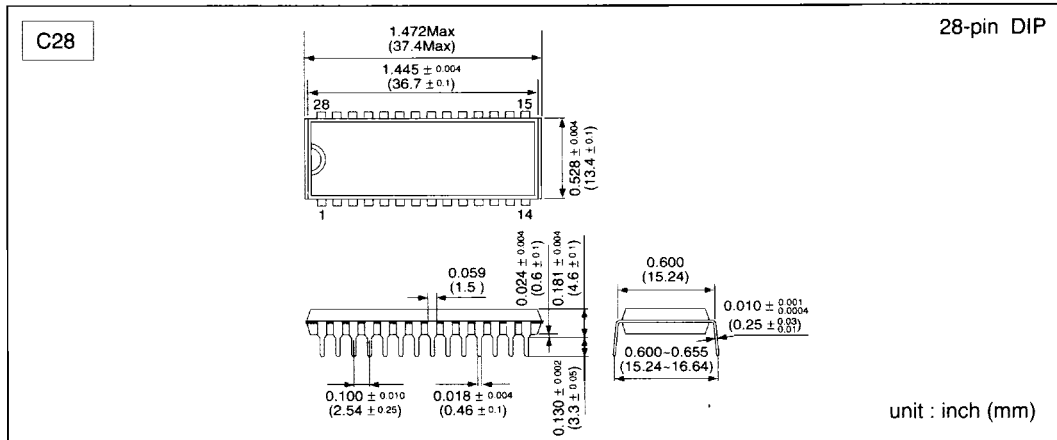
- (1) Hold $\overline{\text{CS}}$ low, set the address, and apply a low pulse to $\overline{\text{WE}}$.
- (2) Hold $\overline{\text{R/W}}$ low, set the address, and apply a low pulse to $\overline{\text{WE}}$.
- (3) Set the address, then apply low pulses to both $\overline{\text{CS}}$ and $\overline{\text{WE}}$.

In each case, data from the DATA I/O terminal is latched into the SRM20256LT10/12 when $\overline{\text{CS}}$ or $\overline{\text{WE}}$ is positive. Since DATA I/O terminals are in high impedance state when $\overline{\text{CS}}$ or $\overline{\text{OE}}$ = "H", the contention on the data bus can be avoided.

● Standby Mode

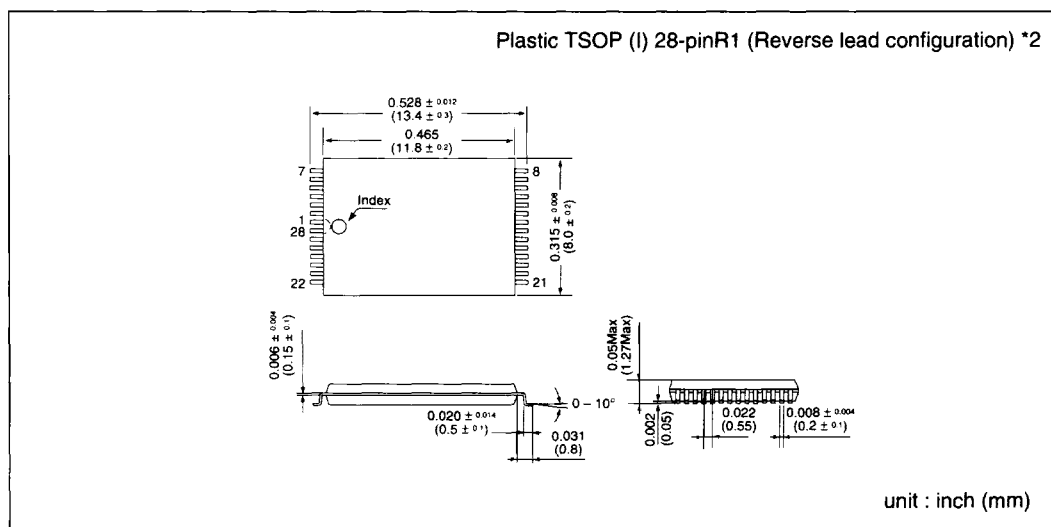
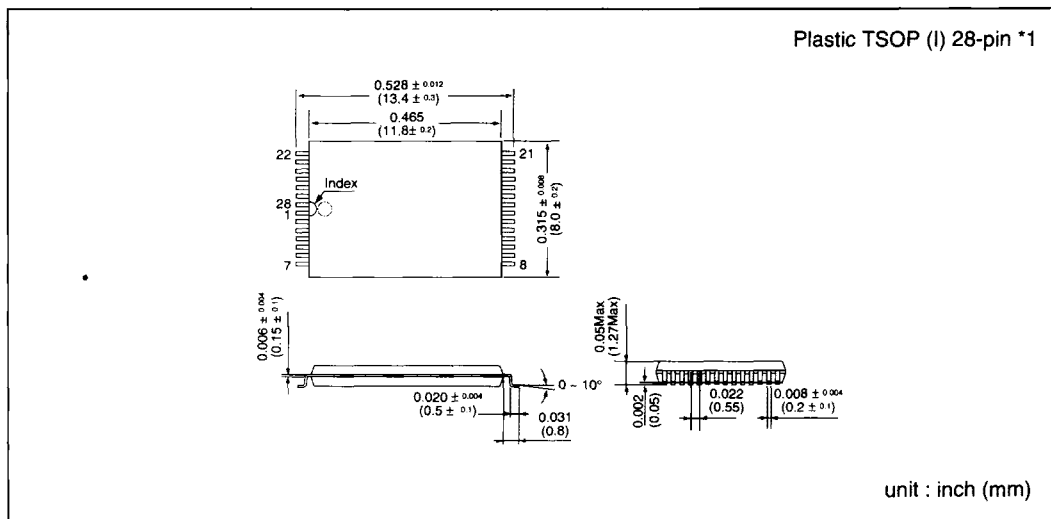
When $\overline{\text{CS}}$ is high, SRM20256LT10/12 is in the stand-by mode. In this case Data I/O terminals are in Hi-Z, so that all inputs of addresses, $\overline{\text{WE}}$ and data can be any "H" or "L". When $\overline{\text{CS}}$ is over V_{DD} - 0.2V, the SRM20256LT10/12 is in the data retention battery back-up mode. In this mode, there is a small current in the SRM20256LT10/12 which flows through the high resistances of the memory cells.

■ PACKAGE DIMENSIONS



* SRM20256LMT10/12 has the same electrical characteristics as SRM20256LCT10/12.

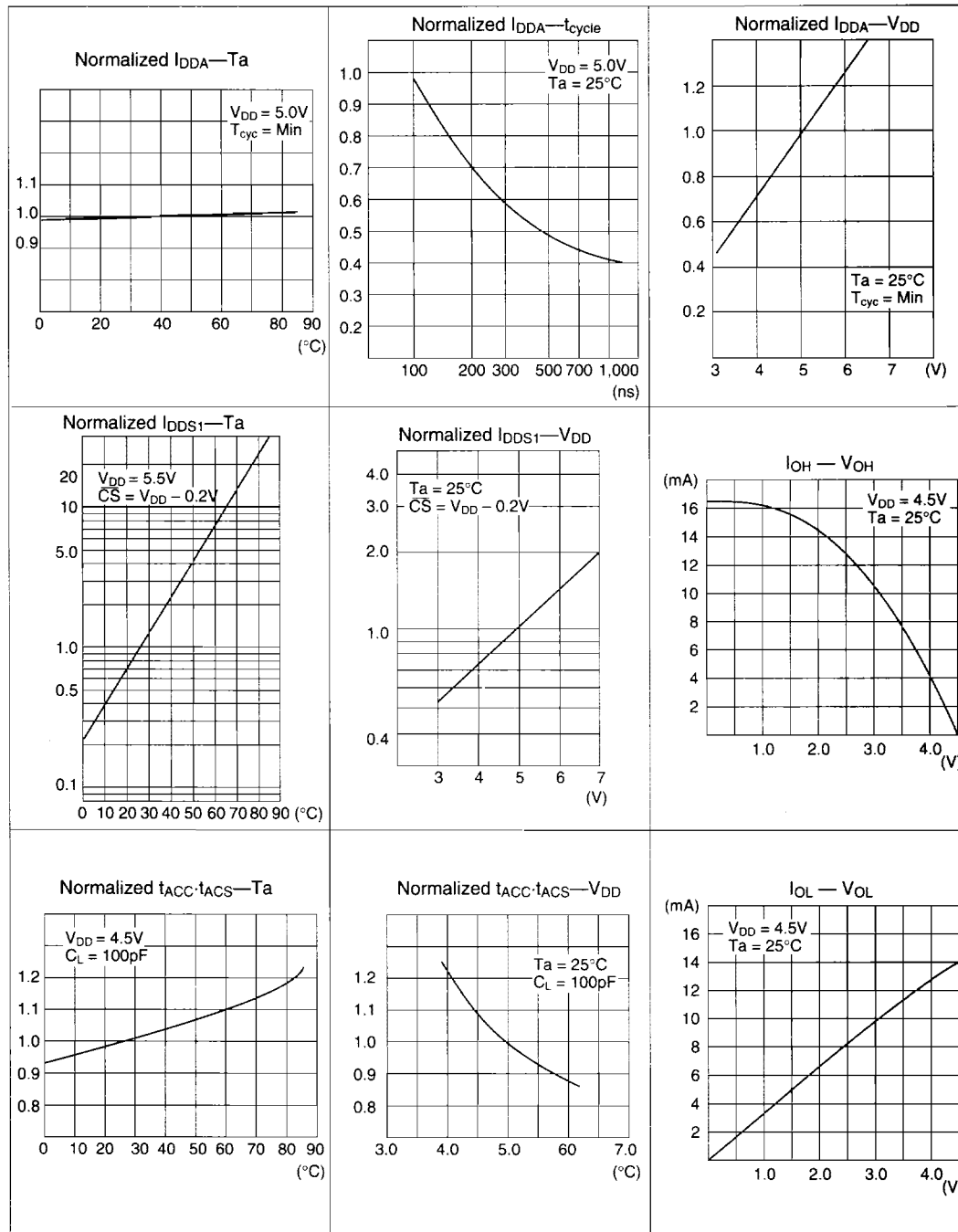
■ PACKAGE DIMENSIONS



* 1 SRM20256LTM10/12 has the same electrical characteristics as SRM20256LC10/12.

* 2 SRM20256LRM10/12 has the same electrical characteristics as SRM20256LC10/12.

■ CHARACTERISTICS CURVES



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