DATA SHEET

74LVC1GU04
Inverter

Product specification
Supersedes data of 2000 Dec 12
File under Integrated Circuits, IC24

2001 Apr 06

Philips Semiconductors

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FEATURES

- Wide supply voltage range from 1.65 to 5.5 V
- High noise immunity
- Complies with JEDEC standard:
  - JESD8-7 (1.65 to 1.95 V)
  - JESD8-5 (2.3 to 2.7 V)
  - JESD8B/JESD36 (2.7 to 3.6 V).
- ±24 mA output drive (V_{CC} = 3.0 V)
- CMOS low power consumption
- Latch-up performance exceeds 250 mA
- Input accepts voltages up to 5 V
- SOT353 package.

DESCRIPTION

The 74LVC1GU04 is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

The input can be driven from either 3.3 or 5 V devices. This feature allows the use of this device in a mixed 3.3 and 5 V environment.

The 74LVC1GU04 provides the inverting single state unbuffered function.

QUICK REFERENCE DATA

Ground = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 2.5$ ns.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay A to Y	V_{CC} = 1.8 V; C_L = 30 pF; R_L = 1 kΩ	1.7	ns
		V_{CC} = 2.5 V; C_L = 30 pF; R_L = 500 Ω	1.3	ns
		V_{CC} = 3.3 V; C_L = 50 pF; R_L = 500 Ω	1.6	ns
		V_{CC} = 5.0 V; C_L = 50 pF; R_L = 500 Ω	1.3	ns
C_I	input capacitance		6	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	14.9	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz;
   f_o = output frequency in MHz;
   C_L = output load capacitance in pF;
   V_{CC} = supply voltage in Volts.
2. The condition is V_I = GND to V_{CC}.

FUNCTION TABLE

See note 1.

INPUT	OUTPUT
A	**Y**
L	H
H	L

Note

1. H = HIGH voltage level;
   L = LOW voltage level.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE					
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE	MARKING
74LVC1GU04GW	–40 to +85 °C	5	SC-88A	plastic	SOT353	VD

PINNING

PIN	SYMBOL	DESCRIPTION
1	n.c.	not connected
2	A	data input A
3	GND	ground (0 V)
4	Y	data output Y
5	V_{CC}	supply voltage

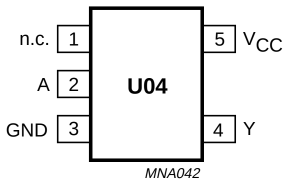


Fig.1 Pin configuration.

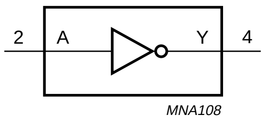


Fig.2 Logic symbol.

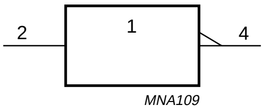


Fig.3 IEE/IEC logic symbol.

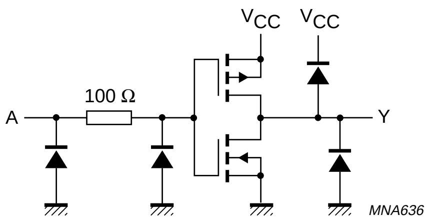


Fig.4 Logic diagram.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		1.65	5.5	V
V_I	input voltage		0	5.5	V
V_O	output voltage		0	V_{CC}	V
T_{amb}	operating ambient temperature		–40	+85	°C
t_r, t_f	input rise and fall times	V_{CC} = 1.65 to 2.7 V	0	20	ns/V
		V_{CC} = 2.7 to 5.5 V	0	10	ns/V

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		–0.5	+6.5	V
I_{IK}	input diode current	$V_I < 0$	–	–50	mA
V_I	input voltage	note 1	–0.5	+6.5	V
I_{OK}	output diode current	$V_O > V_{CC}$ or $V_O < 0$	–	±50	mA
V_O	output voltage	note 1	–0.5	V_{CC} + 0.5	V
I_O	output source or sink current	V_O = 0 to V_{CC}	–	±50	mA
I_{CC}, I_{GND}	V_{CC} or GND current		–	±100	mA
T_{stg}	storage temperature		–65	+150	°C
P_D	power dissipation per package	for temperature range from –40 to +85 °C; note 2	–	200	mW

Notes

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. Above 55 °C the value of P_D derates linearly with 2.5 mW/K.

DC CHARACTERISTICS

At recommended operating conditions; voltage are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		T_{amb} (°C) –40 to +85			UNIT
		OTHER	V_{CC} (V)	MIN.	TYP.[1]	MAX.	
V_{IH}	HIGH-level input voltage		1.65 to 5.5	$0.75 \times V_{CC}$	–	–	V
V_{IL}	LOW-level input voltage		1.65 to 5.5	–	–	$0.25 \times V_{CC}$	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}; $I_O = 100$ μA	1.65 to 5.5	–	–	0.1	V
		$V_I = V_{IH}$ or V_{IL}; $I_O = 4$ mA	1.65	–	–	0.45	V
		$V_I = V_{IH}$ or V_{IL}; $I_O = 8$ mA	2.3	–	–	0.3	V
		$V_I = V_{IH}$ or V_{IL}; $I_O = 12$ mA	2.7	–	–	0.4	V
		$V_I = V_{IH}$ or V_{IL}; $I_O = 24$ mA	3.0	–	–	0.55	V
		$V_I = V_{IH}$ or V_{IL}; $I_O = 32$ mA	4.5	–	–	0.55	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}; $I_O = -100$ μA	1.65 to 5.5	$V_{CC} - 0.1$	–	–	V
		$V_I = V_{IH}$ or V_{IL}; $I_O = -4$ mA	1.65	1.2	–	–	V
		$V_I = V_{IH}$ or V_{IL}; $I_O = -8$ mA	2.3	1.9	–	–	V
		$V_I = V_{IH}$ or V_{IL}; $I_O = -12$ mA	2.7	2.2	–	–	V
		$V_I = V_{IH}$ or V_{IL}; $I_O = -24$ mA	3.0	2.3	–	–	V
		$V_I = V_{IH}$ or V_{IL}; $I_O = -32$ mA	4.5	3.8	–	–	V
I_{LI}	input leakage current	$V_I = 5.5$ V or GND	3.6	–	±0.1	±5	μA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; $I_O = 0$	5.5	–	0.1	10	μA

Note

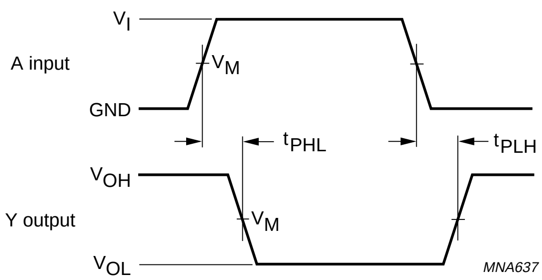
1. All typical values are measured at $V_{CC} = 3.3$ V and $T_{amb} = 25$ °C.

AC CHARACTERISTICS

GND = 0 V; $t_r = t_f \leq 2.0$ ns.

SYMBOL	PARAMETER	TEST CONDITIONS		T_{amb} (°C)			UNIT
		WAVEFORMS	V_{CC} (V)	−40 to +85			
				MIN.	TYP.	MAX.	
t_{PHL}/t_{PLH}	propagation delay A to Y	see Figs 5 and 8	1.65 to 1.95	0.3	1.7	5.0	ns
			2.3 to 2.7	0.3	1.3	4.0	ns
			2.7	0.5	1.7	5.0	ns
			3.0 to 3.6	0.5	1.6	3.7	ns
			4.5 to 5.5	0.5	1.3	3.0	ns

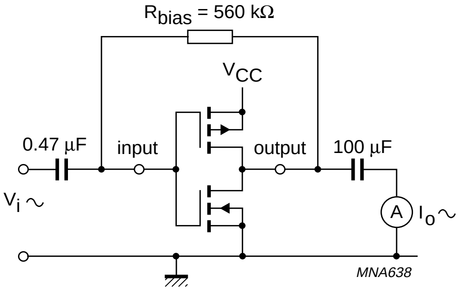
AC WAVEFORMS



V_{CC}	V_M	INPUT	
		V_I	$t_r = t_f$
1.65 to 1.95 V	$0.5 \times V_{CC}$	V_{CC}	≤ 2.0 ns
2.3 to 2.7 V	$0.5 \times V_{CC}$	V_{CC}	≤ 2.0 ns
2.7 V	1.5 V	2.7 V	≤ 2.5 ns
3.0 to 3.6 V	1.5 V	2.7 V	≤ 2.5 ns
4.5 to 5.5 V	$0.5 \times V_{CC}$	V_{CC}	≤ 2.5 ns

V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig.5 Input A to output Y propagation delay times.

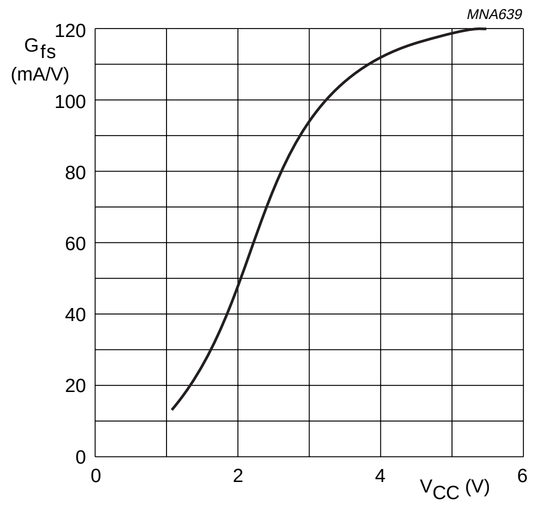


$$G_{fs} = \frac{\Delta I_o}{\Delta V_i}$$

f_i = 1 kHz.

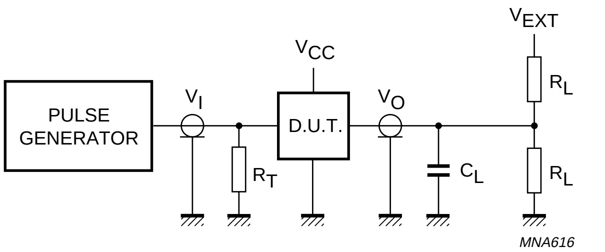
V_O is constant.

Fig.6 Test set-up for measuring forward transconductance.



T_{amb} = 25 °C.

Fig.7 Typical forward transconductance as a function of supply voltage.



V_{CC}	V_I	C_L	R_L	V_{EXT}		
				t_{PLH}/t_{PHL}	t_{PZH}/t_{PHZ}	t_{PZL}/t_{PLZ}
1.65 to 1.95 V	V_{CC}	30 pF	1 kΩ	open	GND	2 × V_{CC}
2.3 to 2.7 V	V_{CC}	30 pF	500 Ω	open	GND	2 × V_{CC}
2.7 V	2.7 V	50 pF	500 Ω	open	GND	6 V
3.0 to 3.6 V	2.7 V	50 pF	500 Ω	open	GND	6 V
4.5 to 5.5 V	V_{CC}	50 pF	500 Ω	open	GND	2 × V_{CC}

Definitions for test circuit:

R_L = Load resistor.

C_L = Load capacitance including jig and probe capacitance (see Chapter “AC characteristics”).

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig.8 Load circuitry for switching times.

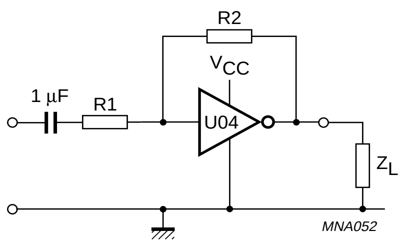
APPLICATION INFORMATION

Some applications for the 74LVC1GU04 are:

- Linear amplifier (see Fig.9)
- Crystal oscillator (see Fig.10).

Remark to the application information.

All values given are typical values unless otherwise specified.



Z_L > 10 kΩ, R1 ≥ 3 kΩ and R2 ≤ 1 MΩ.

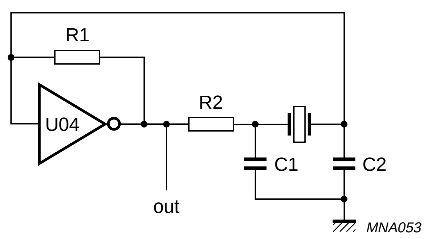
Open loop amplification: A_{OL} = 20 (typical value).

Voltage amplification: $A_u = -\frac{A_{OL}}{1 + \frac{R1}{R2}(1 + A_{OL})}$

Maximum output voltage: $V_{o(p\text{-}p)} \approx V_{CC} - 1.5$ V centered at $0.5V_{CC}$

Unity gain bandwidth product: B = 5 MHz (typical value).

Fig.9 Used as a linear amplifier.



C1 = 47 pF (typical).

C2 = 22 pF (typical).

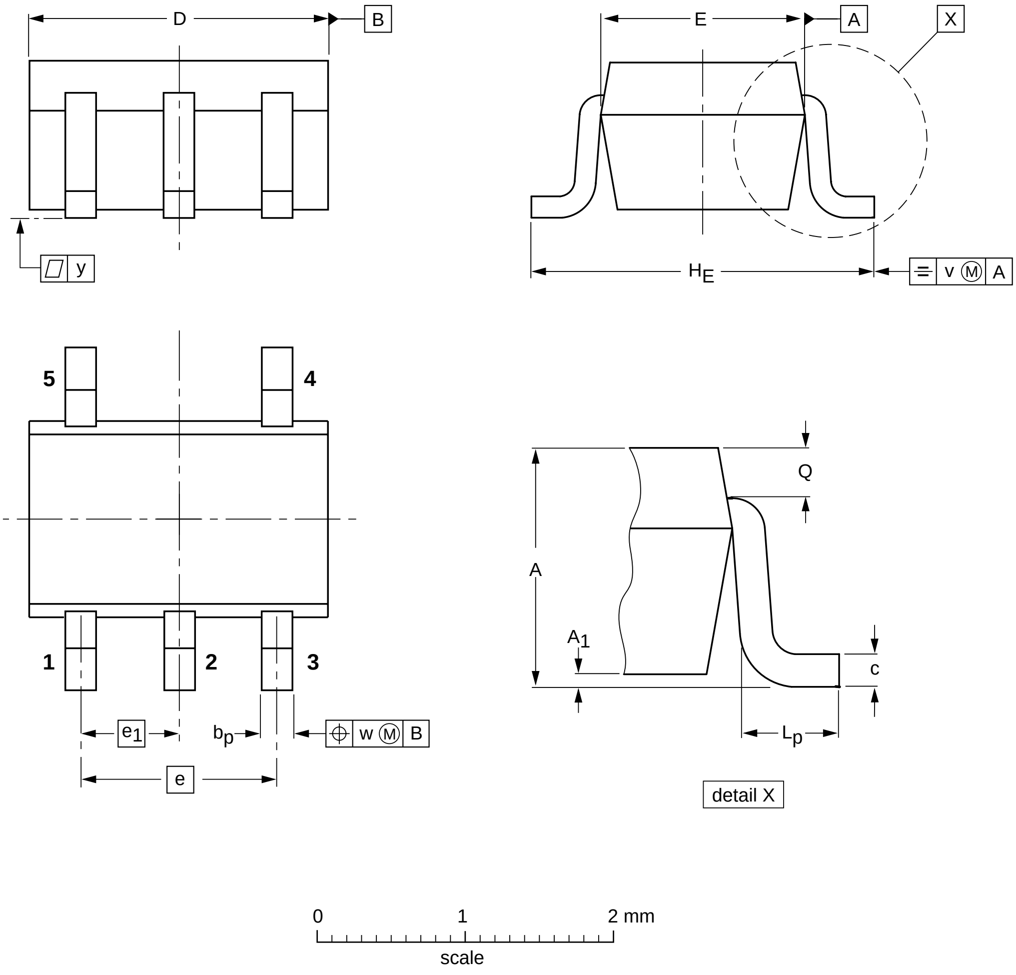
R1 = 1 to 10 MΩ (typical).

R2 optimum value depends on the frequency and required stability against changes in V_{CC} or average minimum I_{CC} (I_{CC} = 2 mA (typical) at V_{CC} = 3.3 V and f = 10 MHz).

Fig.10 Crystal oscillator configuration.

PACKAGE OUTLINE

Plastic surface mounted package; 5 leads **SOT353**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max	b_p	c	D	E (2)	e	e_1	H_E	L_p	Q	v	w	y
mm	1.1 0.8	0.1	0.30 0.20	0.25 0.10	2.2 1.8	1.35 1.15	1.3	0.65	2.2 2.0	0.45 0.15	0.25 0.15	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT353			SC-88A			97-02-28

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW(1)
BGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS	not suitable(2)	suitable
PLCC(3), SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended(3)(4)	suitable
SSOP, TSSOP, VSO	not recommended(5)	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *“Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods”*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

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Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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Notes

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