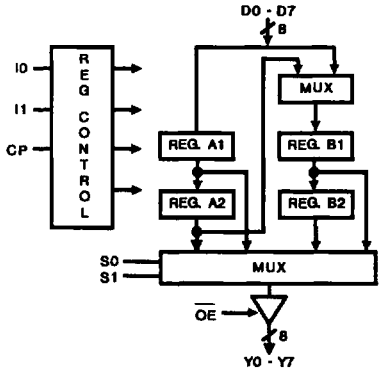
CD54/74FCT29520A, CD54/74FCT29520BT
CD54/74FCT29521A, CD54/74FCT29521BT

July 1990



FUNCTIONAL DIAGRAM

Multilevel Pipeline Registers
Positive-Edge-Triggered

Type Features:

- *Buffered inputs*
- *Typical propagation delay: 7ns @ VCC = 5V, TA = 25°C, CL = 50pF (FCT29520A, FCT29521A)*

The CD54/74FCT29520A, 29520BT, 29521A and 29521BT positive-edge-triggered multilevel pipeline registers use a small-geometry BiCMOS technology. The output stage is a combination of bipolar and CMOS transistors that limits the output-HIGH level to two diode drops below VCC. This resultant lowering of output swing (0V to 3.7V) reduces power bus ringing (a source of EMI) and minimizes VCC bounce and ground bounce and their effects during simultaneous output switching. The output configuration also enhances switching speed and is capable of sinking 32 to 48 milliamperes.

These devices each contain four 8-bit positive-edge-triggered registers that can be operated as a dual 2-level or as a single 4-level pipeline. A single 8-bit input, stored in any of the four registers, is available at the multiplexed 3-state output.

The CD54/74FCT29520A, 29520BT, 29521A and 29521BT differ only in the way the data is loaded into and between the registers in the 2-level operation. (They operate identically in the single 4-level mode.) When data is entered into the first level of the CD54/74FCT29520A, 29520BT the data stored in that level is moved into the second level. In the CD54/74FCT29521A, 29521BT the same instructions (I0 = 0, I1 = 1 for A registers; I0 = 1, I1 = 0 for the B registers) simply cause the data in the first level to be overwritten. The transfer of data to the second level is accomplished by the instruction I0 = 0, I1 = 0. The transfer also causes the first level to change. In either device, I0 = 1, I1 = 1 initiates the HOLD mode. See Figure 1 for instructions/loading relationships.

The CD54/74FCT29520A, 29520BT, 29521A and 29521BT are supplied in 24-lead dual-in-line narrow-body plastic packages (EN suffix) and in 24-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over two temperature ranges: Commercial (0°C to +70°C) and Extended Industrial (-55°C to +125°C).

Family Features:

- *SCR-latchup-resistant BiCMOS process and circuit design*
- *FCTXXXXXA - Speed of bipolar FAST*/AS/S; FCTXXXXXBT - 30% faster than FAST/AS/S with significantly reduced power consumption*
- *48/32-mA output sink current (commercial/extended industrial)*
- *Output voltage swing limited to 3.7V @ VCC = 5V*
- *Controlled output-edge rates*
- *Input/output isolation to VCC*
- *BiCMOS technology with low quiescent power*

* FAST is a registered trademark of Fairchild Semiconductor Corp.

The CD54FCT29520A and 29521A are also available in chip form (H suffix). These unpackaged devices are operable over the -55°C to +125°C temperature range.

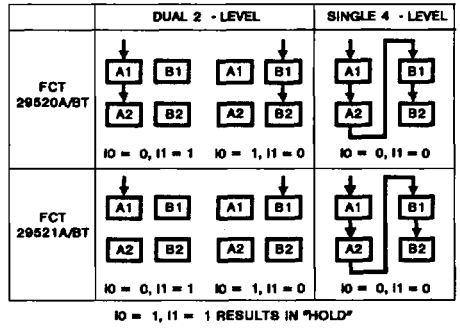


Figure 1 - Data loading vs. instructions.

File Number **2401**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE (VCC) ..... -0.5V to 6V
DC INPUT DIODE CURRENT, IIK (for VI < -0.5V) ..... -20mA
DC OUTPUT DIODE CURRENT, IOK (for VO < -0.5V) ..... -50mA
DC OUTPUT SINK CURRENT per Output Pin, IO ..... +70mA
DC OUTPUT SOURCE CURRENT per Output Pin, IO ..... -30mA
DC VCC CURRENT (ICC) 260mA
DC GROUND CURRENT (IGND) 400mA
POWER DISSIPATION PER PACKAGE (PD):
For TA = -55°C to +100°C (PACKAGE TYPE E) 500mW
For TA = +100°C to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8mW/°C to 300mW
For TA = -55°C to +70°C (PACKAGE TYPE M) 400mW
For TA = +70°C to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6mW/°C to 70mW
OPERATING-TEMPERATURE RANGE (TA):
PACKAGE TYPE E, M ..... -55°C to +125°C
STORAGE TEMPERATURE (Tstg) ..... -65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 in. ± 1/32 in. (1.59mm ± 0.79mm) from case for 10s maximum ..... +265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59mm) with solder contacting lead tips only ..... +300°C

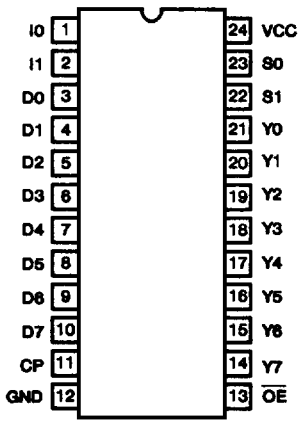
RECOMMENDED OPERATING CONDITIONS:

The following are normal operating ranges for these devices. For maximum reliability, devices should always be operated within these ranges.

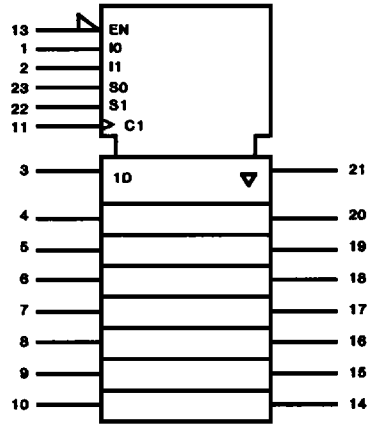
CHARACTERISTIC		LIMITS MIN	LIMITS MAX	UNITS
Supply-Voltage Range, VCC*:	CD74 Series, TA = 0°C to 70°C	4.75	5.25	V
	CD54 Series, TA = -55°C to +125°C	4.5	5.5	V
DC Input Voltage, VI		0	VCC	V
DC Output Voltage, VO		0	≤ VCC	V
Operating Temperature, TA		-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv		0	10	ns/V

* Unless otherwise specified, all voltages are referenced to ground.

CD54/74FCT29520A, CD54/74FCT29520BT, CD54/74FCT29521A AND CD54/74FCT29521BT TYPES



TERMINAL ASSIGNMENT



IEC LOGIC SYMBOL

STATIC ELECTRICAL CHARACTERISTICS

FCT Series: 74FCT Commercial Temperature Range, 0°C to +70°C; VCC max = 5.25V, VCC min = 4.75V
54FCT Extended Industrial Temperature Range, -55°C to +125°C; VCC max = 5.5V, VCC min = 4.5V

CHARACTERISTICS		TEST CONDITIONS			AMBIENT TEMPERATURE (TA)						UNITS
					+25°C		0°C to +70°C		-55°C to +125°C		
		VI (V)	IO (mA)	VCC (V)	MIN	MAX	MIN	MAX	MIN	MAX	
High-Level Input Voltage	VIH			4.5 to 5.5	2	-	2	-	2	-	V
Low-Level Input Voltage	VIL			4.5 to 5.5	-	0.8	-	0.8	-	0.8	V
High-Level Output Voltage	VOH	VIH or VIL	-24	MIN	2.4	-	2.4	-	-	-	V
			-20	MIN	2.4	-	-	-	2.4	-	V
Low-Level Output Voltage	VOL	VIH or VIL	48	MIN	-	0.55	-	0.55	-	-	V
			32	MIN	-	0.55	-	-	-	0.55	V
High-Level Input Current	IIH	VCC		MAX	-	0.1	-	1	-	1	µA
Low-Level Input Current	IIL	GND		MAX	-	-0.1	-	-1	-	-1	µA
3-State Leakage Current	IOZH	VCC		MAX	-	0.5	-	10	-	10	µA
	IOZL	GND		MAX	-	-0.5	-	-10	-	-10	µA
Short-Circuit Output Current *	IOS	VCC or GND VO = 0		MAX	-75	-	-75	-	-75	-	mA
Input Clamp Voltage	VIK	VCC or GND	-18	MIN	-	-1.2	-	-1.2	-	-1.2	V
Quiescent Supply Current, MSI	ICC	VCC or GND	0	MAX	-	8	-	80	-	500	µA
Additional Quiescent Supply Current per Input Pin TTL Inputs High, 1 Unit Load	ΔICC	3.4V†		MAX	-	1.6	-	1.6	-	2	mA

* Not more than one output should be shorted at one time. Test duration should not exceed 100ms.
† Inputs that are not measured are at VCC or GND.

FCT Input Loading: All inputs are 1 unit load. Unit load is ΔICC limit specified in Static Characteristics Chart, e.g., 1.6mA max. @ +70°C.

PREREQUISITE FOR SWITCHING

CHARACTERISTICS	SYMBOL	VCC (V)	CD54/74FCT29520A, 29521A AMBIENT TEMPERATURE (T_A)					CD54/74FCT29520BT, 29521BT AMBIENT TEMPERATURE (T_A)					UNITS
			+25°C	0°C to +70°C		-55°C to +125°C		+25°C	0°C to +70°C		-55°C to +125°C		
			TYP	MIN	MAX	MIN	MAX	TYP	MIN	MAX	MIN	MAX	
Clock Pulse Width	tW	5†		7	-	8	-			-		-	ns
Setup Time — Data to Clock, Instruction to Clock	tSU	5		5	-	6	-			-		-	ns
Hold Time — Data to Clock, Instruction to Clock	tH	5		1	-	2	-			-		-	ns
Maximum Clock Frequency	fMAX	5		70	-	60	-			-		-	MHz

†5V: min. is @ 4.5V
5V: min. is @ 4.75V for 0°C to +70°C
typ. is @ 5V

SWITCHING CHARACTERISTICS

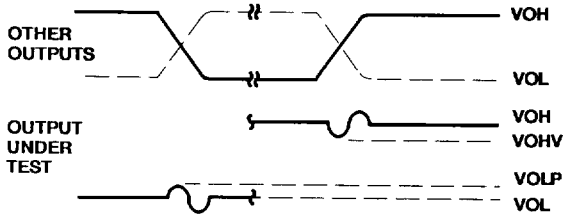
FCT Series: tr, tf = 2.5ns, CL = 50pF, RL - See Figure 5

CHARACTERISTICS	SYMBOL	VCC (V)	CD54/74FCT29520A, 29521A AMBIENT TEMPERATURE (T_A)					CD54/74FCT29520BT, 29521BT AMBIENT TEMPERATURE (T_A)					UNITS
			+25°C	0°C to +70°C		-55°C to +125°C		+25°C	0°C to +70°C		-55°C to +125°C		
			TYP	MIN	MAX	MIN	MAX	TYP	MIN	MAX	MIN	MAX	
Propagation Delays: Clock to Output	tPLH, tPHL	5†	7	1.5	14	1.5	16						ns
Select to Output	tPLH, tPHL	5	7	1.5	13	1.5	15						ns
Output Disable to Output	tPLZ, tPHZ	5	9	1.5	15	1.5	16						ns
Output Enable to Output	tPZL, tPZH	5	6	1.5	12	1.5	13						ns
Power Dissipation Capacitance	CPD§	-											pF
Min. (Valley) VOHV During Switching of Other Outputs (Output Under Test Not Switching)	VOHV See Figure 2	5	0.5 Typical @ +25°C										V
Max. (Peak) VOLP During Switching of Other Outputs (Output Under Test Not Switching)	VOLP See Figure 2	5	1 Typical @ +25°C										V
Input Capacitance	CI	-		-	10	-	10						pF
3-State Output Capacitance	CO	-		-	15	-	15						pF

†5V: min. is @ 5.5V
max. is @ 4.5V
5V: min. is @ 5.25V for 0°C to +70°C
max. is @ 4.75V for 0°C to +70°C
typ. is @ 5V

§CPD, measured per flip-flop, is used to determine the dynamic power consumption.
PD (per package) = VCC ICC + Σ (VCC^2 fi CPD + VO^2 fo CL + VCC ΔICC D) where:
VCC = supply voltage
ΔICC = flow through current x unit load
CL = output load capacitance
D = duty cycle of input high
fo = output frequency
fi = input frequency

PARAMETER MEASUREMENT INFORMATION



NOTES:
1. VOLP is measured with respect to a ground reference near the output under test. VOHV is measured with respect to VOH.
2. Input pulses have the following characteristics: PRR ≤ 1MHz, tr = 2.5ns, tf = 2.5ns, skew 1ns.
3. R.F. fixture with 700-MHz design rules required. IC should be soldered into test board and bypassed with 0.1μF capacitor. Scope and probes require 700-MHz bandwidth.

Figure 2 - Simultaneous switching transient waveforms.

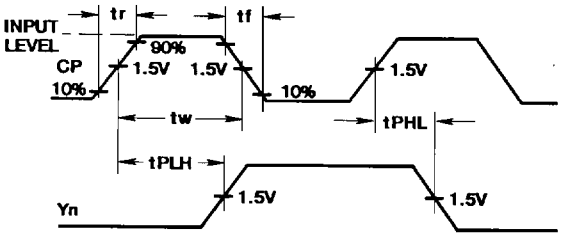


Figure 3 - Propagation delay times.

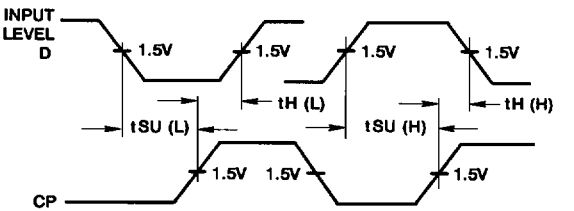
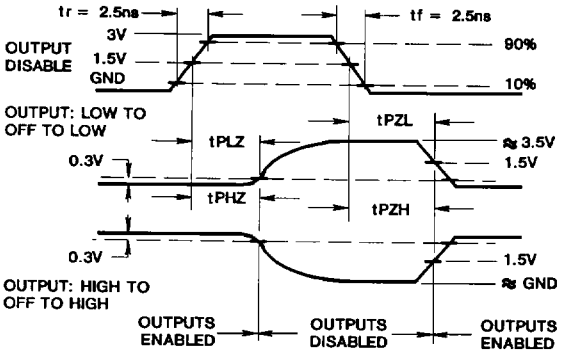
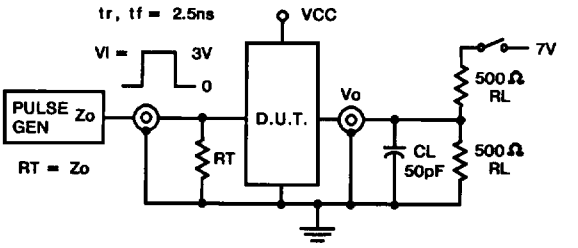


Figure 4 - Setup and hold times.





TEST	SWITCH POSITION
tPLZ, tPZL, OPEN DRAIN	CLOSED
tPHZ, tPZH, tPLH, tPHL	OPEN

Figure 5 - Three-state propagation delay times and test circuit.