⠿Lattice®
⠿⠿ Semiconductor
⠿⠿ Corporation

ispLSI® 5512V

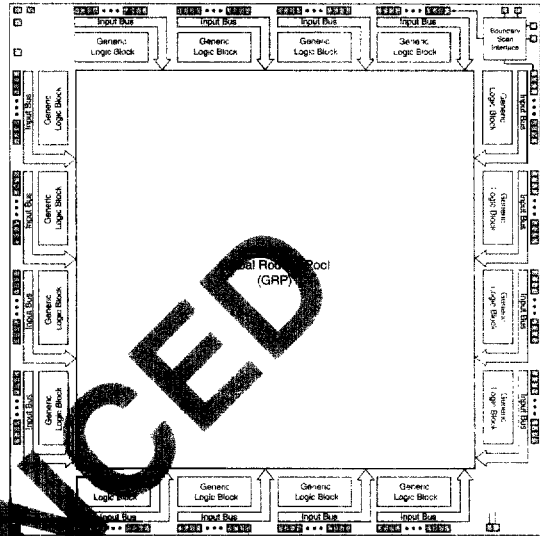## In-System Programmable 3.3V SuperWIDE™ High Density PLD

Features

- **SuperWIDE HIGH DENSITY IN-SYSTEM PROGRAMMABLE LOGIC**
  - 3.3V Power Supply
  - User Selectable 3.3V/2.5V I/O
  - 24000 PLD Gates / 512 Macrocells
  - Up to 384 I/O Pins
  - 512 Registers
  - High-Speed Global Interconnect
  - SuperWide 32 Generic Logic Block (GLB) Size for Optimum Performance
  - Super Wide Input Gating (68 Inputs) for Fast Counters, State Machines, Address Decoders, etc.
  - PCB Efficient Ball Grid Array (BGA) Package Options

- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - fmax = 100 MHz Maximum Operating Frequency
  - tpd = 10 ns Propagation Delay
  - TTL/3.3V/2.5V Compatible Input Thresholds and Output Levels
  - Electrically Erasable and Reprogrammable
  - Non-Volatile
  - Programmable Speed/Power Logic Path Optimization

- **IN-SYSTEM PROGRAMMABLE**
  - Increased Manufacturing Yields, Reduced Time Market, and Improved Product Quality
  - Reprogram Soldered Devices for Faster Debugging

- **100% IEEE 1149.1 BOUNDARY SCAN TESTABLE AN 3.3V IN-SYSTEM PROGRAMMABLE**

- **ARCHITECTURE FEATURES**
  - Enhanced Pin-Locking Archit ure h Single-Level Global Routing Pool a uperW e GLBs
  - Wrap Around Product Term Sh g y Supports up to 35 Product Ter Macr
  - Macrocells Support Co u binatorial and Registered Functions
  - Macrocell Registers Fea e Multiple Control Options Including Set, Re t and Clock Enable
  - Four Dedicated Clock Input Pins Plus Macrocell Product Term Clocks
  - I/O Pins Support Programmable Bus Hold, Pull-up, Open Drain and Slew Rate Options
  - Six Global Output Enable Terms, Two Global OE Pins and One Product Term OE per Macrocell

- **ispEXPERT™ – LOGIC COMPILER AND COMPLETE ISP DEVICE DESIGN SYSTEMS FROM HDL SYNTHESIS THROUGH IN-SYSTEM PROGRAMMING**
  - Superior Quality of Results
  - Tightly Integrated with Leading CAE Vendor Tools
  - Productivity Enhancing Timing Analyzer, Explore Tools, Timing Simulator and ispANALYZER™
  - PC and UNIX Platforms

Functional Block Diagram

ispLSI 5000V Description

The ispLSI 5000V Family of In-System Programmable High Density Logic Devices is based on Generic Logic Blocks (GLBs) of 32 registered macrocells and a single Global Routing Pool (GRP) structure interconnecting the GLBs.

Outputs from the GLBs drive the Global Routing Pool (GRP) between the GLBs. Switching resources are provided to allow signals in the Global Routing Pool to drive any or all the GLBs in the device. This mechanism allows fast, efficient connections across the entire device. Each GLB contains 32 macrocells and a fully populated, programmable AND-array with 160 logic product terms and 5 extra control product terms. The GLB has 68 inputs from the Global Routing Pool which are available in both true and complement form for every product term.

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