256K × 16 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

- **Performance range:**

	tRAC	tCAC	tRC
KM416C156B/BL/BLL-5	50ns	15ns	90ns
KM416C156B/BL/BLL-6	60ns	15ns	110ns
KM416C156B/BL/BLL-7	70ns	20ns	130ns
KM416C156B/BL/BLL-8	80ns	20ns	150ns

- **Fast Page Mode operation**
- **Byte Write operation (2$\overline{W}$)**
- **Word Read/Write operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **Self Refresh Operation (LL-version)**
- **TTL compatible inputs and outputs**
- **Early write or output enable controlled write**
- **Triple +5V ± 10% power supply**
- **Refresh Cycle**
  - **-512 cycle/8ms refresh**
  - **-512 cycle/64ms (L-Version)**
  - **-512 cycle/128ms (LL-Version)**
- **Power Dissipation**
  - **-Standby: 5.5mW (Normal)**
  - **1.1mW (L-version)**
  - **0.83mW (LL-version)**
  - **-Active (50/60/70/80): 605/495/440/415mW**
- **JEDEC standard pinout**
- **Available in plastic SOJ and TSOP (II)**

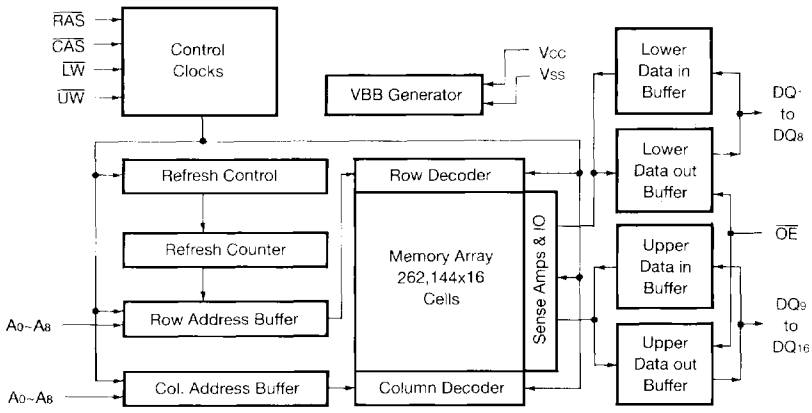
GENERAL DESCRIPTION

The Samsung KM416C156B/BL/BLL is a CMOS high speed 262,144 bit × 16 Dynamic Random Access Memory. Its design is optimized for high performance applications such as minicomputers, graphics and high performance portable computers.

The KM416C156B/BL/BLL features Fast Page Mode operation which allows high speed random access of memory cells within the same row. $\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

The KM416C156B/BL/BLL is fabricated using Samsung's advanced CMOS process.

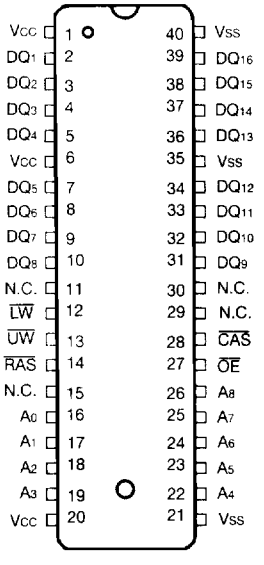
FUNCTIONAL BLOCK DIAGRAM



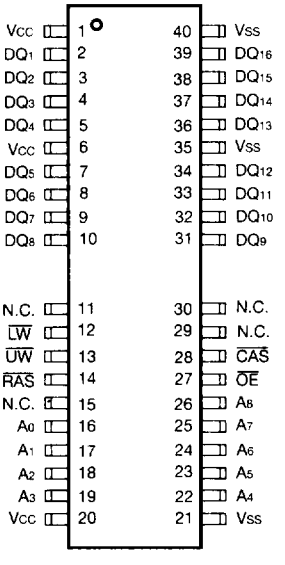
SAMSUNG ELECTRONICS

PIN CONFIGURATION (Top Views)

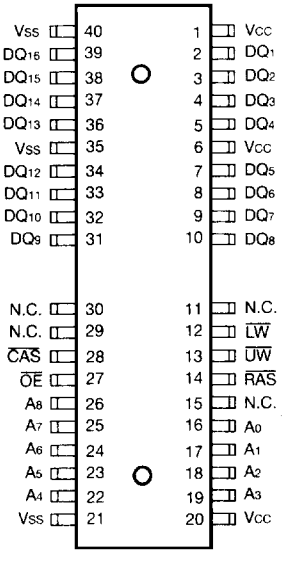
• KM416C156BJ/BLJ/BLLJ



• KM416C156BT/BLT/BLLT



• KM416C156BTR/BLTR/BLLTR



Pin Name	Pin Function
A0-A8	Address Inputs
DQ1~16	Data In/Out
VSS	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{UW}$	Read Upper Byte Write Input
$\overline{LW}$	Read Lower Byte Write Input
$\overline{OE}$	Data Output Enable
VCC	Power(+5V)
N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-1 to + 7.0	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-1 to + 7.0	V
Storage Temperature	T_{stg}	-55 to + 150	C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A=0 to 70 C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC} +1	V
Input Low Voltage	V_{IL}	-1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @ t_{RC}=min.)	KM416C156B/BL/BLL-5	I_{CC1}	-	110	mA
	KM416C156B/BL/BLL-6			90	mA
	KM416C156B/BL/BLL-7			80	mA
	KM416C156B/BL/BLL-8			75	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{UW}$=$\overline{LW}$=V_{IH})		I_{CC2}	-	2	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ Cycling @ t_{RC}=min.)	KM416C156B/BL/BLL-5	I_{CC3}	-	110	mA
	KM416C156B/BL/BLL-6			90	mA
	KM416C156B/BL/BLL-7			80	mA
	KM416C156B/BL/BLL-8			75	mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address Cycling @ t_{PC}=min.)	KM416C156B/BL/BLL-5	I_{CC4}	-	70	mA
	KM416C156B/BL/BLL-6			60	mA
	KM416C156B/BL/BLL-7			55	mA
	KM416C156B/BL/BLL-8			50	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{UW}$=$\overline{LW}$=V_{CC}-0.2V)	KM416C156B	I_{CC5}	-	1	mA
	KM416C156BL			200	mA
	KM416C156BLL			150	μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @ t_{RC}=min.)	KM416C156B/BL/BLL-5	I_{CC6}	-	110	mA
	KM416C156B/BL/BLL-6			90	mA
	KM416C156B/BL/BLL-7			80	mA
	KM416C156B/BL/BLL-8			75	mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage(V_{IH})=V_{CC}-0.2V Input Low Voltage(V_{IL})=0.2V $\overline{CAS}$=0.2V D_{IN}=Don't Care, t_{RC}=125μS(L-ver.), t_{RAS}=t_{RAS} min.~300ns	KM416C156BL	I_{CC7}	-	300	μA

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DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Self Refresh Current $\overline{RAS}$=$\overline{CAS}$=0.2V $\overline{xW}$=$\overline{OE}$=A0-A8=VCC-0.2V or 0.2V	KM416C156BLL	ICCS		200	μA
Input Leakage Current (Any input 0≤VIN≤VCC+0.5V, all other pins not under test=0 volts.)		II(L)	-10	10	μA
Output Leakage Current (Data out is disabled, 0V≤VOUT≤VCC)		IO(L)	-10	10	μA
Output High Voltage Level (IO(H)=-5mA)		VOH	2.4	-	V
Output Low Voltage Level (IO(L)=4.2mA)		VOL	-	0.4	V

*NOTE: ICC1, ICC3, ICC4 and ICC6 are dependent on output loading and cycle rates. Specified values are obtained with the output open. ICC is specified as an average current. In ICC1 and ICC3, address can be changed maximum two times while $\overline{RAS}$=VIL. In ICC4, address can be changed maximum once within one fast page cycle.

CAPACITANCE (TA=25°C, VCC=5V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A0~A8)	CIN1	-	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{LW}$, $\overline{UW}$, $\overline{OE}$)	CIN2	-	7	pF
Input Capacitance (DQ1~DQ16)	CDQ	-	7	pF

AC CHARACTERISTICS (0°C≤TA≤70°C, VCC=5V ± 10%, See notes 1,2)

Parameter	Symbol	-5(*)		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	90		110		130		150		ns	
Read-modify-write cycle time	tRWC	135		155		185		205		ns	
Access time from $\overline{RAS}$	tRAC		50		60		70		80	ns	3,4,11
Access time from $\overline{CAS}$	tCAC		15		15		20		20	ns	3,4,5
Access time from column address	tAA		25		30		35		40	ns	3,11
$\overline{CAS}$ to output in Low-Z	tCLZ	0		0		0		0		ns	3
Output buffer turn-off delay	tOFF	0	15	0	15	0	15	0	15	ns	7
Transition time (rise and fall)	tT	3	50	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	tRP	30		40		50		60		ns	
$\overline{RAS}$ pulse width	tRAS	50	10,000	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	tRSH	15		15		20		20		ns	
$\overline{CAS}$ hold time	tCSH	50		60		70		80		ns	
$\overline{CAS}$ pulse width	tCAS	15	10,000	15	10,000	20	10,000	20	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	35	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	tRAD	15	25	15	30	15	35	15	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		5		ns	
Row address set-up time	tASR	0		0		0		0		ns	

(*) 50ns Product:VCC=5V ± 5%, Cout=50pF

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5(*)		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Row address hold time	tRAH	10		10		10		10		ns	
Column address set-up time	tASC	0		0		0		0		ns	
Column address hold time	tCAH	10		10		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	tAR	40		45		55		60		ns	6
Column address to $\overline{RAS}$ lead time	tRAL	25		30		35		40		ns	
Read command set-up time	tRCS	0		0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		0		ns	9
Write command hold time	tWCH	10		10		10		10		ns	
Write command hold time referenced to $\overline{RAS}$	tWCR	40		45		50		55		ns	6
Write command pulse width	tWP	10		10		10		10		ns	
Write command to $\overline{RAS}$ lead time	tRWL	15		15		15		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	15		15		15		20		ns	
Data set-up time	tDS	0		0		0		0		ns	10
Data hold time	tDH	10		10		15		15		ns	10
Data hold time referenced to $\overline{RAS}$	tDHR	40		45		55		60		ns	6
Refresh period (Normal)	tREF		8		8		8		8	ms	
Refresh period (L-Version)	tREF		64		64		64		64	ms	
Refresh period (LL-Version)	tREF		128		128		128		128	ms	
Write command set-up time	tWCS	0		0		0		0		ns	8
$\overline{CAS}$ to $\overline{LW}$, $\overline{UW}$ delay time	tCWD	40		40		50		50		ns	8
$\overline{RAS}$ to $\overline{LW}$, $\overline{UW}$ delay time	tRWD	75		85		95		105		ns	8
Column address to $\overline{LW}$, $\overline{UW}$ delay time	tAWD	50		55		60		65		ns	8
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	55		60		65		70		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	10		10		10		10		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		10		15		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	tCPT	20		20		25		30		ns	
Access time from $\overline{CAS}$ precharge	tCPA		30		35		40		45	ns	3
Fast Page mode cycle time	tPC	35		40		45		50		ns	
Fast Page mode read-modify-write cycle time	tPRWC	80		80		95		100		ns	
$\overline{CAS}$ precharge time (Fast Page mode)	tCP	10		10		10		10		ns	
$\overline{RAS}$ pulse width (Fast Page mode)	tRASP	50	100K	60	100K	70	100K	80	100K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	30		35		40		45		ns	
$\overline{OE}$ access time	tOEA		15		15		20		20	ns	
$\overline{OE}$ to data delay	tOED	15		15		20		20		ns	
Out put buffer turn off delay time from $\overline{OE}$	tOEZ	0	15	0	15	0	20	0	20	ns	7

(*) 50ns Product:V_{CC}=5V ± 5%, Cout=50pF

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5(*)		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{OE}$ commend hold time	tOEH	15		15		20		20		ns	
Masked write set-up time	tMCS	0		0		0		0		ns	
Masked write hold time referenced to $\overline{RAS}$	tMRH	0		0		0		0		ns	
Masked write hold time referenced to $\overline{CAS}$	tMCH	0		0		0		0		ns	
$\overline{RAS}$ pulse width ($\overline{C}$-B-$\overline{R}$ self refresh)	tRASS	100		100		100		100		μs	12
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	tRPS	90		110		130		150		ns	12
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	tCHS	-50		-50		-50		-50		ns	12

(*) 50ns Product:Vcc=5V ± 5%, Cout=50pF

KM416C156B Truth Table

$\overline{RAS}$	$\overline{CAS}$	$\overline{UW}$	$\overline{LW}$	$\overline{OE}$	DQ1~DQ8	DQ9~DQ16	STATE
H	X	X	X	X	HI-Z	HI-Z	Standby
L	H	X	X	X	HI-Z	HI-Z	Refresh
L	L	H	H	L	DQ-OUT	DQ-OUT	Word Read
L	L	L	L	X	DQ-IN	DQ-IN	Word Write
L	L	H	L	X	DQ-IN	-	Byte Write
L	L	L	H	X	-	DQ-IN	Byte Write

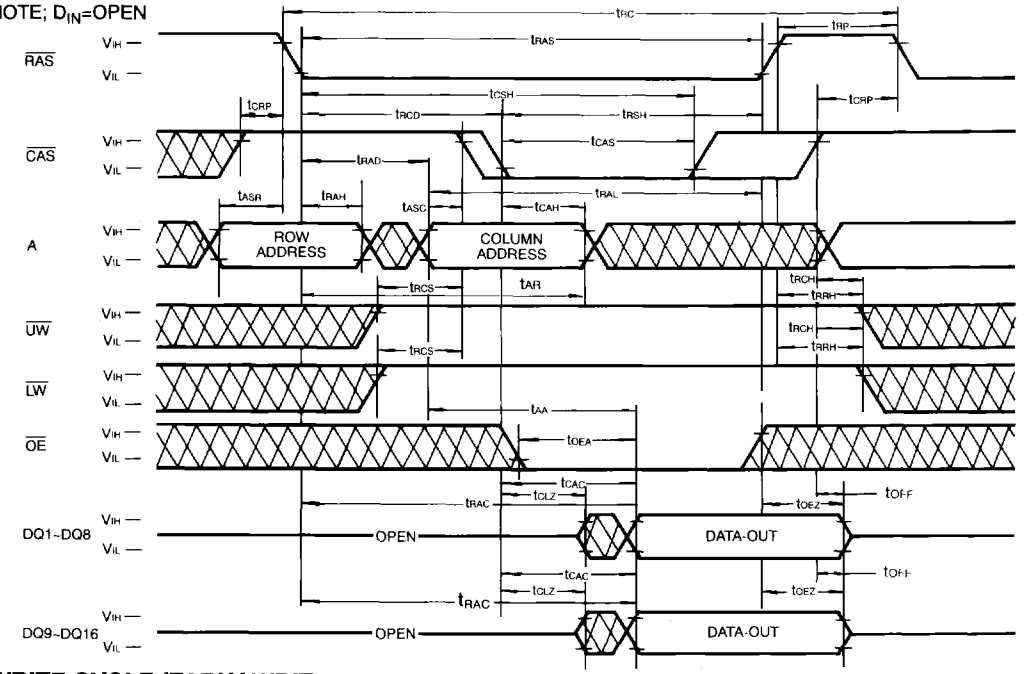
NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to t_{RAD}(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
12. 512 cycles of burst refresh must be executed within 8ms before and after self refresh, In order to meet refresh specification.
13. t_{RCS}, t_{MCS} are referenced to the later $\overline{W}$ rising edge at early write cycle.
14. t_{WCS} is referenced to the later $\overline{W}$ falling edge at early write cycle.
15. t_{CWL}, t_{RWL} are referenced to the later $\overline{W}$ falling edge at early write cycle.
16. t_{WCH}, t_{WP} are referenced to the earler $\overline{W}$ falling edge at early write cycle.
17. t_{RWD}, t_{AWD}, t_{CWD} are referenced to the earler $\overline{W}$ falling edge at Read-Modify-write cycle.

TIMING DIAGRAM

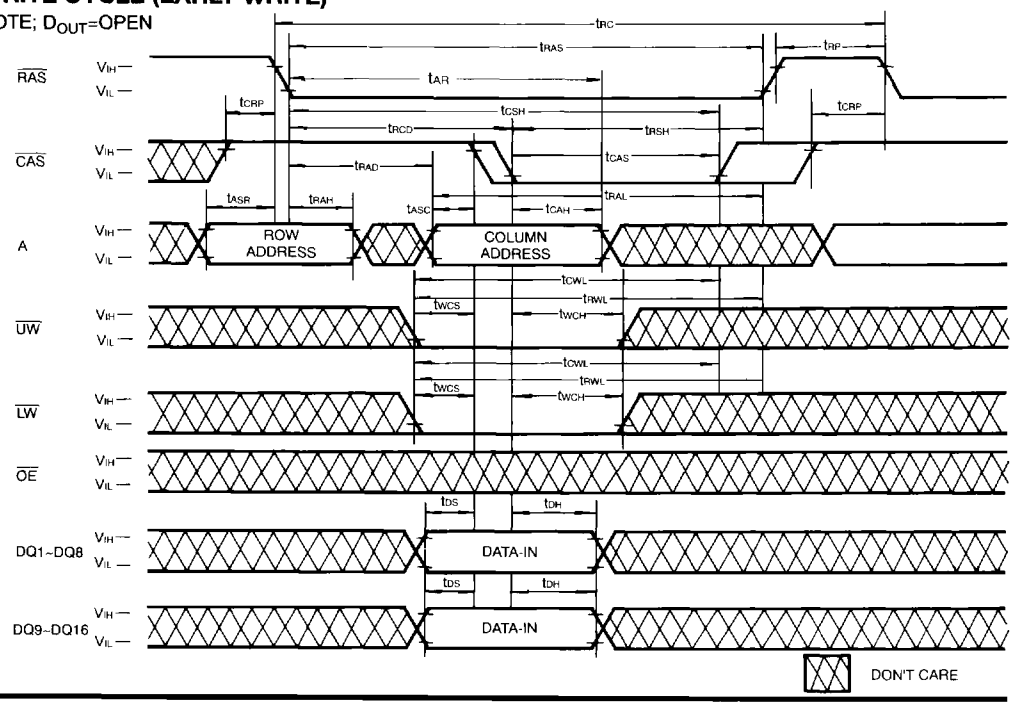
READ CYCLE

NOTE; D_{IN}=OPEN



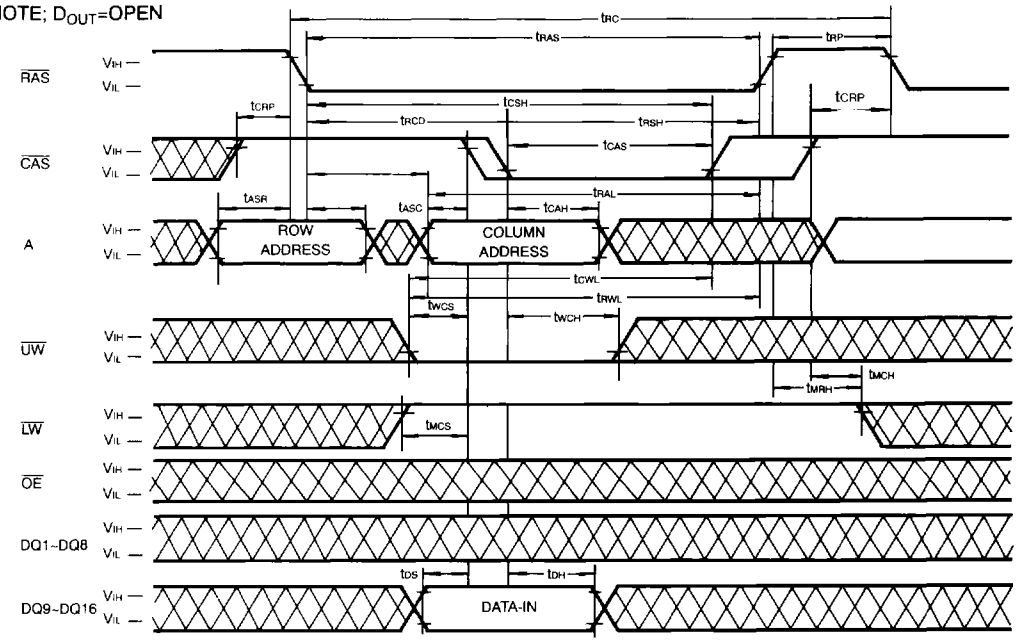
WRITE CYCLE (EARLY WRITE)

NOTE; D_{OUT}=OPEN



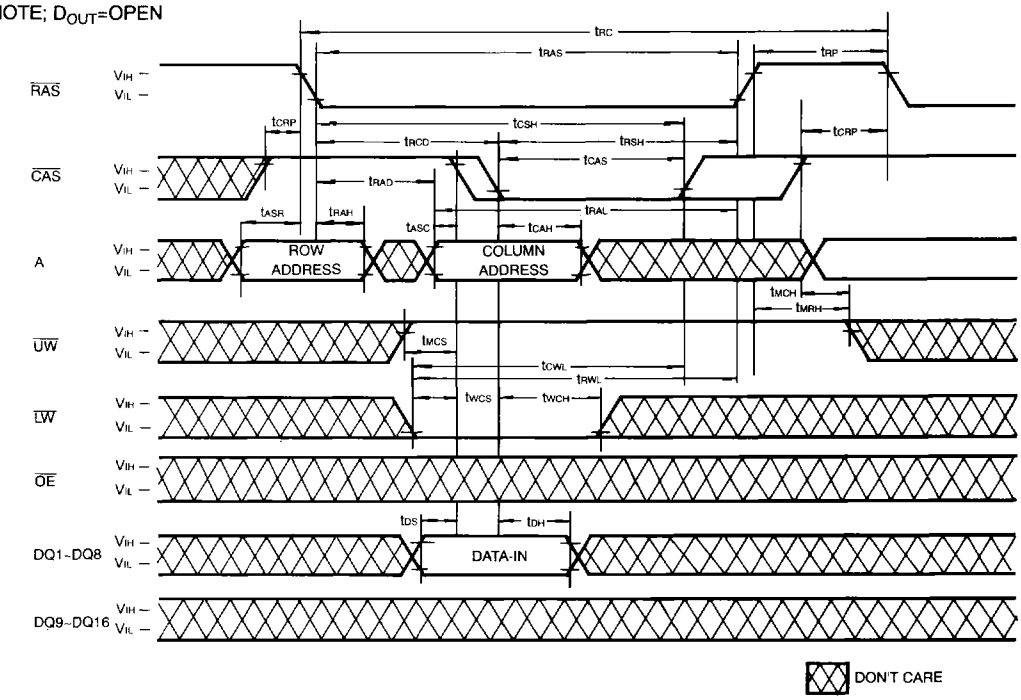
UPPER BYTE WRITE CYCLE (EARLY WRITE)

NOTE; D_{OUT}=OPEN



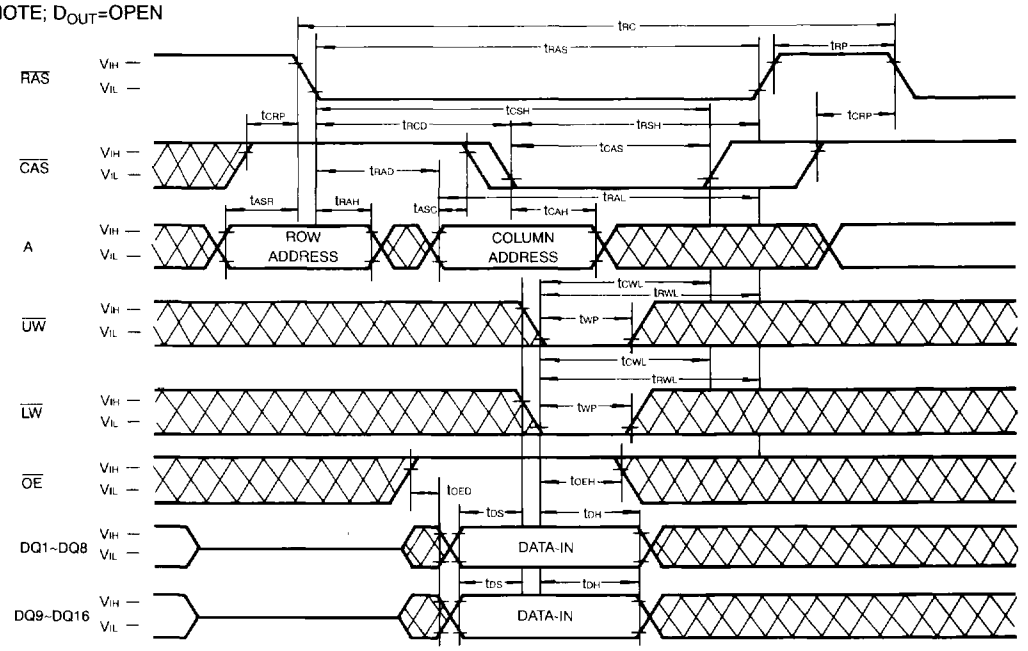
LOWER BYTE WRITE CYCLE (EARLY WRITE)

NOTE; D_{OUT}=OPEN



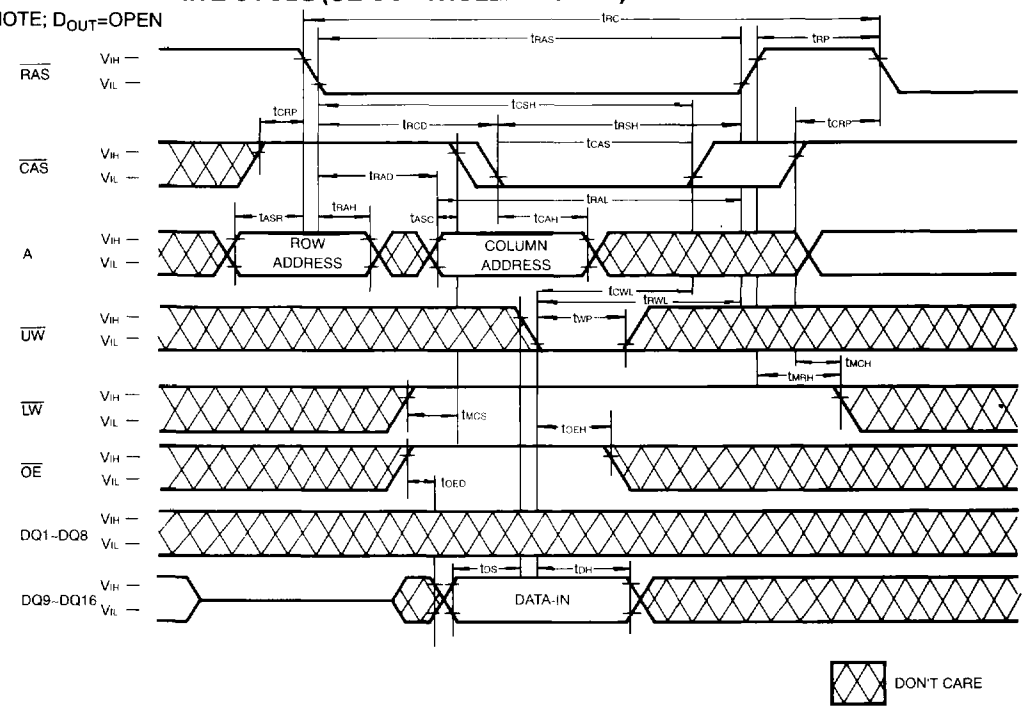
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

NOTE; D_{OUT}=OPEN



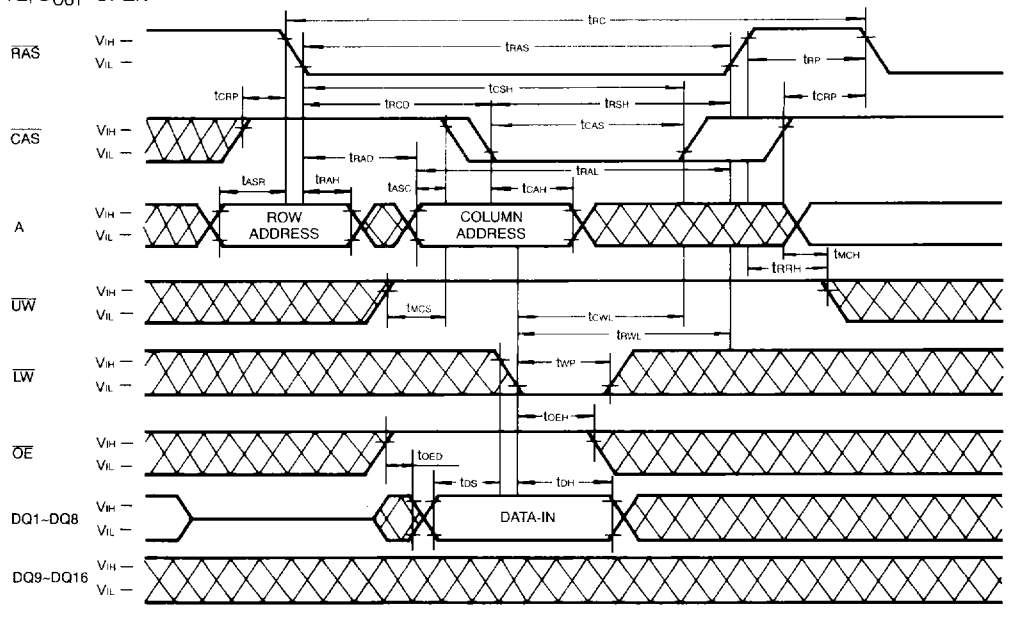
UPPER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

NOTE; D_{OUT}=OPEN

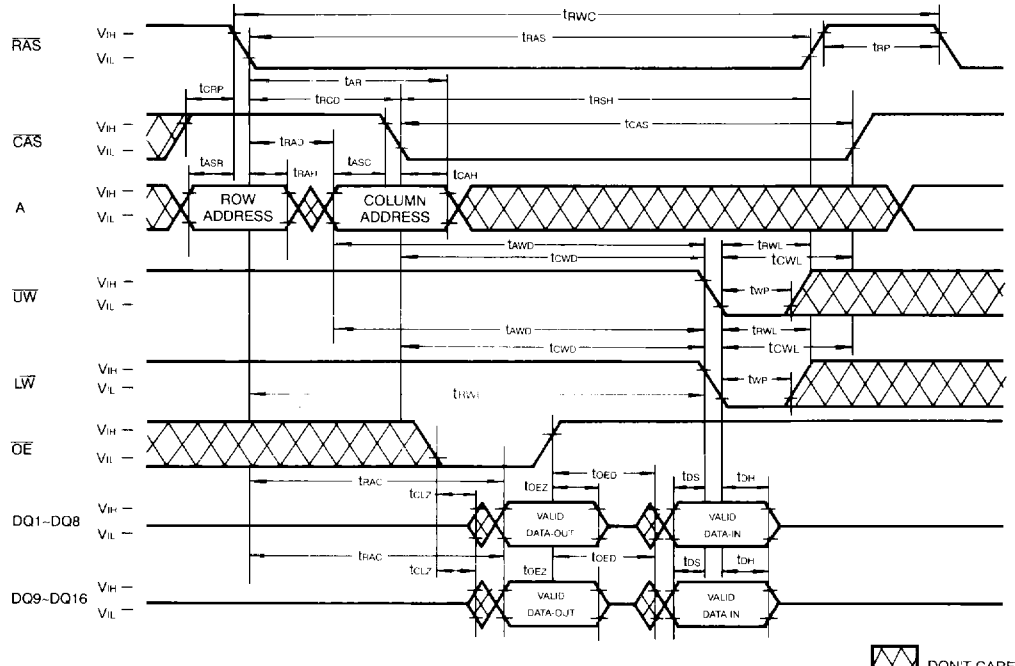


LOWER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

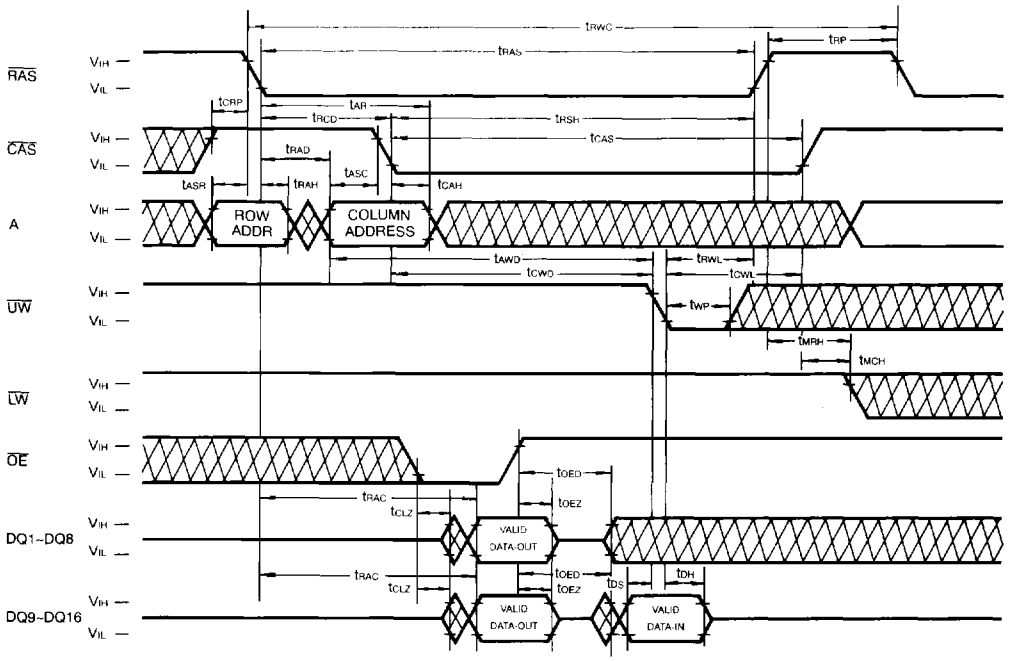
NOTE; D_{OUT}=OPEN



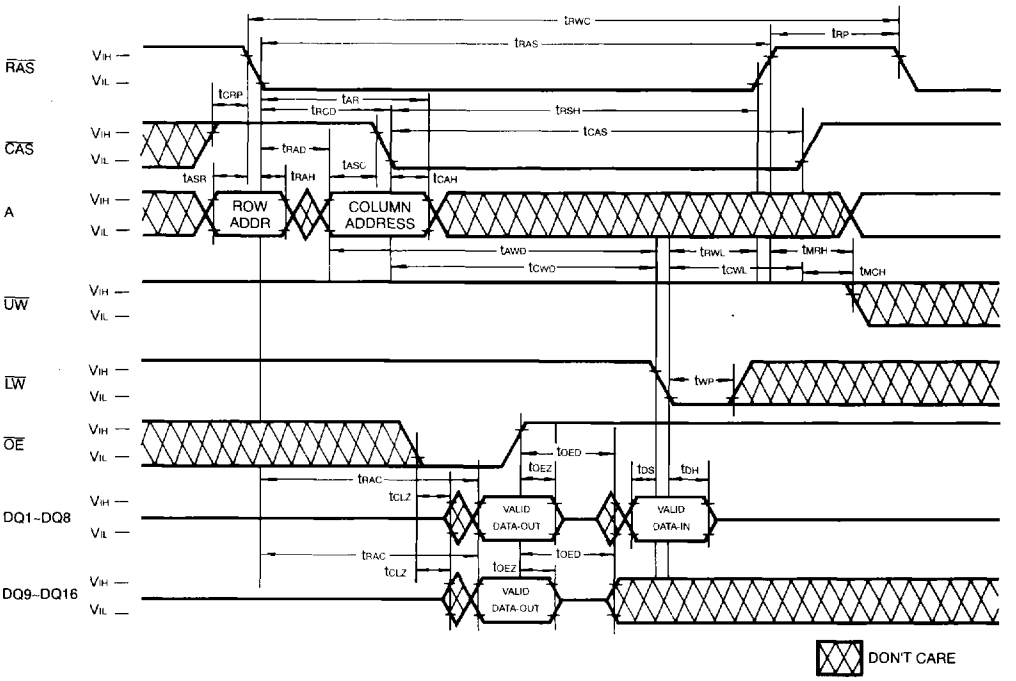
READ-MODIFY-WRITE CYCLE



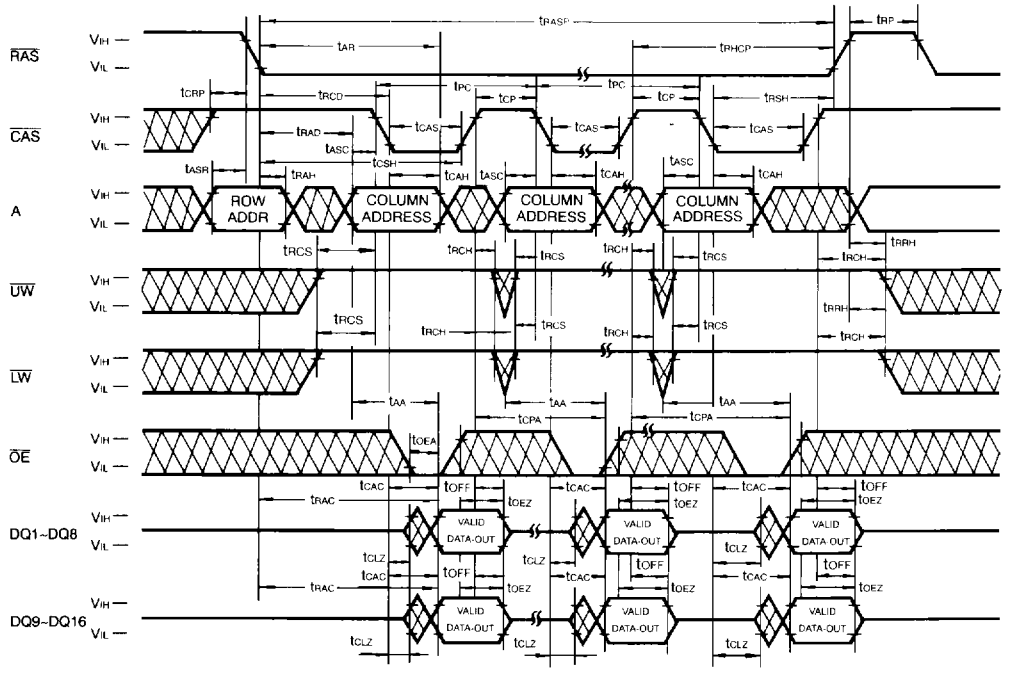
READ-MODIFY-UPPER-BYTE-WRITE CYCLE



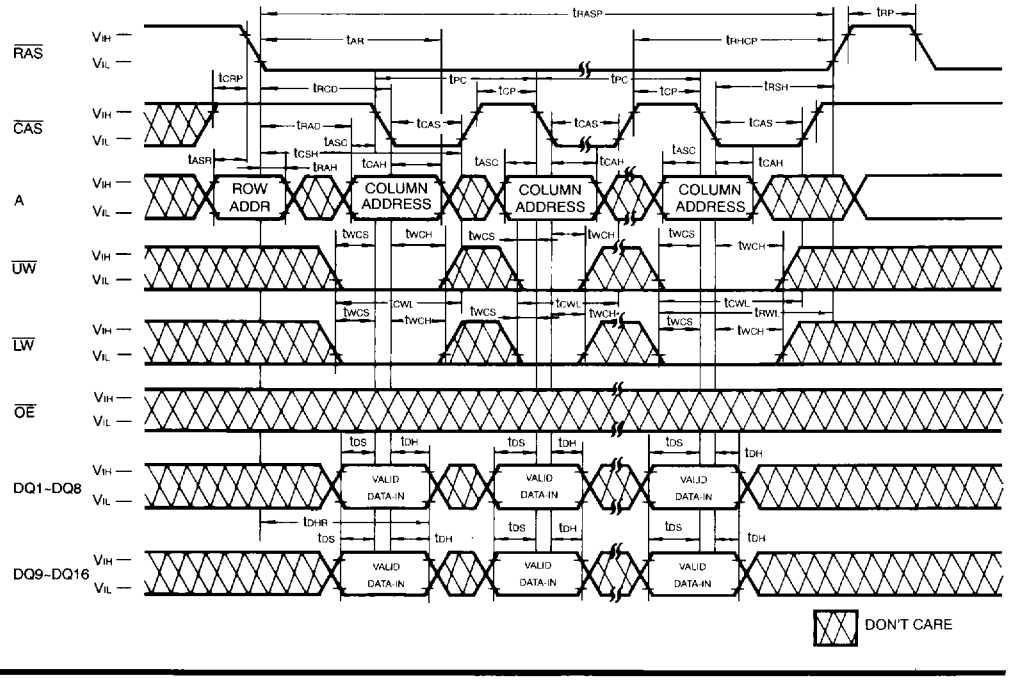
READ-MODIFY-LOWER-BYTE-WRITE CYCLE



FAST PAGE MODE WORD READ CYCLE

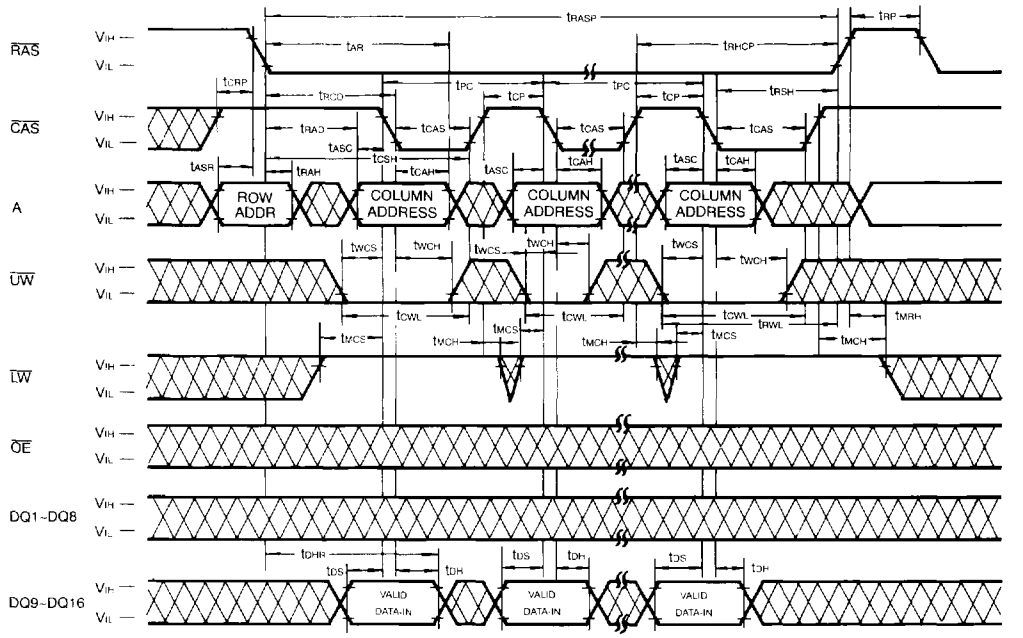


FAST PAGE MODE WORD WRITE CYCLE (EARLY WRITE)



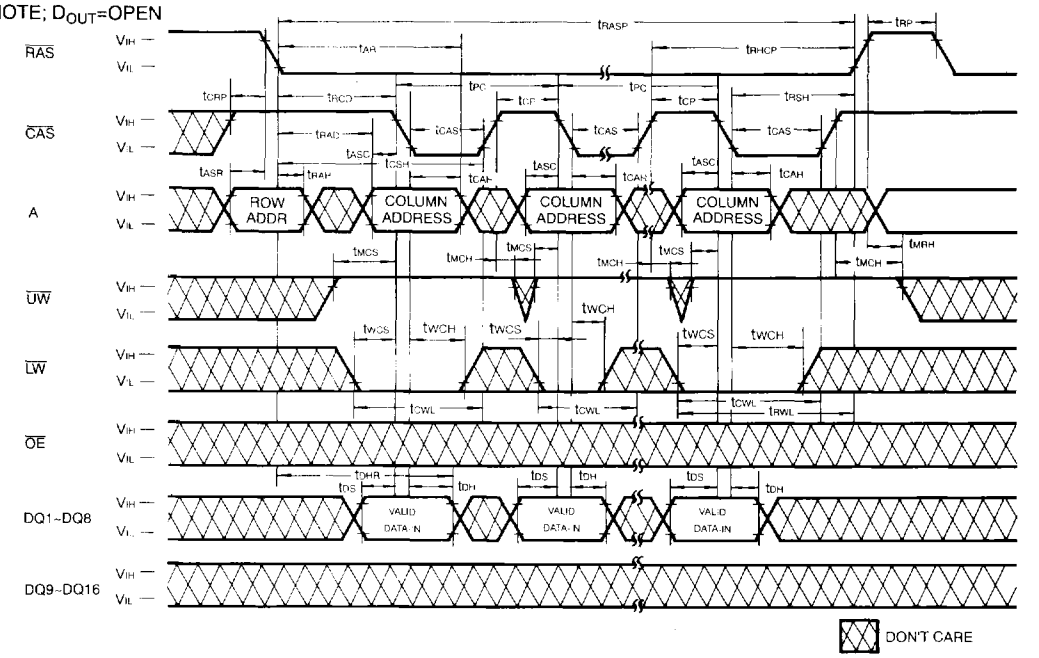
FAST PAGE MODE UPPER BYTE WRITE CYCLE (EARLY WRITE)

NOTE; D_{OUT}=OPEN

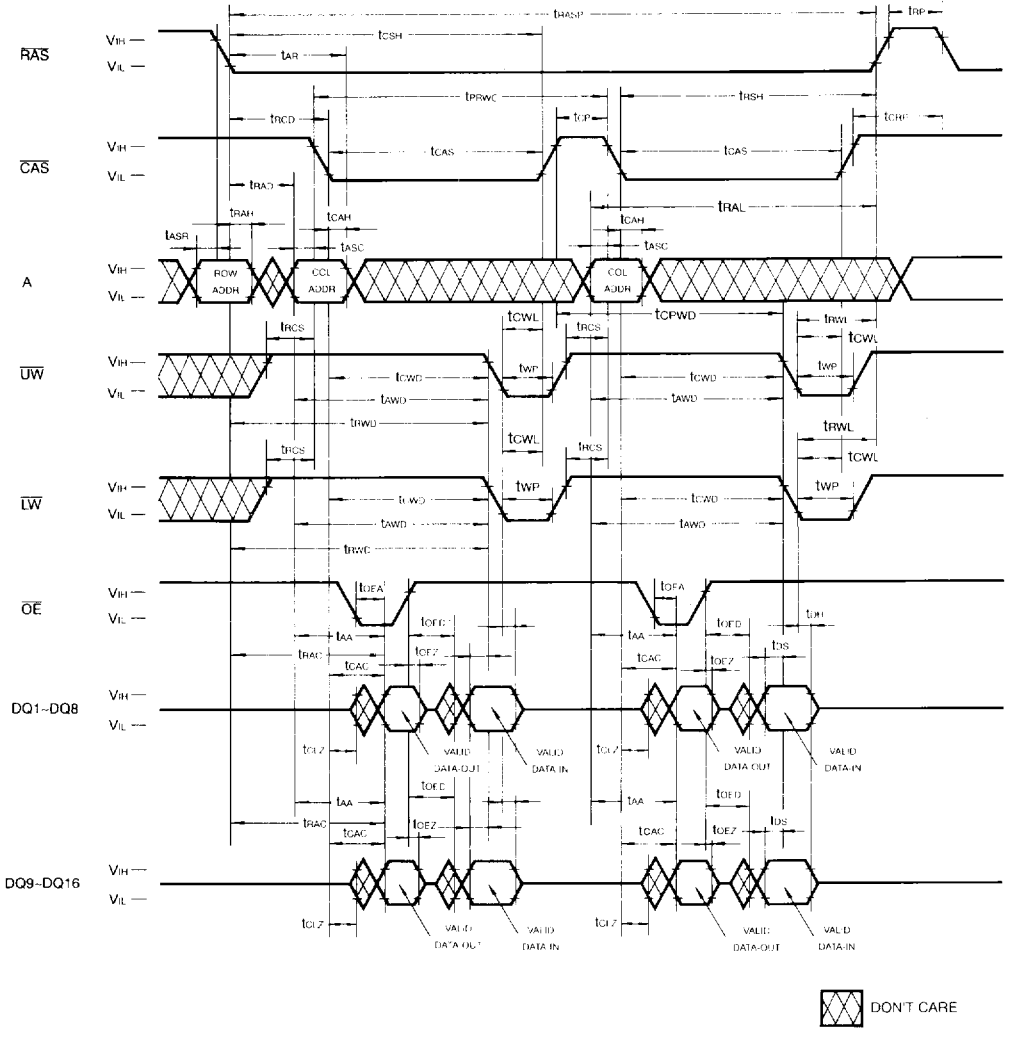


FAST PAGE MODE LOWER BYTE WRITE CYCLE (EARLY WRITE)

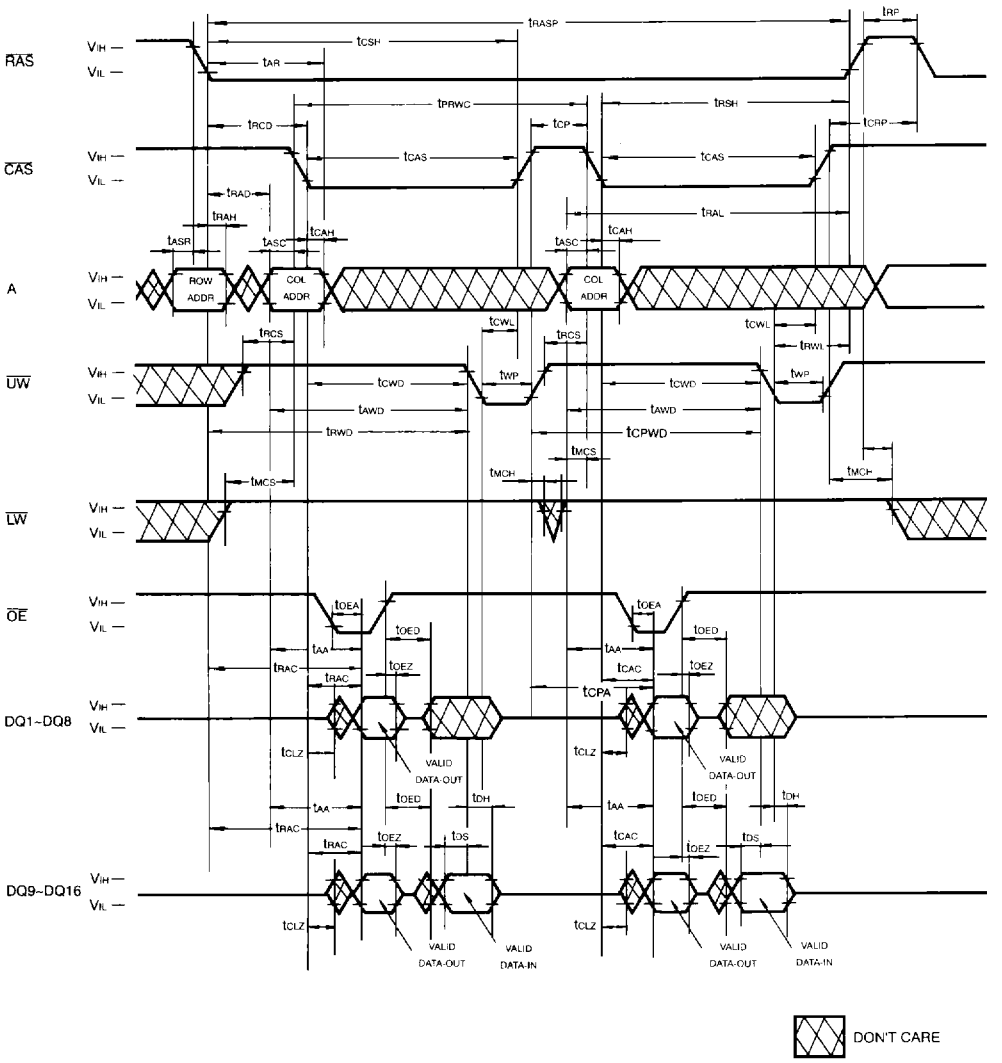
NOTE; D_{OUT}=OPEN



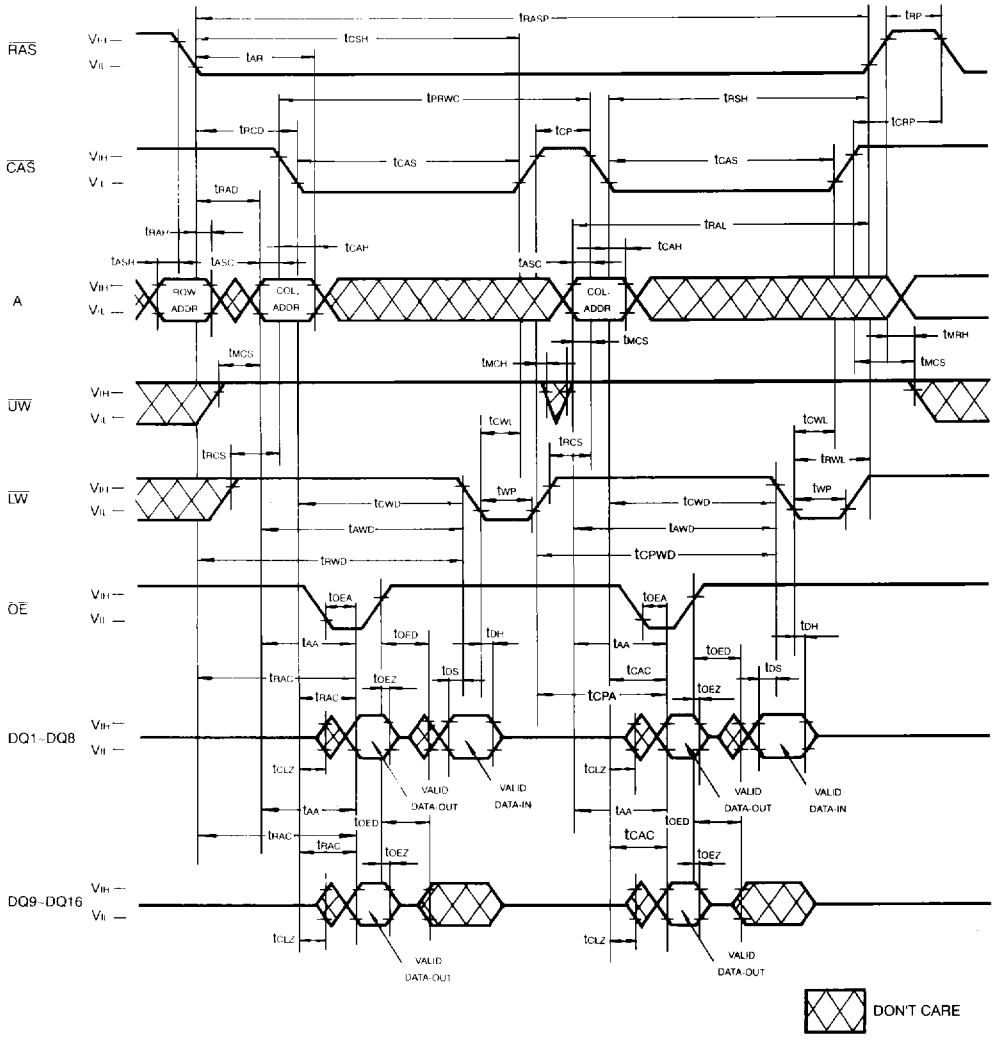
FAST PAGE MODE READ-MODIFY- WRITE CYCLE



FAST PAGE MODE READ-MODIFY-LOWER-BYTE-WRITE CYCLE

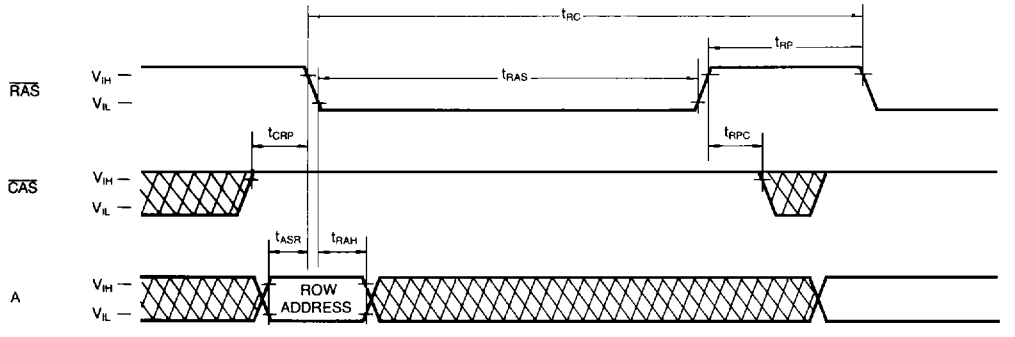


FAST PAGE MODE READ-MODIFY-UPPER-BYTE-WRITE CYCLE



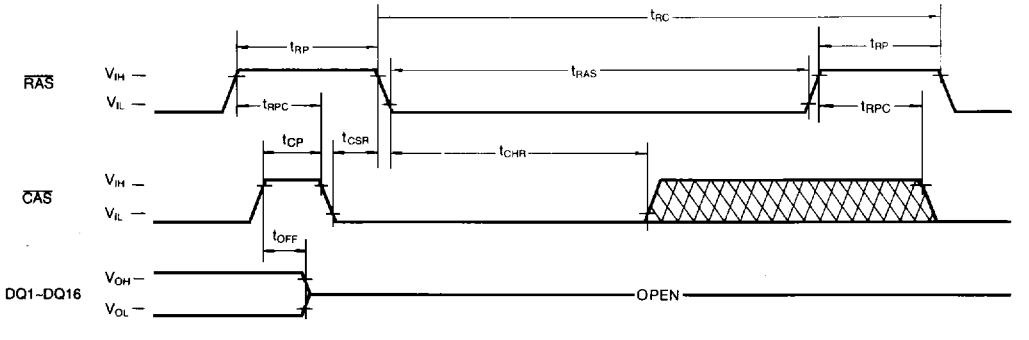
$\overline{RAS}$-ONLY REFRESH CYCLE

NOTE; $\overline{UW}$, $\overline{LW}$, $\overline{OE}$, D_{IN}=Don't Care D_{OUT}=OPEN



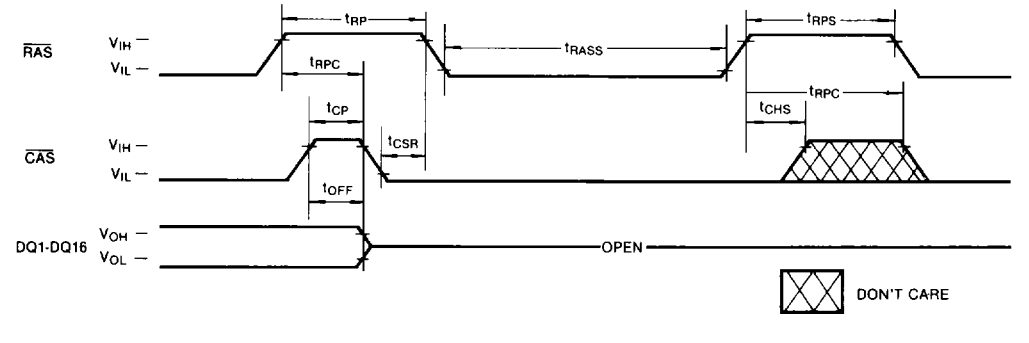
$\overline{CAS}$-before-$\overline{RAS}$ REFRESH CYCLE

NOTE; $\overline{UW}$, $\overline{LW}$, $\overline{OE}$, A=Don't Care

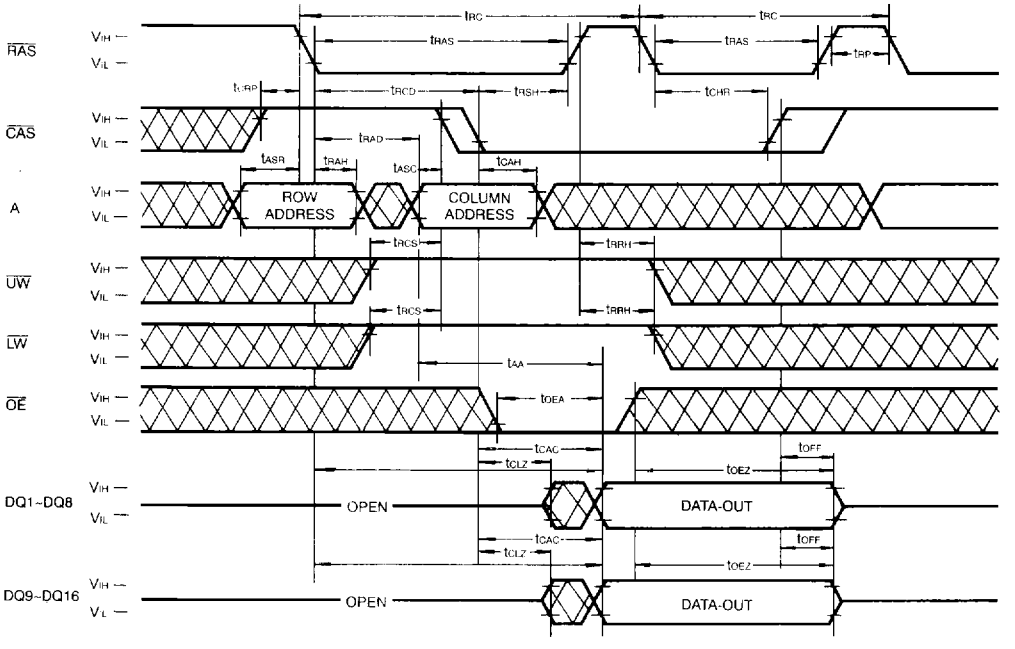


$\overline{CAS}$-before-$\overline{RAS}$ SELF REFRESH CYCLE (LL-version)

NOTE: $\overline{W}$, $\overline{OE}$, A=Don't Care

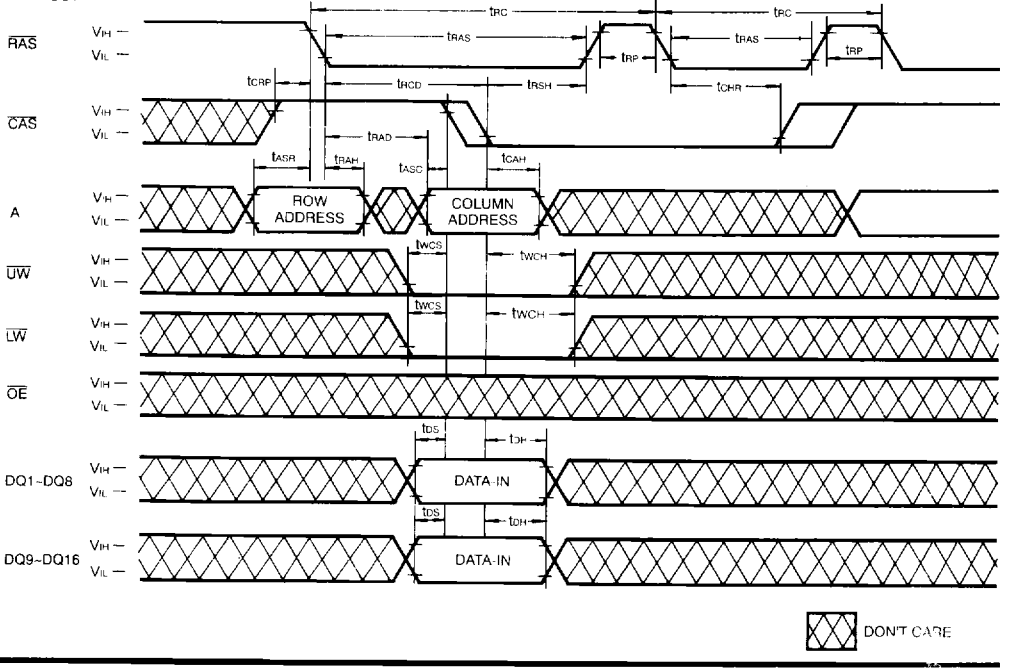


HIDDEN REFRESH CYCLE (READ)



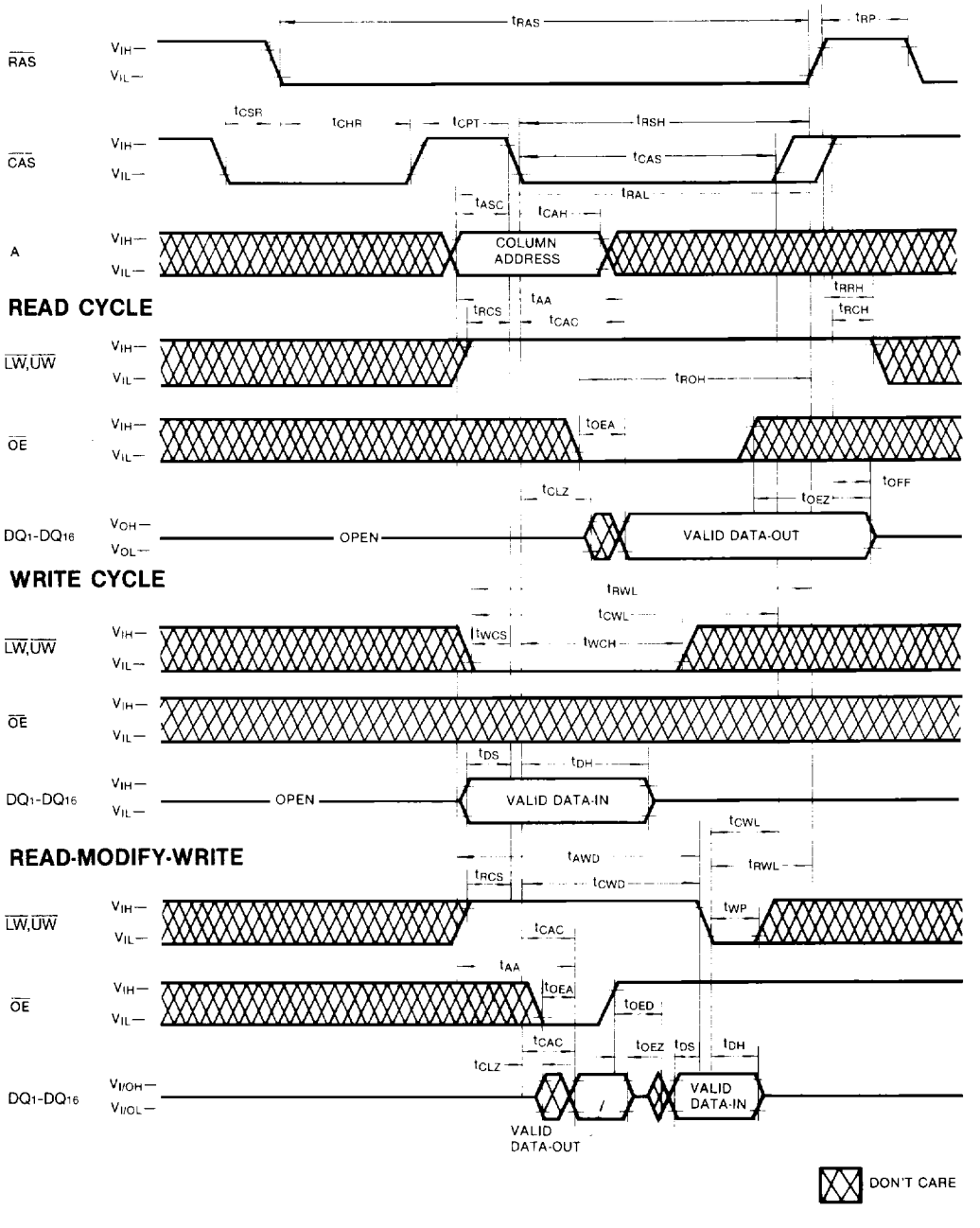
HIDDEN REFRESH CYCLE (WRITE)

NOTE; D_{OUT}=OPEN



TIMING DIAGRAMS (Continued)

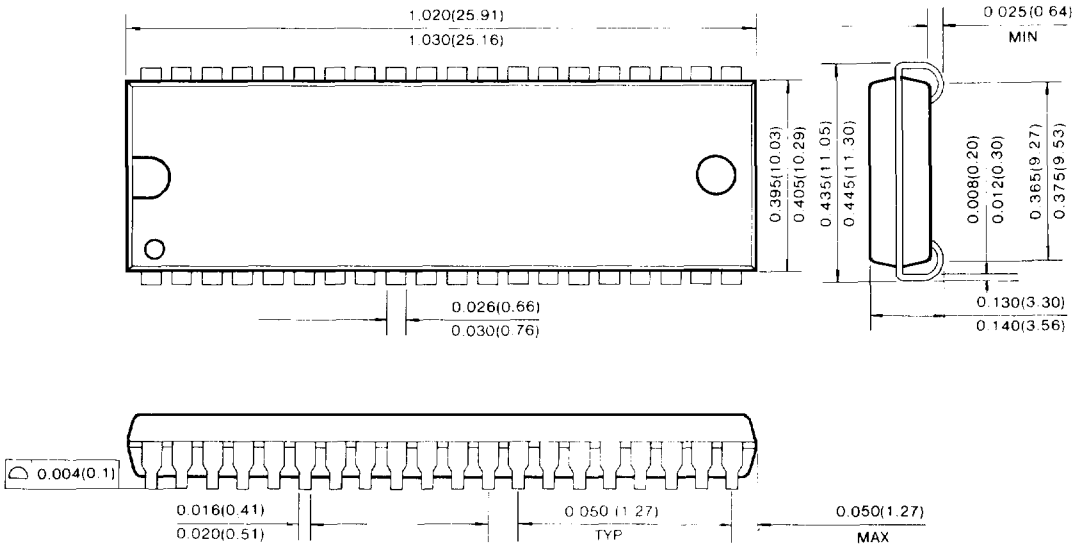
CAS-before-RAS REFRESH COUNTER TEST CYCLE



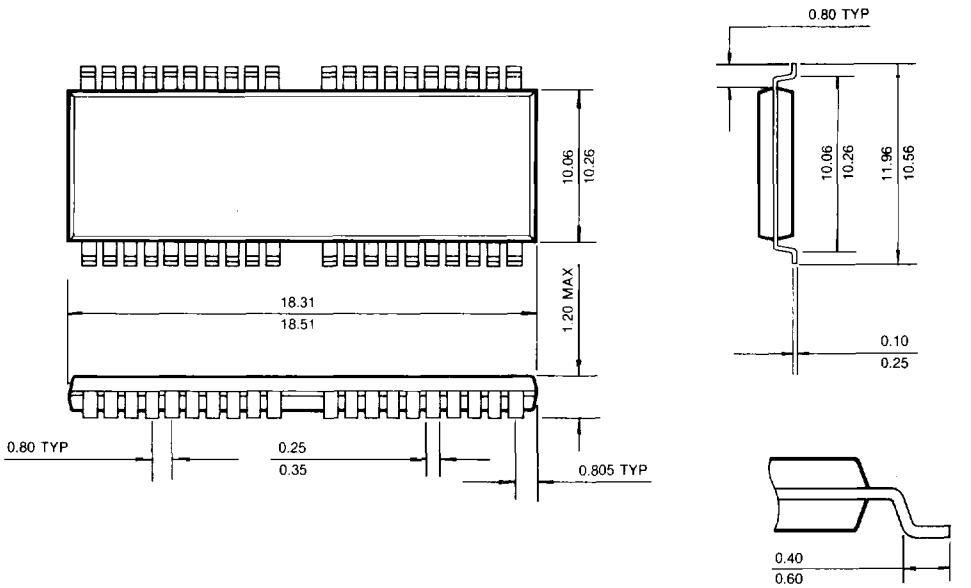
PACKAGE DIMENSION

40-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



40 LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE (II)
(Forward and Reverse Type)



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