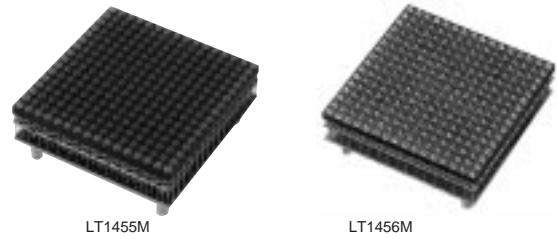


# Dot Matrix LED Unit for Indoor/Outdoor Use LT1455M/LT1456M(Lamp Type)

## ■ Features

- No. of dots : 16X16dots
- Outline dimensions : 96.0X96.0mm
- Dot size : ø5.0mm
- Dot pitch : 6.0mm
- Radiation color : Yellow-green+Red(High-luminosity)dichromatic type
- Driving method : 1/8 duty dynamic drive

Outline dimensions are shown on page 206, Fig.8.



## ■ Absolute Maximum Ratings

(Ta=25°C)

Parameter	Symbol	Rating	Unit
Supply voltage for IC	VCC	-0.3 to +6.0	V
Supply voltage for LED	VLED	-0.3 to +5.5	V
Input voltage	VI	-0.3 to Vcc+0.3	V
Turn-on time	ton	1	ms
Operating temperature	Topr	-10 to +65*1	°C
Storage temperature	Tstg	-20 to +85	°C
Power dissipation	P	22	W

\*1 When dichromatic all dots are lit, duty ratio=1/8.

## ■ Optical Characteristics

(Vcc=5V, VLED=5V, Ta=25°C)

Parameter	Symbol	TYP.	Unit
Viewing angle	2θ1/2	50/40	°
Peak emission wavelength	Red	660	nm
	Yellow-green	565	

Each figure in the table is the one of LT1455M/LT1456M in sequence.

## ■ Luminance

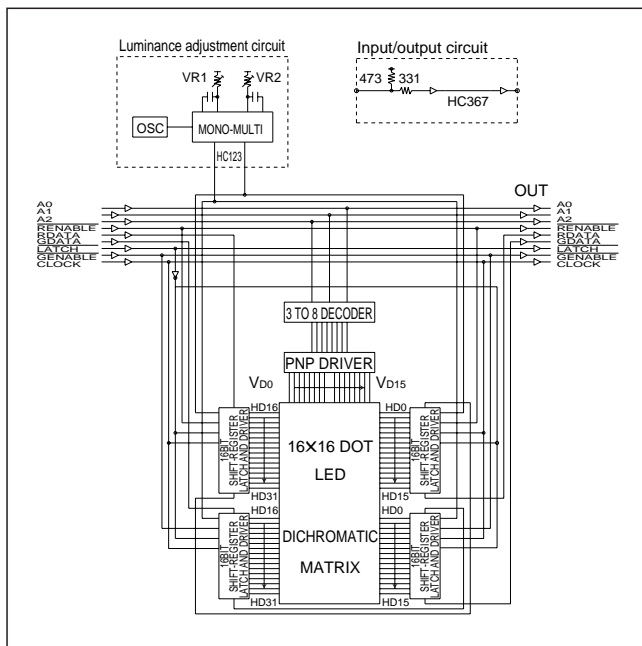
Luminance is classified into 2 ranks shown below.

(Vcc=5V, VLED=5V, Ta=25°C)

Radiation color	Rank		Unit
	1	2	
Red	450/700	550/1 000	cd/m <sup>2</sup>
Yellow-green	330/700	450/1 000	

Each figure in the table is the one of LT1455M/LT1456M in sequence.

## ■ Block Diagram



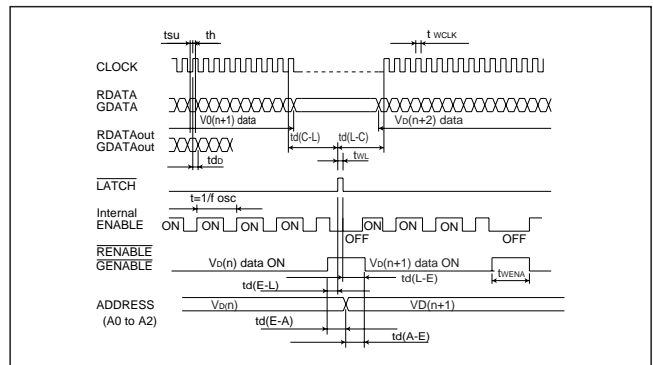
## ■ Electrical Characteristics

(Vcc=5V, VLED=5V, Ta=25°C)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage for IC	VCC	4.75	5.0	5.25	V
Supply voltage for LED	VLED	4.5	5.0	5.25	V
IC current dissipation	ICC	—	15	40	mA
LED current dissipation*1	ILED	—	3.5	3.9	A
Signal input voltage	VIH	3.5	—	—	V
	VIL	—	—	1.5	V
Signal input current	IiH	—	—	0.1	μA
	IiL	—	—	0.12	mA
Clock frequency	fCLK	—	—	3.0	MHz
Frame frequency	fFR	125	200	400	Hz

\*1 Under the condition that dichromatic all dots are lit.

## ■ Timing Chart



## ■ Recommended Timing Conditions

(Vcc=5.0V, Ta=25°C)

Parameter	Symbol	Rating			Unit	Remarks
		Min.	Typ.	Max.		
Clock pulse width	twCLK	100	—	—	ns	
Latch pulse width	tWL	80	—	—	ns	
Enable pulse width	twENA	2	—	—	μs	
Data setup time	tsu	80	—	—	ns	
Data hold time	th	40	—	—	ns	
Clock-latch time	td(C-L)	80	—	—	ns	
Latch-clock time	td(L-C)	150	—	—	ns	
Data output delay time	tdD	—	85	150	ns	RDATA, GDATA
Enable-latch time	td(E-L)	2	—	—	μs	
Latch-enable time	td(L-E)	2	—	—	μs	
Enable-address time	td(E-A)	2	—	—	μs	
Address-enable time	td(A-E)	20	—	—	μs	
Propagation delay time	tPLH, tPHL	—	15	40	ns	Except data terminal
Oscillation frequency	fOSC	—	25	—	kHz	
Enable frequency	fENA	—	—	3.2	kHz	*
Frame frequency	fFR	125	200	400	Hz	

\* When enable frame frequency is close to oscillation frequency, it causes flickering and unevenness of luminance.