FUJITSU
MICROELECTRONICS, INC.

MB8128

MB8128-10
MB8128-15

NMOS 16,384-BIT STATIC RANDOM ACCESS MEMORY

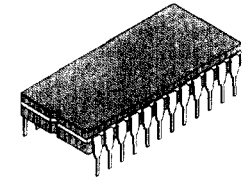
DESCRIPTION

The MB8128 is fabricated using N-channel silicon gate MOS technology. It uses fully static circuitry throughout and therefore requires no clocks or refreshing to operate.

MB8128 is designed for memory applications where high performance, low cost, large bit storage, and simple interfacing are required. The MB8128 is compatible with TTL logic families in all respects; inputs, outputs and a single +5V supply.

FEATURES

- **2048 words x 8-bit organization**
- **Static operation: no clocks or refresh required**
- **Fast access time:**
  MB8128-10 100 ns Max.
  MB8128-15 150 ns Max.
- **Single +5V supply voltage**
- **Common data inputs and outputs**
- **TTL compatible inputs and outputs**
- **Three-state output with OR-tie capability**
- **Chip Enable for simplified memory expansion**
- **Automatic power down**
- **Industry standard 24-pin DIP package**
- **Pin compatible with MB8416 (CMOS Static RAM) and MBM2716 (EPROM)**



CERDIP PACKAGE
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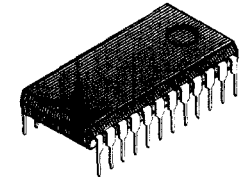
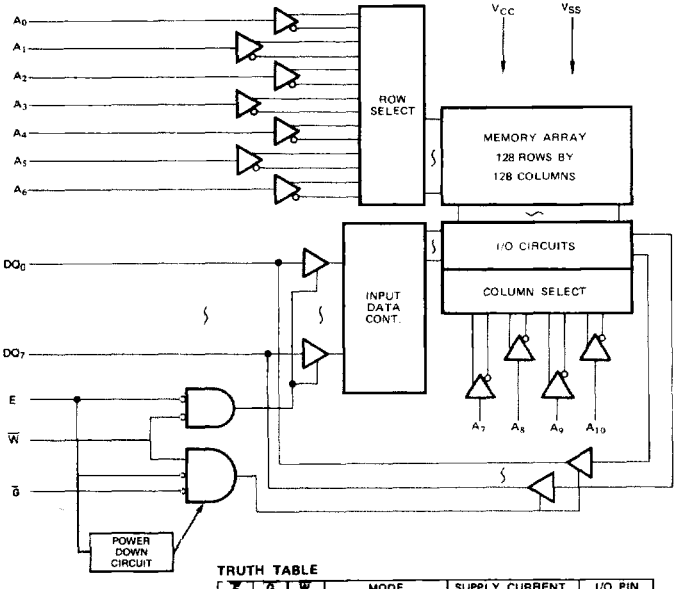


PLASTIC PACKAGE
DIP-24P-M01

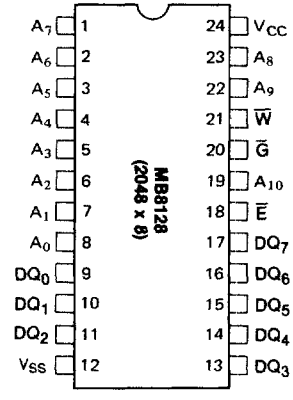
MB8128 BLOCK DIAGRAM



TRUTH TABLE

$\overline{E}$	$\overline{G}$	$\overline{W}$	MODE	SUPPLY CURRENT	I/O PIN
H	X	X	NOT SELECTED	I_{SB}	HIGH Z
L	H	H	D_{OUT} DISABLE	I_{CC}	HIGH Z
L	L	H	READ	I_{CC}	D_{OUT}
L	X	L	WRITE	I_{CC}	D_{IN}

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
Voltage on Any Pin With Respect to V_{SS}	V_{IN}, V_{OUT}, V_{CC}	− 3.5 to +7	V
Temperature Under Bias	T_A	− 10 to +85	°C
Storage Temperature	T_{STG}	− 65 to +150	°C
Power Dissipation	P_D	1.2	W

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. It is advised that normal precautions be taken to avoid application of any voltages higher than maximum rated voltages to this high impedance circuit.

RECOMMENDED OPERATING CONDITIONS (Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit	Ambient (1) Temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
Input Low Voltage	V_{IL}	−3.0	—	0.8	V	
Input High Voltage	V_{IH}	2.2	—	6.0	V	

NOTE: 1) The operating ambient temperature range is guaranteed with traverse airflow exceeding 2 linear meters/second.

DC CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Parameter			Symbol	Min	Typ	Max	Unit
Input Leakage Current (V_{IN} = V_{SS} to V_{CC}, V_{CC} = Max)			I_{LI}	−10	—	10	μA
Input/Output Leakage Current ($\overline{E}$ or $\overline{G}$ = V_{IH}, $V_{I/O}$ = V_{SS} to V_{CC}, V_{CC} = Max)			I_{LO}	−10	—	10	μA
Power Supply Current (V_{CC} = Max, $\overline{E}$ = V_{IL}, DQ = Open)	T_A = 25°C	MB8128-10	I_{CC}	—	70	—	mA
		MB8128-15		—	50	—	
	T_A = 0°C	MB8128-10		—	—	100	
		MB8128-15		—	—	70	
Output Low Voltage (I_{OL} = 2.1 mA)			V_{OL}	—	—	0.4	V
Output High Voltage (I_{OH} = − 1.0 mA)			V_{OH}	2.4	—	—	V
Standby Current (V_{CC} = Min to Max, $\overline{E}$ = V_{IH})		MB8128-10	I_{SB}	—	8	20	mA
		MB8128-15		—	6	15	
Peak Power-On Current (V_{CC} = V_{SS} to V_{CC} Min, $\overline{E}$ = Lower of V_{CC} or V_{IH} Min)		MB8128-10	I_{PO}	—	—	20	mA
		MB8128-15		—	—	15	

AC CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

READ CYCLE

Parameter	Symbol	MB8128-10			MB8128-15			Unit
		Min	Typ	Max	Min	Typ	Max	
Read Cycle Time	TAVAV	100	—	—	150	—	—	ns
Address Access Time	TAVQV	—	—	100	—	—	150	ns
Chip Enable Access Time	TELQV	—	—	100	—	—	150	ns
Output Hold from Address Change	TAXQX	15	—	—	20	—	—	ns
Chip Enable to Output Active	TELQX	0	—	—	0	—	—	ns
Chip Enable to Output in High Z	TEHQX	—	—	40	—	—	60	ns
Output Enable to Output Valid	TGLQV	—	—	50	—	—	60	ns
Output Enable to Output Active	TGLQX	10	—	—	10	—	—	ns
Output Enable to Output in High Z	TGLQZ	—	—	40	—	—	60	ns
Chip Select to Power Up Time	TELIH	0	—	—	0	—	—	ns
Chip Select to Power Down Time	TEHIL	—	—	40	—	—	60	ns

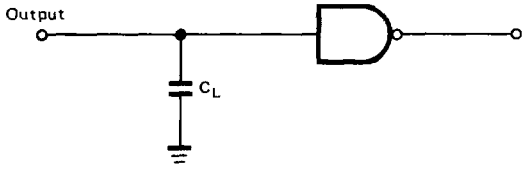
CAPACITANCE (T_A = 25°C, f = 1MHz)

R2

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (V_{IN} = 0V)	C_{IN}	—	5	pF
Input/Output Capacitance (V_{OUT} = 0V)	$C_{I/O}$	—	7	pF

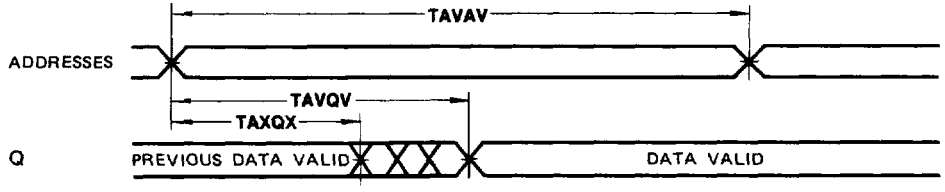
AC TEST CONDITIONS

Input Pulse Levels:	0.8V to 2.4V
Input Pulse Rise and Fall Time:	10 ns
Timing Measurement Reference Levels:	Input: 1.5V
	Output: 1.5V
Output Load:	1 TTL Gate and C_L = 100 pF

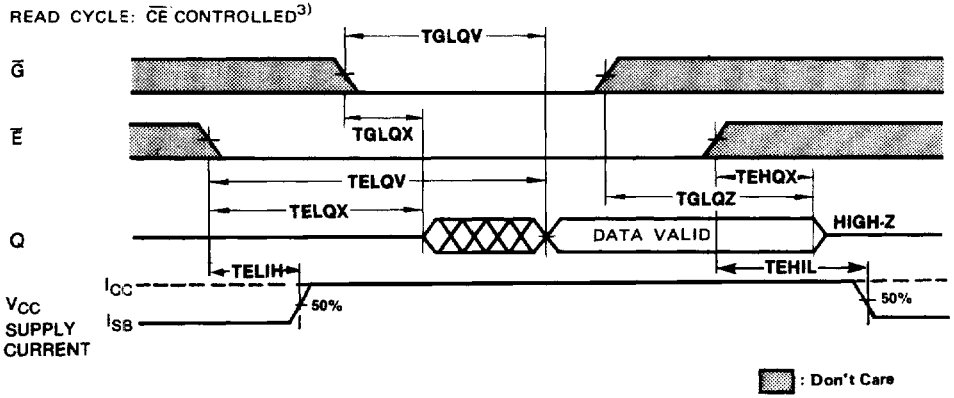


READ CYCLE

READ CYCLE: ADDRESS CONTROLLED[2]



READ CYCLE: $\overline{CE}$ CONTROLLED[3]



: Don't Care

: Undefined Data

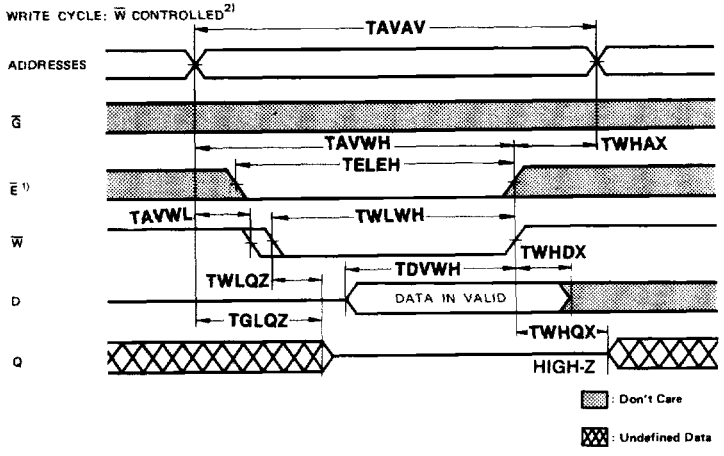
Note: 1) $\overline{W}$ is high for Read Cycle.
2) Device is continuously selected, $\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$.
3) Addresses valid prior to or coincident with $\overline{E}$ transition low.

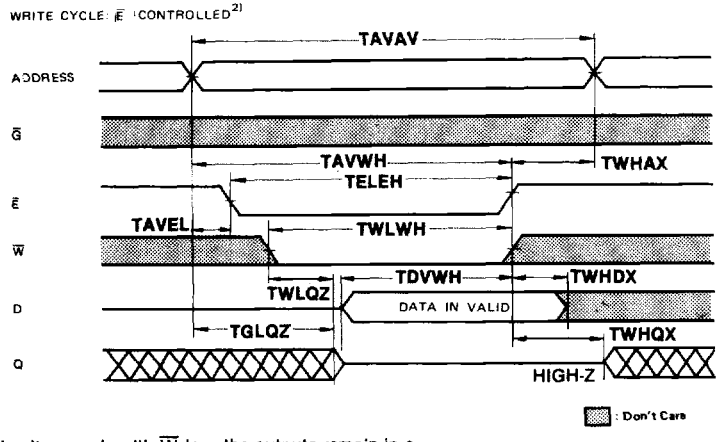
WRITE CYCLE

R 11

Parameter	Symbol	MB8128-10			MB8128-15			Unit
		Min	Typ	Max	Min	Typ	Max	
Write Cycle Time	TAVAV	100	—	—	150	—	—	ns
Address Valid to End of Write	TAVWH	95	—	—	140	—	—	ns
Chip Select to End of Write	TELEH	95	—	—	140	—	—	ns
Data Valid to End of Write	TDVWH	40	—	—	60	—	—	ns
Data Hold Time	TWHDX	5	—	—	5	—	—	ns
Write Pulse Width	TWLWH	85	—	—	130	—	—	ns
Write Recovery Time	TWHAX	5	—	—	10	—	—	ns
Address Setup Time	TAVWL	0	—	—	0	—	—	ns
	TAVEL	0	—	—	0	—	—	ns
Output Active From End of Write	TWHQX	10	—	—	10	—	—	ns
Write Enable to Output in High Z	TWLQZ	—	—	40	—	—	60	ns

WRITE CYCLE





Note: 1) If $\overline{E}$ goes low simultaneously with $\overline{W}$ low, the outputs remain in a high impedance state.
2) $\overline{E}$ or $\overline{W}$ must be high during address transitions.

OVERVIEW

The MB8128 from Fujitsu is a high performance part, designed for high speed and low system power requirements.

The high speed is obtained by advanced NMOS processing. The low system power requirements are achieved by the use of the MB8128 chip enable (active low). The MB8128 automatically enters standby operation drawing only I_{SB} whenever the chip enable is high. Upon activation of chip enable ($\overline{E}$ = LOW) the MB8128 automatically powers up. This automatic power up/down is an extremely useful feature. Care must be used as proper decoupling will minimize power line glitches.

Input and data bus lines are an additional area of concern. Unless bus lines are properly designed and terminated, cross coupling, cross talk and reflections can occur. Of particular importance is the undershoot on address lines. Once again, careful attention to good PC board layout and proper termination techniques will yield a well designed and reliable memory system.