P54/74FCT543/A (P54/74PCT543/A)
P54/74FCT544/A (P54/74PCT544/A)
OCTAL REGISTERED TRANSCEIVER

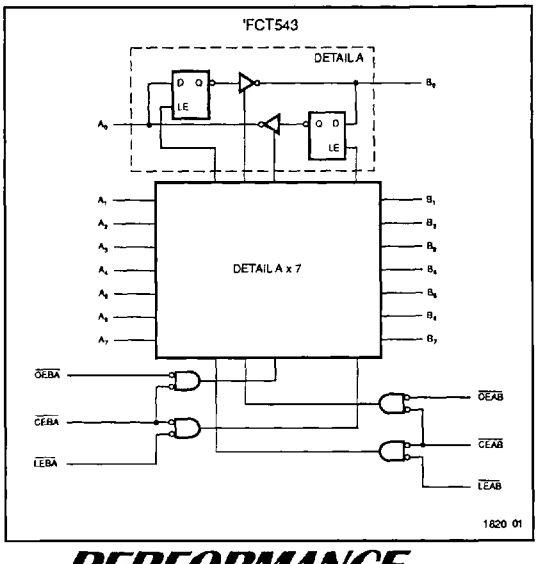
FEATURES

- Function, Pinout, and Drive Compatible with the FCT and F Logic
- FCT-A speed at 6.5ns max. (Com'l)
  FCT speed at 8.5ns max. (Com'l)
- CMOS V_{OH} Levels for Low Power Consumption — Typically 1/3 of FAST Bipolar Logic
- Edge-rate Control Circuitry for Significantly Improved Noise Characteristics
- ESD protection exceeds 2000V
- Inputs and Outputs Interface Directly with TTL, NMOS, and CMOS Devices
- Outputs Meet Levels Required for CMOS Static RAM Low Power Standby Mode
- 64 mA Sink Current (Com'l), 48 mA (Mil)
  15 mA Source Current (Com'l), 12 mA (Mil)
- Separate Controls for Data Flow in Each Direction
- Back to Back Latches for Storage
- 3-State Output
- Manufactured in 0.8 micron PACE Technology™

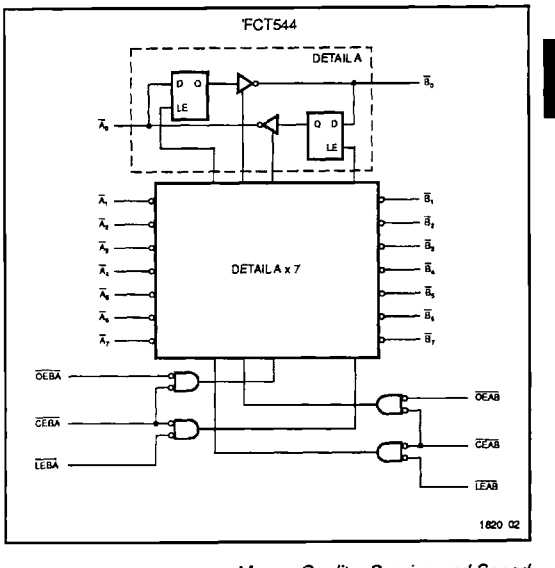
DESCRIPTION

The 'FCT543 and 'FCT544 Octal Registered Transceivers contain two sets of eight D-type latches with separate Latch Enable ($\overline{LEAB}$, $\overline{LEBA}$) and Output Enable ($\overline{OEAB}$, $\overline{OEBA}$) controls for each set to permit independent control of inputting and outputting in either direction of data flow. For data flow from A to B, for example, the A-to-B Enable ($\overline{CEAB}$) input must be LOW in order to enter data from A0–A7 or to take data from B0–B7, as indicated in the truth table. With $\overline{CEAB}$ LOW, a LOW signal on the A-to-B Latch Enable ($\overline{LEAB}$) input makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the $\overline{LEAB}$ signal puts the A latchs in the storage mode and their output no longer change with the A inputs. With $\overline{CEAB}$ and $\overline{OEAB}$ both LOW, the 3-state B output buffers are active and reflect the data present at the output of the A latches. Control of data from B to A is similar, but uses $\overline{CEAB}$, $\overline{LEAB}$ and $\overline{OEAB}$ inputs.

FUNCTIONAL BLOCK DIAGRAM



FUNCTIONAL BLOCK DIAGRAM



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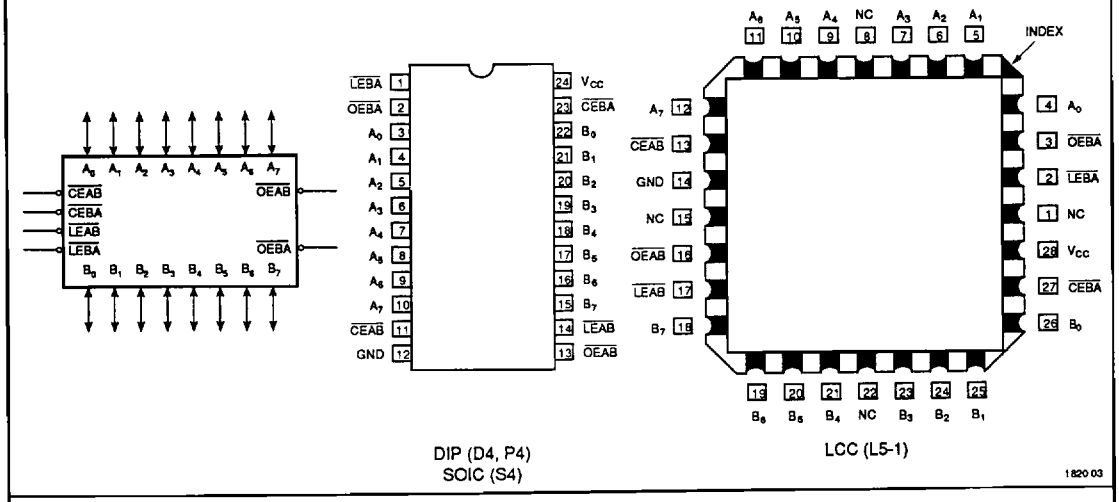
LOGIC SYMBOL AND PIN CONFIGURATIONS

'FCT543

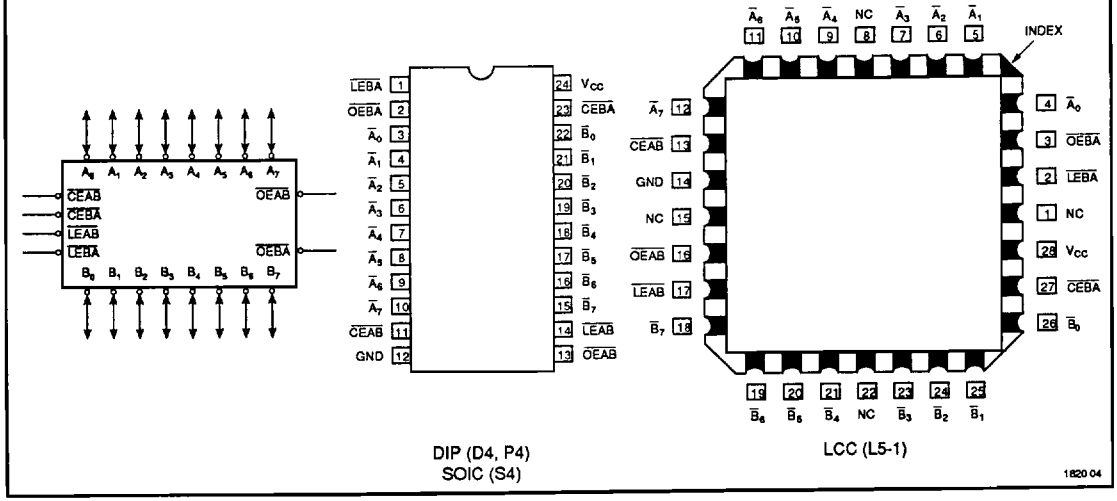


DIP (D4, P4)
SOIC (S4)

LCC (L5-1)

1820 03

'FCT544



DIP (D4, P4)
SOIC (S4)

LCC (L5-1)

1820 04

PIN DESCRIPTIONS

Pin Name	Description
$\overline{OEAB}$	A-to-B Output Enable Input (Active LOW)
$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
$\overline{CEAB}$	A-to-B Enable Input (Active LOW)
$\overline{CEBA}$	B-to-A Enable Input (Active LOW)
$\overline{LEAB}$	A-to-B Latch Enable Input (Active LOW)
$\overline{LEBA}$	B-to-A Latch Enable Input (Active LOW)
A_0–A_7	A-to-B Data Inputs or B-to-A 3-State Outputs
B_0–B_7	B-to-A Data Inputs or A-to-B 3-State Outputs

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ABSOLUTE MAXIMUM RATINGS[1,2]

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	–65 to +150	°C
T_A	Ambient Temperature Under Bias	–65 to +135	°C
V_{CC}	V_{CC} Potential to Ground	–0.5 to +7.0	V
I_{IN}	Input Current	–30 to +5.0	mA

1820 Tbl 02

Symbol	Parameter	Value	Unit
I_{OUTPUT}	Current Applied to Output	120	mA
V_{IN}	Input Voltage	–0.5 to V_{CC} + 0.5	V
V_{OUT}	Voltage Applied to Output	–0.5 to V_{CC} + 0.5	V

1820 Tbl 03

Notes:

1. Operation beyond the limits set forth in the above table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
2. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

RECOMMENDED OPERATING CONDITIONS

Free Air Ambient Temperature	Min	Max
Military	–55°C	+125°C
Commercial	0°C	+70°C

1820 Tbl 04

Supply Voltage (V_{CC})	Min	Max
Military	+4.5V	+5.5V
Commercial	+4.75V	+5.25V

1820 Tbl 05

DC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions)

Symbol	Parameter		Min	Typ[1]	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		
V_{IL}	Input LOW Voltage			0.8	V			
V_H	Hysteresis			0.35		V		All inputs
V_{CD}	Input Clamp Diode Voltage			–0.7	–1.2	V	MIN	I_{IN} = –18mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = 0.2V, or V_{CC} – 0.2V	V_{CC} – 0.2	V_{CC}		V		I_{OH} = –32µA
		Military/Commercial (CMOS)	V_{CC} – 0.2	V_{CC}		V	MIN	I_{OH} = –300µA
		Military (TTL)	2.4	4.3		V	MIN	I_{OH} = –12mA
		Commercial (TTL)	2.4	4.3		V	MIN	I_{OH} = –15mA
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = 0.2V, or V_{CC} – 0.2V		GND	0.2	V		I_{OL} = 300µA
		Military/Commercial (CMOS)		GND	0.2	V	MIN	I_{OL} = 300µA
		Military (TTL)		0.3	0.55	V	MIN	I_{OL} = 48mA
		Commercial (TTL)		0.3	0.55	V	MIN	I_{OL} = 64mA
I_{IH}	Input HIGH Current (Except I/O PIns)				5	µA	MAX	V_{IN} = V_{CC}
I_{IL}	Input LOW Current (Except I/O PIns)				–5	µA	MAX	V_{IN} = GND
I_{IH}	Input HIGH Current[3] (Except I/O PIns)				5	µA	MAX	V_{IN} = 2.7V
I_{IL}	Input LOW Current[3] (Except I/O PIns)				–5	µA	MAX	V_{IN} = 0.5V
I_{IH}	Input HIGH Current (I/O Pins only)				15	µA	MAX	V_{IN} = V_{CC}
I_{IL}	Input LOW Current (I/O Pins only)				–15	µA	MAX	V_{IN} = GND
I_{IH}	Input HIGH Current[3] (I/O Pins only)				15	µA	MAX	V_{IN} = 2.7V
I_{IL}	Input LOW Current[3] (I/O Pins only)				–15	µA	MAX	V_{IN} = 0.5V
I_{OS}	Output Short Circuit Current[2]		–60	–120		mA	MAX	V_{OUT} = 0.0V
C_{IN}	Input Capacitance[3]			5	10	pF		All inputs
C_{OUT}	Output Capacitance[3]			9	12	pF		All outputs

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Notes:

1. Typical limits are at V_{CC} = 5.0V, T_A = +25°C ambient.
2. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{os} tests should be performed last.
3. This parameter is guaranteed but not tested.

DC CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Typ.[1]	Max.	Units	Conditions
I_{CC}	Quiescent Power Supply Current (CMOS inputs)	0.003	0.5	mA	V_{CC} = MAX, f_1 = 0, Outputs Open, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC} - 0.2V$
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs)	0.5	2.0	mA	V_{CC} = MAX, V_{IN} = 3.4V[2], f_1 = 0, Outputs Open
I_{CCD}	Dynamic Power Supply Current[3]	0.15	0.25	mA/ mHz	V_{CC} = MAX, One Input Toggling, 50% Duty Cycle, $\overline{CEAB}$ + $\overline{OEAB}$ = Low, Outputs Open, $\overline{CEAB}$ = High, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC} - 0.2V$
I_C	Total Power Supply Current[5]	1.7	4.0	mA	V_{CC} = MAX, f_0 = 10MHz, $\overline{CEAB}$ + $\overline{OEAB}$ = Low 50% Duty Cycle, Outputs Open, $\overline{CEBA}$ = High One Bit Toggling at f_1 = 5MHz, $f_0 = \overline{LEAB}$ = 10MHz, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC} - 0.2V$
		2.2	6.0	mA	V_{CC} = MAX, f_0 = 10MHz, $\overline{CEAB}$ + $\overline{OEAB}$ = Low 50% Duty Cycle, Outputs Open, $\overline{CEBA}$ = High One Bit Toggling at f_1 = 5MHz, $f_0 = \overline{LEAB}$ = 10MHz, V_{IN} = 3.4V or V_{IN} = GND
		7.0	12.8[4]	mA	V_{CC} = MAX, f_0 = 10MHz, $\overline{CEAB}$ + $\overline{OEAB}$ = Low 50% Duty Cycle, Outputs Open, $\overline{CEBA}$ = High Eight Bits Toggling at f_1 = 5MHz, $f_0 = \overline{LEAB}$ = 10MHz, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC} - 0.2V$
		9.2	21.8[4]	mA	V_{CC} = MAX, f_0 = 10MHz, $\overline{CEAB}$ + $\overline{OEAB}$ = Low 50% Duty Cycle, Outputs Open, $\overline{CEBA}$ = High Eight Bits Toggling at f_1 = 5MHz, $f_0 = \overline{LEAB}$ = 10MHz, V_{IN} = 3.4V or V_{IN} = GND

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Notes:

1. Typical values are at V_{CC} = 5.0V, +25°C ambient.
2. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
3. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
4. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
5. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD}(f_0/2 + f_1 N_1)$
   I_{CC} = Quiescent Current with CMOS input levels
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_0 = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_1 = Input Frequency
   N_1 = Number of Inputs at f_1
   All currents are in milliamps and all frequencies are in megahertz.

TRUTH TABLE FOR A-TO-B (Symmetric with B-to-A)

Inputs			Latch Status	Outputs 'FCT543	Outputs 'FCT544
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{OEAB}$	A-TO-B	B0–B7	B0–B7
H	–	–	Storing	High Z	High Z
–	H	–	Storing	–	–
–	–	H	–	High Z	High Z
L	L	L	Transparent	Current A Inputs	Previous A Inputs
L	H	L	Storing	Previous A Inputs	Current A Inputs

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* = Before $\overline{LEAB}$ LOW-to-HIGH Transition
H = HIGH Voltage Level
L = LOW Voltage Level
– = Don't Care or Irrelevent
A-to-B data flow shown: B-to-A flow control is the same, except using $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$

AC CHARACTERISTICS

Sym.	Parameter	'FCT543 'FCT544				'FCT543A 'FCT544A				Units	Fig. No.
		MIL		COM'L		MIL		COM'L			
		Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.		
t_{PLH} t_{PHL}	Propagation Delay Transparent Mode A_n to B_n or B_n to A_n	2.0	10.0	2.5	8.5	2.5	7.5	2.5	6.5	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay $\overline{LEBA}$ to A_n $\overline{LEAB}$ to B_n	2.5	14.0	2.5	12.5	2.5	9.0	2.5	8.0	ns	1, 5
t_{PZH} t_{PZL}	Output Enable Time $\overline{OEBA}$ or $\overline{OEAB}$ to A_n or B_n $\overline{CEBA}$ or $\overline{CEAB}$ to A_n or B_n	2.0	14.0	2.0	12.0	2.0	10.0	2.0	9.0	ns	1,7,8
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OEBA}$ or $\overline{OEAB}$ to A_n or B_n $\overline{CEBA}$ or $\overline{CEAB}$ to A_n or B_n	2.0	13.0	2.0	9.0	2.0	8.5	2.0	7.5	ns	1,7,8

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Note: Minimum limits are guaranteed on Propagation Delays.

AC OPERATING REQUIREMENTS

Sym.	Parameter	'FCT543 'FCT544				'FCT543A 'FCT544A				Units	Fig. No.
		MIL		COM'L		MIL		COM'L			
		Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.		
t_s (H) t_s (L)	Set-up Time HIGH or LOW A_n or B_n to $\overline{LEBA}$ or $\overline{LEAB}$	3.0	—	3.0	—	2.0	—	2.0	—	ns	9
t_h (H) t_h (L)	Hold Time HIGH or LOW A_n or B_n to $\overline{LEBA}$ or $\overline{LEAB}$	2.0	—	2.0	—	2.0	—	2.0	—	ns	9
t_w	$\overline{LEBA}$ or $\overline{LEAB}$ Pulse Width LOW	5.0	—	5.0	—	5.0	—	5.0	—	ns	6

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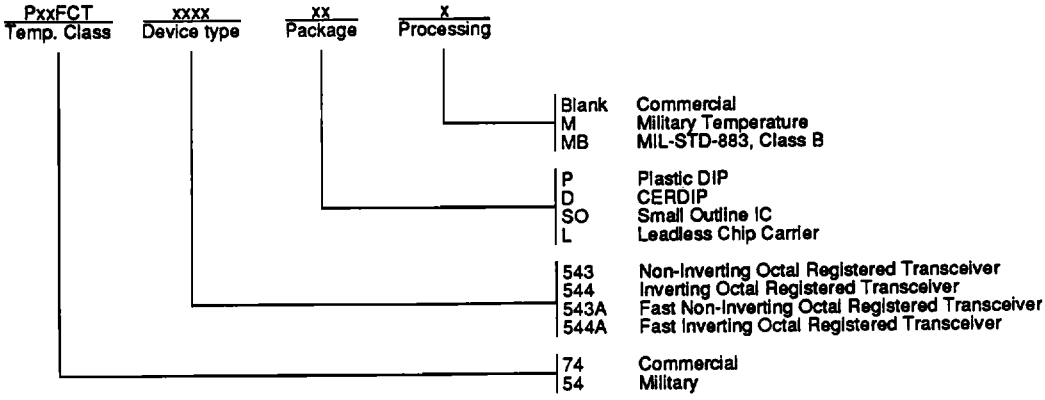
ORDERING INFORMATION



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