GOULD

AMI Semiconductors

16-Bit, 16 μs Self-Calibrating A/D Converter

S5016

Features

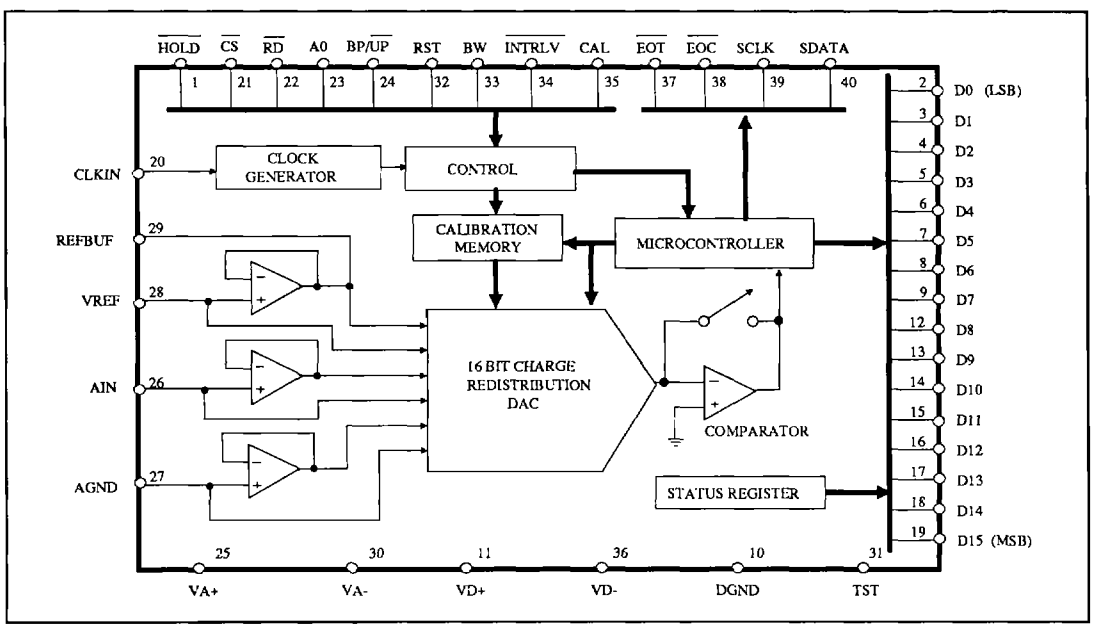
- Monolithic CMOS A/D Converter
  - Microprocessor Compatible
  - Parallel and Serial Output
  - Inherent Track/Hold Input
- True 16-Bit Precision
  - Linearity Error: 0.001% FS
  - No Missing Codes
- Ultra-Low Distortion
  - Total Harmonic Distortion: 0.001%
  - *Peak Harmonic or Noise: -104 dB*
- 16.25 μs Conversion Time
  - Sample Rates up to 50 kHz
- Self Calibration Maintains Accuracy Over Time and Temperature
- Low Power Dissipation: 120 mW
- Pin Compatible with S5012/S5014
- Second Sourced by Crystal's CS5016

General Description

The S5016 is a 16-bit monolithic analog to digital converter with a 16.25 μs conversion time. Unique self-calibration circuitry insures maximum nonlinearity of 0.001% FS and no missing codes. This insures low distortion and maintains good signal to noise performance with low-level signals. Offset and full scale errors are kept within 1 LSB, eliminating the need for manual calibration of any kind. Unipolar and bipolar input ranges are digitally selectable.

The S5016 consists of a DAC, conversion and calibration microcontroller, oscillator, comparator, microprocessor compatible 3-state I/O, and calibration circuitry. The input track-and-hold, inherent to the device's sampling architecture, acquires the analog input signal after each conversion within 3.75 μs to 0.01%, allowing throughput rates up to 50 kHz.

An evaluation board (DB5016) is available for the S5016 which can be easily configured to simulate any combination of operating conditions to greatly simplify system design and testing.



A/D Converters

Analog Characteristics (T_A = 25 °C; VA+, VD+ = 5V; VA-, VD- = -5V; VREF = 4.5V; f_{clk} = 4 MHz for -16, 2 MHz for -32; Analog Source Impedance = 200 Ω; Synchronous Sampling.)

Parameter *			S5016 -J,K min	S5016 -J,K typ	S5016 -J,K max	S5016 -A,B min	S5016 -A,B typ	S5016 -A,B max	S5016 -S,T min	S5016 -S,T typ	S5016 -S,T max	Units
Specified Temperature Range			0 to +70			-40 to +85			-55 to +125			°C
Accuracy												
Linearity Error	(Note 1)	-J,A,S		0.002	0.003		0.002	0.003		0.002	0.0076	% FS
		-K,B,T		0.001	0.0015		0.001	0.0015		0.001	0.0015	% FS
	(Note 3)	Drift		± 1/4			± 1/4			± 1/4		ΔLSB
Differential Linearity		(Note 2)	16			16			16			Bits
Full Scale Error	(Note 1)	-J,A,S		± 2	± 3		± 2	± 3		± 2	± 4	LSB
		-K,B,T		± 2	± 3		± 2	± 3		± 2	± 3	LSB
	(Note 3)	Drift		± 1			± 1			± 2		ΔLSB
Unipolar Offset	(Note 1)	-J,A,S		± 1	± 2		± 1	± 3		± 1	± 4	LSB
		-K,B,T		± 1	± 3/2		± 1	± 3		± 1	± 3	LSB
	(Note 3)	Drift		± 1			± 1			± 2		ΔLSB
Bipolar Offset	(Note 1)	-J,A,S		± 1	± 2		± 1	± 2		± 1	± 4	LSB
		-K,B,T		± 1	± 3/2		± 1	± 2		± 1	± 2	LSB
	(Note 3)	Drift		± 1			± 2			± 2		ΔLSB
Bipolar Negative Full-Scale Error	(Note 1)	-J,A,S		± 2	± 3		± 2	± 3		± 2	± 5	LSB
		-K,B,T		± 2	± 3		± 2	± 3		± 2	± 3	LSB
	(Note 3)	Drift		± 1			± 2			± 2		ΔLSB
Dynamic Performance		(Bipolar Mode)										
Peak Harmonic or Spurious Noise												
Full-Scale, 1kHz Input	(Note 1)	-J,A,S	96	100		96	100		92	100		dB
		-K,B,T	100	104		100	104		100	104		dB
Full-Scale, 12kHz Input		-J,A,S	85	88		85	88		82	88		dB
		-K,B,T	85	91		85	91		85	91		dB
Total Harmonic Distortion												
Full-Scale, 1kHz Input		-J,A,S		0.002			0.002			0.002		%
		-K,B,T		0.001			0.001			0.001		%
Signal-to-Noise Ratio												
1kHz, 0dB Input	(Note 1, 4)	-J,A,S	87	90		87	90		84	90		dB
		-K,B,T	90	92		90	92		90	92		dB
1kHz, -60dB Input		-J,A,S		30			30			30		dB
		-K,B,T		32			32			32		dB
Noise (Note 5)		Unipolar Mode		35			35			35		uV_{rms}
		Bipolar Mode		70			70			70		uV_{rms}

Notes:
1. Applies after calibration at any temperature within the specified temperature range.
2. Minimum resolution for which no missing codes is guaranteed
3. Total drift over specified temperature range since calibration at power-up at 25 °C.
4. Refer to Figure 16 for a detailed plot of S/(N+D) vs. Input Amplitude.
5. Wideband noise aliased into the baseband. Referred to the input.

* Refer to *Parameter Definitions* (immediately following the pin descriptions at the end of this data sheet).

Specifications are subject to change without notice.

Analog Characteristics (continued)

Parameter *	S5016 -J,K min	S5016 -J,K typ	S5016 -J,K max	S5016 -A,B min	S5016 -A,B typ	S5016 -A,B max	S5016 -S,T min	S5016 -S,T typ	S5016 -S,T max	Units
Specified Temperature Range		0 to +70			-40 to +85			-55 to +125		°C
Analog Input										
Aperture Time		25			25			25		ns
Aperture Jitter		100			100			100		ps
Aperture Time Matching (Note 6)		TBD			TBD			TBD		ns
Input Capacitance (Note 7)										
Unipolar Mode		275	375		275	375		275	375	pF
Bipolar Mode		165	220		165	220		165	220	pF
Conversion & Throughput										
Conversion Time −16			16.25			16.25			16.25	us
(Notes 8, 9) −32			32.5			32.5			32.5	us
Acquisition Time −16		3.0	3.75		3.0	3.75		3.0	3.75	us
(Note 9) −32		4.5	5.25		4.5	5.25		4.5	5.25	us
Throughput −16		50			50			50		kHz
(Note 9) −32		26.5			26.5			26.5		kHz
Power Supplies										
Power Supply Currents (Note 10)										
I_{A+}		9	19		9	19		9	19	mA
I_{A-}		−9	−19		−9	−19		−9	−19	mA
I_{D+}		3	6		3	6		3	6	mA
I_{D-}		−3	−6		−3	−6		−3	−6	mA
Power Dissipation (Note 10)		120	250		120	250		120	250	mW
Power Supply Rejection (Note 11)										
Positive Supplies		84			84			84		dB
Negative Supplies		84			84			84		dB

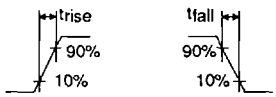
Notes:
6. Part to part.
7. Applies only in track mode. When converting or calibrating, input capacitance will not exceed 15 pF.
8. Measured from falling transition on $\overline{HOLD}$ to falling transition on $\overline{EOC}$.
9. Conversion, acquisition, and throughput times depend on the master clock, sampling, and calibration conditions. The numbers shown assume sampling and conversion is synchronized with the CS5016's conversion clock, interleave calibrate is disabled, and operation is from the full-rated, external clock. Refer to the section *Conversion Time/Throughput* for a detailed discussion of conversion timing.
10. All outputs unloaded. All inputs CMOS levels.
11. With 300 mV p-p, 1 kHz ripple applied to each analog supply separately in bipolar mode. Rejection improves by 6 dB in the unipolar mode to 90 dB. Figure 22 shows a plot of typical power supply rejection versus frequency.

Switching Characteristics ($T_A = T_{min}$ to T_{max};

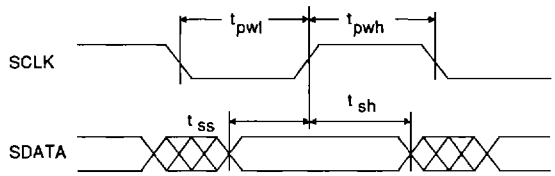
VA+, VD+ = 5V ± 10%; VA-, VD- = -5V ± 10%; Inputs: Logic 0 = 0V, Logic 1 = VD+; C_L = 50 pF; BW = VD+)

Parameter	Symbol	Min	Typ	Max	Units
Master Clock Frequency:					
Internally Generated: J,K,A,B, -16	f_{CLK}	2	-	-	MHz
S,T, -16		1.75	-	-	
-32		1	-	-	
Externally Supplied: -16		100 kHz	-	4	
-32		100 kHz	-	2	
Master Clock Duty Cycle	-	40	-	60	%
Rise Times: Any Digital Input	t_{rise}	-	-	1.0	us
Any Digital Output		-	20	-	ns
Fall Times: Any Digital Input	t_{fall}	-	-	1.0	us
Any Digital Output		-	20	-	ns
$\overline{HOLD}$ Pulse Width	t_{hpw}	$1/f_{CLK} + 50$	-	t_c	ns
Conversion Time	t_c	$65/f_{CLK}$	-	$69/f_{CLK} + 235$	ns
Data Delay Time	t_{dd}	-	40	100	ns
$\overline{EOC}$ Pulse Width (Note 12)	t_{epw}	$4/f_{CLK} - 20$	-	-	ns
Set Up Times: CAL, $\overline{INTRLV}$ to $\overline{CS}$ Low	t_{cs}	20	10	-	ns
A0 to $\overline{CS}$ and $\overline{RD}$ Low	t_{as}	20	10	-	
Hold Times:					
$\overline{CS}$ or $\overline{RD}$ High to A0 Invalid	t_{ah}	50	30	-	ns
$\overline{CS}$ High to CAL, $\overline{INTRLV}$ Invalid	t_{ch}	50	30	-	
Access Times: $\overline{CS}$ Low to Data Valid					
-J,K,A,B	t_{ca}	-	90	120	ns
-S,T		-	115	150	
$\overline{RD}$ Low to Data Valid					
-J,K,A,B	t_{ra}	-	90	120	ns
-S,T		-	115	150	
Output Float Delay: -J,K,A,B	t_{fd}	-	90	110	ns
$\overline{CS}$ or $\overline{RD}$ High to Output Hi-Z -S,T			90	140	
Serial Clock Pulse Width Low	t_{pwl}	-	$2/f_{CLK}$	-	ns
Pulse Width High	t_{pwh}	-	$2/f_{CLK}$	-	
Set Up Times: SDATA to SCLK Rising	t_{ss}	$2/f_{CLK} - 50$	$2/f_{CLK}$	-	ns
Hold Times: SCLK Rising to SDATA	t_{sh}	$2/f_{CLK} - 100$	$2/f_{CLK}$	-	ns

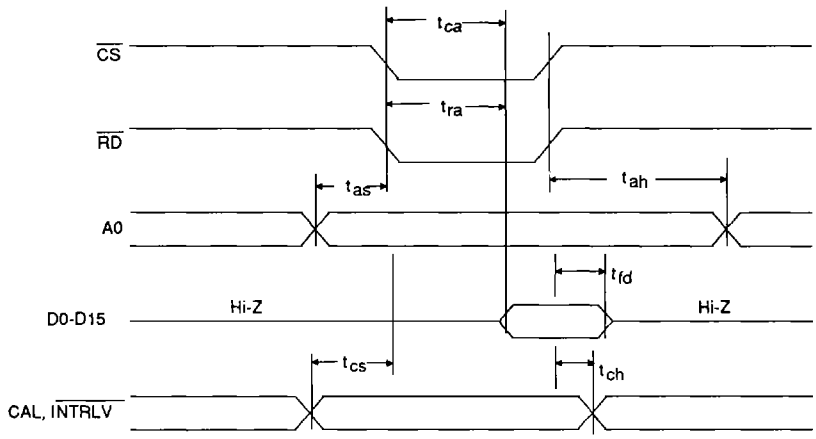
Note: 12. $\overline{EOC}$ remains low 4 master clock cycles if $\overline{CS}$ and $\overline{RD}$ are held low. Otherwise, it returns high within 4 master clock cycles from the start of a data read operation or a conversion cycle.



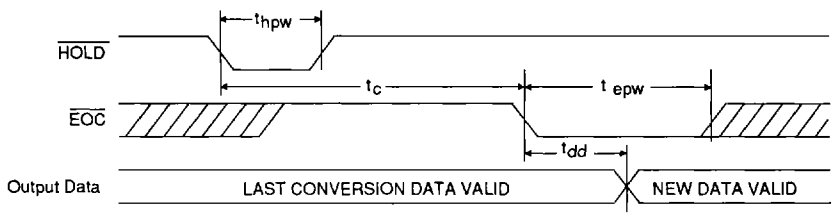
Rise and Fall Times



Serial Output Timing



Read and Calibration Control Timing



Conversion Timing

Digital Characteristics ($T_A = T_{min}$ to T_{max}; VA+, VD+ = 5V ± 10%; VA-, VD- = -5V ± 10%) All measurements below are performed under static conditions.

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage	V_{IH}	2.0	–	–	V
Low-Level Input Voltage	V_{IL}	–	–	0.8	V
High-Level Output Voltage (Note 13)	V_{OH}	(VD+) - 1.0V	–	–	V
Low-Level Output Voltage Iout=1.6mA	V_{OL}	–	–	0.4	V
Input Leakage Current	I_{in}	–	–	10	uA
3-State Leakage Current	I_{OZ}	–	–	±10	uA
Digital Output Pin Capacitance	C_{out}	–	9	–	pF

Note. 13 I_{out} = -100 µA. This specification guarantees TTL compatability (V_{OH} = 2.4V @ I_{out} = -40 µA).

Recommended Operating Conditions (AGND, DGND = 0V, see note 14.)

Parameter		Symbol	Min	Typ	Max	Units
DC Power Supplies:	Positive Digital	VD+	4.5	5.0	VA+	V
	Negative Digital	VD-	−4.5	−5.0	−5.5	V
	Positive Analog	VA+	4.5	5.0	5.5	V
	Negative Analog	VA-	−4.5	−5.0	−5.5	V
Analog Reference Voltage		VREF	2.5	4.5	(VA+) - 0.5	V
Analog Input Voltage:	Unipolar	V_{AIN}	AGND	–	VREF	V
(Note 15)	Bipolar	V_{AIN}	-VREF	–	VREF	V

Notes: 14. All voltages with respect to ground.
15. The S5016 can accept input voltages up to the analog supplies (VA+ and VA-). It will output all 1's for inputs above VREF and all 0's for inputs below AGND in unipolar mode and -VREF in bipolar mode.

Absolute Maximum Ratings (AGND, DGND = 0V, all voltages with respect to ground.)

Parameter		Symbol	Min	Max	Units
DC Power Supplies:	Positive Digital	VD+	−0.3	(VA+) + 0.3	V
	Negative Digital	VD-	0.3	−6.0	V
	Positive Analog	VA+	−0.3	6.0	V
	Negative Analog	VA-	0.3	−6.0	V
Input Current, Any Pin Except Supplies (Note 16)		I_{in}	–	±10	mA
Analog Input Voltage (AIN and VREF pins)		V_{INA}	(VA-) - 0.3	(VA+) + 0.3	V
Digital Input Voltage		V_{IND}	-0.3	(VA+) + 0.3	V
Ambient Operating Temperature		T_A	-55	125	°C
Storage Temperature		T_{stg}	-65	150	°C

Note: 16 Transient currents of up to 100 mA will not cause SCR latch-up.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Theory of Operation

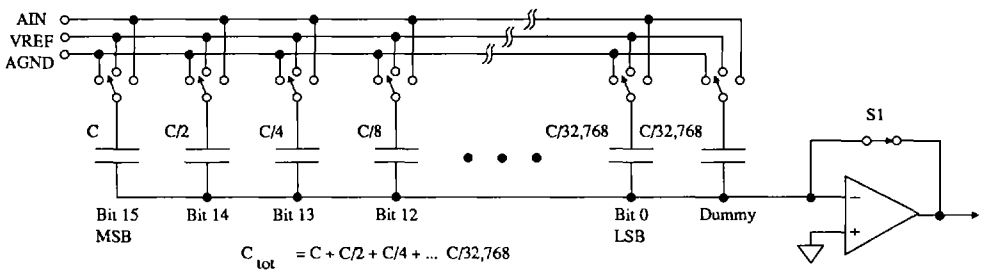


Figure 1. Charge Redistribution DAC

The S5016 utilizes a successive approximation conversion technique. The analog input is successively compared to the output of a D/A converter controlled by the conversion algorithm. Successive approximation begins by comparing the analog input to the DAC output which is set to half-scale (MSB on, all other bits off). If the input is found to be below half-scale, the MSB is reset to zero and the input is compared to one-quarter scale (next MSB on, all others off). If the input were above half-scale, the MSB would remain high and the next comparison would be at three-quarters of full scale. This procedure continues until all bits have been exercised.

The S5016 implements the successiveapproximation algorithm using a unique charge redistribution architecture. Instead of the traditional resistor network, the DAC is an array of binary-weighted capacitors. All capacitors in the array share a common node at the comparator's input. Their other terminals are capable of being connected to AIN, AGND, or VREF (Figure 1). When the device is not calibrating or converting, all capacitors are tied to AIN forming C_{tot}. Switch S1 is closed and the charge on the array, Q_{in}, tracks the input signal V_{in} (Figure 2a).

When the conversion command is issued, switch S1 opens as shown in Figure 2b. This traps charge Q_{in} on the comparator side of the capacitor array and creates a floating node at the comparator's input. The conversion algorithm operates on this fixed charge, and the signal at the analog input pin is ignored. In effect, the entire DAC capacitor array serves as analog memory during conversion much like a hold capacitor in a sample/hold amplifier.

The conversion consists of manipulating the free plates of the capacitor array to VREF and AGND to form a capacitive divider. Since the charge at the floating node remains fixed, the voltage at that point

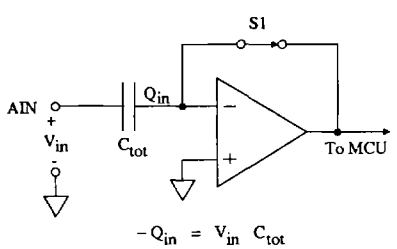


Figure 2a. Tracking Mode

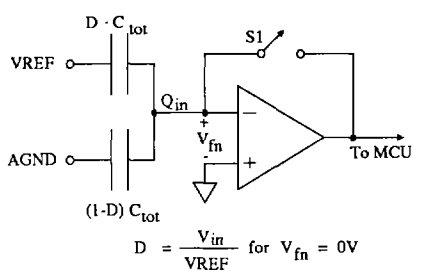


Figure 2b. Convert Mode

depends on the proportion of capacitance tied to VREF versus AGND. The successive-approximation algorithm is used to find the proportion of capacitance, termed D in Figure 2b, which when connected to the reference will drive the voltage at the floating node (V_{fn}) to zero. That binary fraction of capacitance represents the converter's digital output.

The S5016's charge redistribution architecture easily supports bipolar input ranges. If half the capacitor array (the MSB capacitor) is tied to VREF rather than AIN in the track mode, the input range is doubled and is offset half-scale. The magnitude of the reference voltage thus defines both positive and negative full-scale (-VREF to +VREF), and the digital code is an offset binary representation of the input.

Calibration

The ability of the S5016 to convert accurately to 16-bits clearly depends on the accuracy of its comparator and DAC. The S5016 utilizes an "auto-zeroing" scheme to null errors introduced by the comparator. All offsets are stored on the capacitor array while in the track mode and are effectively subtracted from the input signal when a conversion is initiated. Auto-zeroing enhances power supply rejection at frequencies well below the conversion rate.

To achieve 16-bit accuracy from the DAC, the S5016 uses a novel self-calibration scheme. Each bit capacitor shown in Figure 1 actually consists of several capacitors which can be manipulated to adjust the overall bit weight. An on-chip microcontroller adjusts the subarrays to precisely ratio the bits. Each bit is adjusted to just balance the sum of all less significant bits plus one dummy LSB (for example, 16C = 8C + 4C + 2C + C + C). During calibration, the S5016 implements statistical noise reduction to calibrate accurately to ± 1/4 LSB. It performs multiple experiments per calibration decision to reduce the effective noise bandwidth and the probability of making an incorrect decision.

Digital Circuit Connections

The S5016 can be applied in a wide variety of master clock, sampling, and calibration conditions which directly affect the device's conversion time and throughput. The device also features on-chip 3-state output buffers and a complete interface for connecting to 8-bit and 16-bit digital systems. Output data is also available in serial format.

Master Clock

The S5016 operates from a master clock which can be externally supplied or internally generated. The internal oscillator is activated by externally tying the CLKIN input low. Alternatively, the S5016 can be synchronized to the external system by driving the CLKIN pin with a TTL or CMOS clock signal.

All calibration, conversion, and throughput times directly scale to master clock frequency. Thus, throughput can be precisely controlled and/or maximized using an external master clock. In contrast, the S5016's internal oscillator will vary from unit-to-unit and over temperature. Its tolerance gives rise to minimum and maximum conversion times and throughput rates. The -16 version of the S5016 is specified for accurate operation with an external clock up to 4 MHz; its internal clock frequency is specified at a minimum of 2 MHz. The -32 version can handle external clocks up to 2 MHz; its internal clock can range as low as 1 MHz (see the table, *Switching Characteristics*, at the front of this data sheet). Both versions can typically convert with clocks as low as 10 kHz at room temperature.

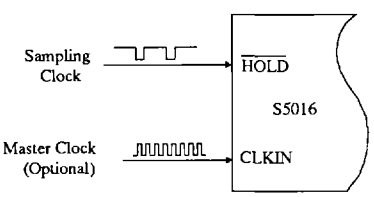


Figure 3a. Asynchronous Sampling

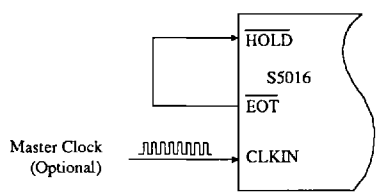


Figure 3b. Synchronous Sampling

Initiating Conversions

A falling transition on the $\overline{HOLD}$ pin places the input in the hold mode and initiates a conversion cycle. Upon completion of the conversion cycle, the S5016 automatically returns to the track mode. In contrast to systems with separate track-and-holds and A/D converters, a sampling clock can simply be connected to the $\overline{HOLD}$ input (Figure 3a). The duty cycle of this clock is not critical. It need only remain low at least one master clock cycle plus 50 ns, but no longer than the minimum conversion time or an additional conversion cycle will be initiated with inadequate time for acquisition.

Microprocessor-Controlled Operation

Sampling and conversion can be placed under microprocessor control (Figure 4) by simply gating the device's decoded address with the write strobe for the $\overline{HOLD}$ input. Thus, a write cycle to the S5016's base address will initiate a conversion. However, the write cycle must be to the odd address (A0 high) to avoid initiating a software controlled reset (see *Reset* below).

The calibration control inputs, CAL, and $\overline{INTRLV}$ are also internally latched by $\overline{CS}$, so they must be in the appropriate state whenever the chip is selected during a read or write cycle. Address lines A1 and A2 are shown connected to CAL and $\overline{INTRLV}$ in Figure 4 placing calibration under microprocessor control as well. Thus, any read or write cycle to the S5016's base address will initiate or terminate calibration. Alternatively, A0, $\overline{INTRLV}$, and CAL may be connected to the microprocessor data bus.

Conversion Time/Throughput

Upon completing a conversion cycle and returning to the track mode, the S5016 requires time to acquire the analog input signal before another conversion can be initiated. The acquisition time is specified as six master clock cycles plus 2.25 µs. This adds to the conversion time to define the converter's maximum throughput. The conversion time of the S5016, in turn, depends on the sampling, calibration, and master clock conditions.

Asynchronous Sampling

The S5016 internally operates from a clock which is delayed and divided down from the master clock ($f_{CLK}/4$). If sampling is not synchronized to this internal clock, the conversion cycle may not begin until up to four clock cycles after $\overline{HOLD}$ goes low *even though the charge is trapped immediately.* In this asynchronous mode (Figure 3a), the four clock cycles add to the minimum 65 clock cycles to define the maximum conversion time (see Figure 5a and Table 1).

Synchronous Sampling

To achieve maximum throughput, sampling can be synchronized with the internal conversion clock by connecting the End-of-Track ($\overline{EOT}$) output to $\overline{HOLD}$ (Figure 3b). The $\overline{EOT}$ output falls 15 master clock cycles after $\overline{EOC}$ indicating the analog input has been acquired to the S5016's specified accuracy. The $\overline{EOT}$ output is synchronized to the internal conversion clock, so the four clock cycle synchronization uncertainty is removed yielding throughput at 1/80th of the master clock frequency (see Figure 5b and Table 1).

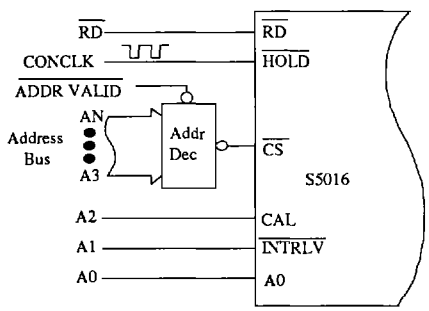


Figure 4a. Conversions Asynchronous to Master Clock

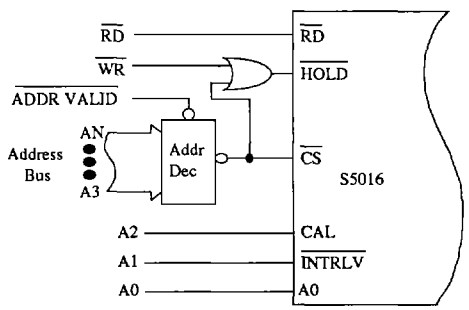


Figure 4b. Conversions under Microprocessor Control

A/D Converters

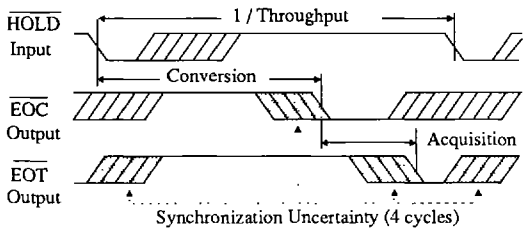
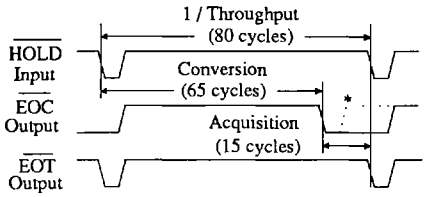


Figure 5a. Asynchronous Sampling (External Clock)



* Dashed line : $\overline{CS}$ & $\overline{RD}$ = 0
Solid line: See Figure 9.

Figure 5b. Synchronous (Loopback) Mode

Also, the S5016's internal RC oscillator exhibits significant jitter (typically ± 0.05% of its period), which is high compared to crystal oscillators. If the S5016 is configured for synchronous sampling while operating from its internal oscillator, this jitter will directly affect sampling purity.

Reset

Upon power up, the S5016 must be reset to guarantee a consistent starting condition and initially calibrate the device. Due to the S5016's low power dissipation and low temperature drift, no warm-up time is required before reset to accommodate any self-heating effects. However, the voltage reference input should have stabilized to within 0.25% of its final value before RST falls to guarantee an accurate calibration. Later, the S5016 may be reset at any time to initiate a single full calibration. Reset overrides all other functions. If reset, the S5016 will clear and initiate a new calibration cycle mid-conversion or mid-calibration.

Resets can be initiated in hardware or software. The simplest method of resetting the S5016 involves strobing the RST pin high for at least 100 ns. When RST is brought high all internal logic clears. When it returns low a full calibration begins which takes 1,441,020 master clock cycles (approximately 360 ms with a 4 MHz clock) to complete. A simple power-on reset circuit can be built using a resistor and capacitor, and a Schmitt-trigger inverter to prevent oscillation (see Figure 6). The S5016 can also be reset in software when under microprocessor control. The S5016 will reset whenever $\overline{CS}$, A0, and $\overline{HOLD}$ are taken low simultaneously. See the *Microprocessor Interface* section (below) to eliminate the possibility of inadvertent software reset. The $\overline{EOC}$ output remains high throughout the reset operation and will fall upon its completion. It can thus be used to generate an interrupt indicating the S5016 is ready for operation. Six master clock cycles plus 2.25 µs must be allowed after $\overline{EOC}$ falls to allow for acquisition. Under microprocessor-independent operation with 3-states permanently enabled ($\overline{CS}$, $\overline{RD}$ low; A0 high) the $\overline{EOC}$ output will not fall at the completion of the reset operation.

Initiating Calibration

All modes of calibration can be controlled in hardware or software. Accuracy can thereby be insured at any time or temperature throughout operating life. After initial calibration at power-up, the S5016's charge-redistribution design yields better temperature drift and more graceful aging than resistor-based technologies, so calibration is normally only required once, after power-up.

Sampling Mode	Conversion Time Min	Conversion Time Max	Throughput Time Min	Throughput Time Max
Synchronous (Loopback)	65 t_{clk}	65 t_{clk}	80 t_{clk}	80 t_{clk}
Asynchronous	65 t_{clk}	69 t_{clk} + 235 ns	N/A	75 t_{clk} + 2 25 us

Table 1. Conversion and Throughput Times (t_{clk} = Master Clock Period)

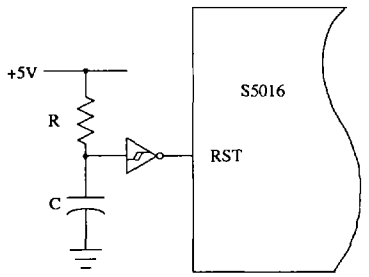


Figure 6. Power-On Reset Circuit

The first mode of calibration, reset, results in a single full calibration cycle. The second type of calibration, "burst" cal, is useful when the ADC sees some downtime but not enough to perform a full reset calibration. Burst cal can be terminated mid-calibration; it picks up where it left off previously, so calibrations can be done in piecemeal fashion. Burst cal is initiated by bringing the CAL input high with $\overline{CS}$ low. The CAL input is level-triggered and latches on the rising edge of $\overline{CS}$, so a write cycle can be used to control calibration in software. Burst cal will continue to loop through calibration cycles until terminated. Once CAL returns low, at least 26 master clock cycles plus 2.25 µs (8.75 µs @ 4 MHz clock) must be allowed before a conversion is initiated to ensure the S5016 has completed its calibration experiment and has acquired the analog input. The $\overline{EOC}$ output indicates the completion of the final calibration experiment. (See the *Addendum* which appends this data sheet.)

The S5016 features a background calibration mode called "interleave." Interleave appends a single calibration experiment to each conversion cycle and thus requires no dead time for calibration. The S5016 gathers data between conversions and will adjust its transfer function once it completes the entire sequence of experiments (one calibration cycle per 72,051 conversions). Initiated by bringing both the $\overline{INTRLV}$ input and $\overline{CS}$ low (or hard-wiring $\overline{INTRLV}$ low), interleave extends the S5016's effective conversion time by 20 master clock cycles (5 µs @ 4 MHz). Other than reduced throughput, interleave is totally transparent to the user.

Burst calibrations initiated at CAL pick up where interleave left off, so calibration cycles can be hastened by "bursting" a number of experiments whenever the S5016 sees free time. Interleave is subordinate to burst calibrations, so $\overline{INTRLV}$ could still be externally tied low. If used, interleave should be left active continuously.

The fact that the S5016 offers several calibration modes is not to imply that the device needs to be recalibrated often. The device is very stable in the presence of large temperature changes. Tests have indicated that after using a single reset calibration at 25 °C most devices exhibit very little change in offset or gain when exposed to temperatures from -55 to +125 °C. The data indicated 30 ppm as the typical worst case total change in offset or gain over this temperature range. Differential linearity remained virtually unchanged. System error sources outside of the A/D converter, whether due to changes in temperature or to long-term aging, will generally dominate total system error.

Microprocessor Interface

The S5016 features an intelligent microprocessor interface which offers detailed status information and allows software control of the self-calibration functions. Output data is available in either 8-bit or 16-bit formats for easy interfacing to industry-standard microprocessors.

Strobing both $\overline{CS}$ and $\overline{RD}$ low enables the S5016's 3-state output buffers with either output data or status information depending on the status of A0. An address bit can be connected to A0 as shown in Figure 4b thereby memory mapping the status register and output data. Conversion status can be polled in software by reading the status register ($\overline{CS}$ and $\overline{RD}$ strobed low with A0 low), and masking status bits S0-S5 and S7 (by logically AND'ing the status word with 01000000) to determine the value of S6. Similarly, the software routine can determine calibration status using other status bits (see Table 2). *Care must be taken not to read the status register (A0 low) while HOLD is low, or a software reset will result* (see *Reset* above).

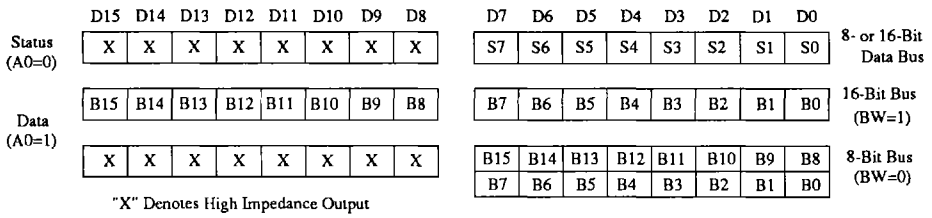


Figure 7. Data Format

Alternatively, the End-of-Convert ($\overline{EOC}$) output can be used to generate an interrupt or drive a DMA controller to dump the output directly into memory after each conversion. The $\overline{EOC}$ pin falls as each conversion cycle is completed and data is valid at the output. It returns high within four master clock cycles of the first subsequent data read operation or after the start of a new conversion cycle.

To interface with a 16-bit data bus, the BW input to the S5016 should be held high and all 16 data bits read in parallel on pins D0-D15. With an 8-bit bus, the converter's 16-bit result must be read in two portions. In this instance, BW should be held low and the 8 MSB's obtained on the first read cycle following a conversion. The second read cycle will yield the 8 LSB's. Both bytes appear on pins D0-D7. The upper/lower bytes of the same data will continue to toggle on subsequent reads until the next conversion finishes. Status bit S2 indicates which byte will appear on the next data read operation.

The S5016 internally buffers its output data, so data can be read while the device is tracking or converting the next sample. Therefore, retrieving the converter's digital output requires no reduction in ADC throughput. Enabling the 3-state outputs while the S5016 is converting will not introduce conversion errors. Connecting CMOS logic to the digital outputs is recommended. Suitable logic families include 4000B, 74HC, 74AC, 74ACT, and 74HCT.

Microprocessor Independent Operation

The S5016 can be operated in a stand-alone mode independent of intelligent control. In this mode, $\overline{CS}$ and $\overline{RD}$ are hard-wired low. This permanently enables the 3-state output buffers and allows transparent latch inputs (CAL and $\overline{INTRLV}$) to be active. A free-running condition is established when BW

PIN	STATUS BIT	STATUS	DEFINITION
D0	S0	$\overline{END\ OF\ CONVERSION}$	Falls upon completion of a conversion, and returns high on the first subsequent read.
D1	S1	RESERVED	Reserved for factory use.
D2	S2	LOW BYTE/$\overline{HIGH\ BYTE}$	When data is to be read in an 8-bit format (BW=0), indicates which byte will appear at the output next.
D3	S3	$\overline{END\ OF\ TRACK}$	When low, indicates the input has been acquired to the devices specified accuracy.
D4	S4	RESERVED	Reserved for factory use.
D5	S5	TRACKING	High when the device is tracking the input.
D6	S6	CONVERTING	High when the device is converting the held input.
D7	S7	CALIBRATING	High when the device is calibrating.

Table 2. Status Pin Definitions

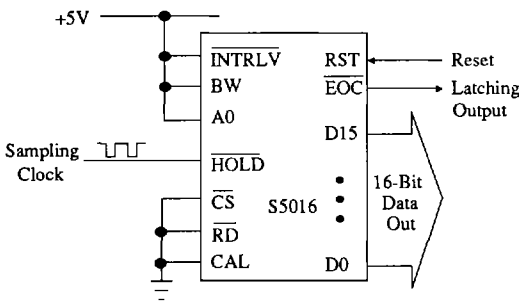


Figure 8. Microprocessor-Independent

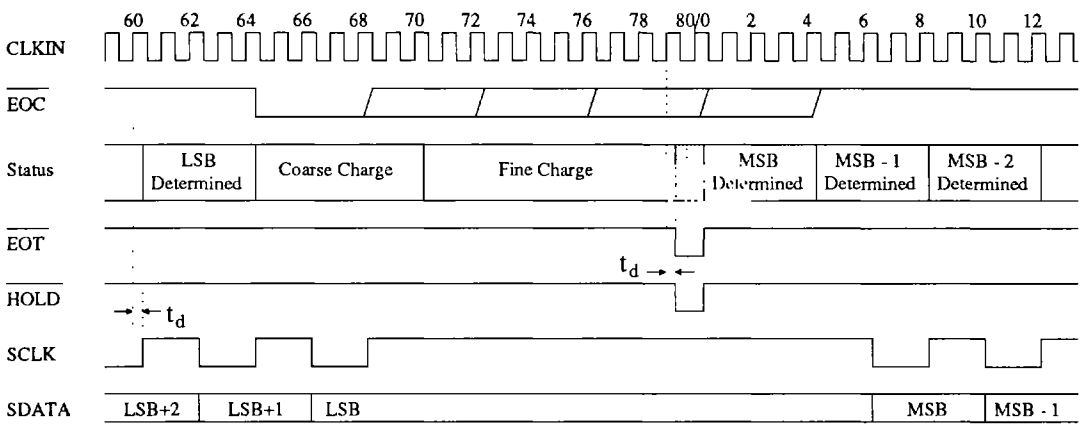
is tied high, CAL is tied low, and $\overline{HOLD}$ is continually strobed low or tied to $\overline{EOT}$. The S5016's $\overline{EOC}$ output can be used to externally latch the output data if desired. With $\overline{CS}$ and $\overline{RD}$ hard-wired low, $\overline{EOC}$ will strobe low for four master clock cycles after each conversion. Data will be unstable up to 100 ns after $\overline{EOC}$ falls, so it should be latched on the rising edge of $\overline{EOC}$.

Serial Output

All successive-approximation A/D converters derive their digital output serially starting with the MSB. The S5016 presents each bit to the SDATA pin four master clock cycles after it is derived and can be latched using the serial clock output, SCLK. Just subsequent to each bit decision SCLK will fall and return high once the bit information on SDATA has stabilized. Thus, the rising edge of the SCLK output should be used to clock the data from the S5016 (See Figure 9).

Analog Circuit Connections

Most popular successive-approximation A/D converters generate dynamic loads at their analog connections. The S5016 internally buffers all analog inputs (AIN, VREF, and AGND) to ease the demands placed on external circuitry. However, accurate system operation still requires careful attention to details at the design stage regarding source impedances as well as grounding and decoupling schemes.



Notes:
1. Synchronous (loopback) mode is illustrated. After $\overline{EOC}$ falls the converter goes into coarse charge mode for 6 CLKIN cycles, then to fine charge mode for 9 cycles, then $\overline{EOT}$ falls. In loopback mode, $\overline{EOT}$ trips $\overline{HOLD}$ which captures the analog sample. Conversion begins on the next rising edge of CLKIN. If operated asynchronously, $\overline{EOT}$ will remain low until after $\overline{HOLD}$ is taken low. When $\overline{HOLD}$ occurs the analog sample is captured immediately, but conversion may not begin until four CLKIN cycles later.
2. Timing delay td (relative to CLKIN) can vary between 135 ns to 235 ns over the military temperature range and over ± 10% supply variation
3. $\overline{EOC}$ returns high in 4 CLKIN cycles if A0 = 1 and $\overline{CS}$ = $\overline{RD}$ = 0 (Microprocessor Independent Mode); within 4 CLKIN cycles after a data read (Microprocessor Mode), or 4 CLKIN cycles after $\overline{HOLD}$ = 0 is recognized on a rising edge of CLKIN/4.

Figure 9. Serial Output Timing

A/D Converters

Reference Considerations

An application note titled "*Voltage References for the S501X Series of A/D Converters*" is available for the S5016. In addition to working through a reference circuit design example, it offers several built-and-tested reference circuits.

During conversion, each capacitor of the calibrated capacitor array is switched between VREF and AGND in a manner determined by the successive-approximation algorithm. The charging and discharging of the array results in a current load at the reference. The S5016 includes an internal buffer amplifier to minimize the external reference circuit's drive requirement and preserve the reference's integrity. Whenever the array is switched during conversion, the buffer is used to pre-charge the array thereby providing the bulk of the necessary charge. The appropriate array capacitors are then switched to the unbuffered VREF pin to avoid any errors due to offsets and/or noise in the buffer.

The external reference circuitry need only provide the residual charge required to fully charge the array after pre-charging from the buffer. This creates an ac current load as the S5016 sequences through conversions. The reference circuitry must have a low enough output impedance to drive the requisite current without changing its output voltage significantly. As the analog input signal varies, the switching sequence of the internal capacitor array changes. The current load on the external reference circuitry thus varies in response with the analog input. Therefore, the external reference must not exhibit significant peaking in its output impedance characteristic at signal frequencies or their harmonics.

A large capacitor connected between VREF and AGND can provide sufficiently low output impedance at the high end of the frequency spectrum, while almost all precision references exhibit extremely low output impedance at dc.

The magnitude of the current load on the external reference circuitry will scale to the master clock frequency. At full speed (4 MHz clock), the reference must supply a maximum load current of 10 µA peak-to-peak (1 µA typical). An output impedance of 2 Ω will therefore yield a maximum error of 20 µV. With a 4.5V reference and LSB size of 69 µV, this would insure approximately 1/4 LSB accuracy. A 10 µF capacitor exhibits an impedance of less than 2 Ω at frequencies greater than 16 kHz. A high-quality tantalum capacitor in parallel with a smaller ceramic capacitor is recommended.

Peaking in the reference's output impedance can occur because of capacitive loading at its output. Any peaking that might occur can be reduced by placing a small resistor in series with the capacitors (Figure 10). The equation in Figure 10 can be used to help calculate the optimum value of R for a particular reference. The term "f_{peak}" is the frequency of the peak in the output impedance of the reference before the resistor is added.

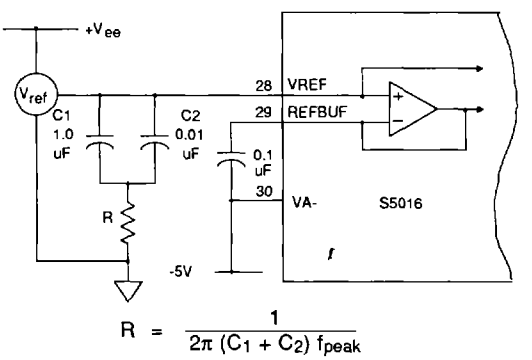


Figure 10. Reference Connections

The S5016 can operate with a wide range of reference voltages, but signal-to-noise performance is maximized by using as wide a signal range as possible. The recommended reference voltage is 4.5 volts. The S5016 can actually accept reference voltages up to the positive analog supply. However, the buffer's offset may increase as the reference voltage approaches VA+ thereby increasing external drive requirements at VREF. A 4.5V reference is the maximum reference voltage recommended. This allows 0.5V headroom for the internal reference buffer. Also, the buffer enlists the aid of an external 0.1 µF ceramic capacitor which must be tied be-

tween its output, REFBUF, and the negative analog supply, VA-. For more information on references, consult "Application Note: *Voltage References for the S501X Series of A/D Converters*".

Analog Input Connection

The analog input terminal functions similarly to the VREF input after each conversion when switching into the track mode. During the first six master clock cycles in the track mode, the buffered version of the analog input is used for pre-charging the capacitor array. An additional period is required for fine-charging directly from AIN to obtain the specified accuracy. Figure 11 exemplifies this operation. During pre-charge the charge on the capacitor array first settles to the buffered version of the analog input. This voltage is offset from the actual input voltage. During fine-charge, the charge then settles to the accurate unbuffered version.

The acquisition time of the S5016 depends on the master clock frequency. This is due to a fixed pre-charge period. For instance, operating the -16 version with an external 4 MHz master clock results in a 3.75 µs acquisition time: 1.5 µs for pre-charging (6 clock cycles) and 2.25 µs for fine-charging. Fine-charge settling is specified as a maximum of 2.25 µs for an analog source impedance of less than 200 Ω. In addition, the comparator requires a source impedance of less than 400 Ω around 2 MHz for stability, which is met by practically all bipolar op amps. Large dc source impedances can be accommodated by adding capacitance from AIN to ground (typically 200 pF) to decrease source impedance at high frequencies. However, high dc source resistances will increase the input's RC time constant and extend the necessary acquisition time. For more information on input applications, consult the application note: *Input Buffer Amplifiers for the S501X Family of A/D Converters.*

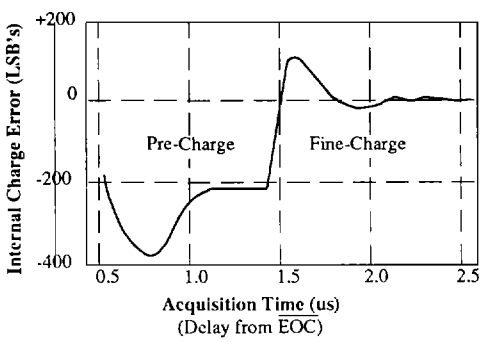


Figure 11. Internal Acquisition Time

During the first six clock cycles following a conversion (pre-charge), the S5016 is capable of slewing at 5 V/µs in unipolar mode. In bipolar mode, only half the capacitor array is connected to the analog input so the S5016 can slew at 10 V/µs. After the first six master clock cycles, it will slew at 0.25 V/µs in the unipolar mode and 0.5 V/µs in bipolar mode. Acquisition of fast slewing signals (step functions) can be hastened if the step occurs during or immediately following the conversion cycle. For instance, channel selection in multiplexed applications should occur while the S5016 is converting (see Figure 12). Multiplexer settling is thereby removed from the overall throughput equation, and the S5016 can convert at full speed.

Analog Input Range/Coding Format

The reference voltage directly defines the input voltage range in both the unipolar and bipolar configurations. In the unipolar configuration (BP/$\overline{UP}$ low), the first code transition occurs 0.5 LSB above AGND, and the final code transition occurs 1.5 LSB's below VREF. Coding is in straight binary format. In the bipolar configuration (BP/$\overline{UP}$ high), the first code transition occurs 0.5 LSB above -VREF and the last transition occurs 1.5 LSB's below +VREF. Coding is in an offset-binary format. Positive full scale gives a digital output of 1111111111111111, and negative full scale gives a digital output of 0000000000000000.

The BP/$\overline{UP}$ mode pin may be switched after calibration without having to recalibrate the converter. However, the BP/$\overline{UP}$ mode should be changed during the previous conversion cycle, that is, between $\overline{HOLD}$ falling and $\overline{EOC}$ falling. If BP/$\overline{UP}$ is changed at any other time, one dummy conversion cycle must be allowed for proper acquisition of the input.

Grounding and Power Supply Decoupling

The S5016 uses the analog ground connection, AGND, only as a reference voltage. No dc power currents flow through the AGND connection, and it is completely independent of DGND. However, any noise riding on the AGND input relative to the system's analog ground will induce conversion errors. Therefore, both the analog input and reference voltage should be referred to the AGND pin, which should be used as the entire system's analog ground reference point.

The digital and analog supplies are isolated within the S5016 and are pinned out separately to minimize coupling between the analog and digital sections of the chip. All four supplies should be decoupled to their respective grounds using 0.1 µF ceramic capacitors. If significant low-frequency noise is present on the supplies, 1 µF tantalum capacitors are recommended in parallel with the 0.1 µF capacitors.

The positive digital power supply of the S5016 must never exceed the positive analog supply by more than a diode drop or the S5016 could experience permanent damage. If the two supplies are derived from separate sources, care must be taken that the analog supply comes up first at power-up. The system connection diagram in Figure 23 shows a decoupling scheme which allows the S5016 to be powered from a single set of ± 5V rails.

As with any high-precision A/D converter, the S5016 requires careful attention to grounding and layout arrangements. However, no unique layout issues must be addressed to properly apply the S5016. The DB5016 evaluation board is available for the S5016, which avoids the need to design, build, and debug a high-precision PC board to initially characterize the part. The board comes with a socketed S5016, and can be quickly reconfigured to simulate any combination of sampling, calibration, master clock, and analog input range conditions.

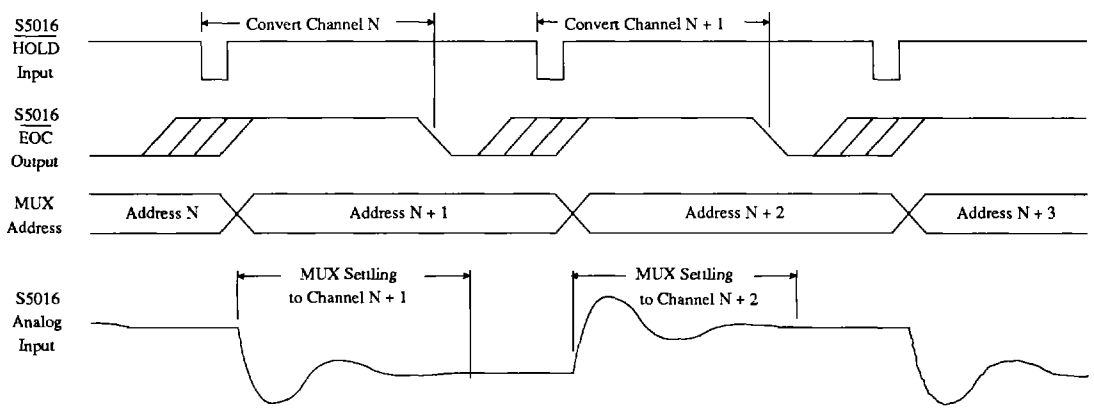


Figure 12. Pipelined MUX Input Channels

S5016 Performance

Differential Nonlinearity

One source of nonlinearity in A/D converters is bit weight errors. These errors arise from the deviation of bits from their ideal binary-weighted ratios, and lead to nonideal widths for each code. If DNL errors are large, and code widths shrink to zero, it is possible for one or more codes to be entirely missing. The S5016 calibrates all bits in the capacitor array to within ± 1/4 LSB resulting in nearly ideal DNL. A histogram plot of typical DNL can be seen in Figure 13.

A histogram test is a statistical method of deriving an A/D converter's differential nonlinearity. A ramp is input to the A/D and a large number of samples are taken to insure a high confidence level in the test's result. The number of occurrences for each code is monitored and stored. A perfect A/D converter would have all codes of equal size and therefore equal numbers of occurrences. In the histogram test a code with the average number of occurrences will be considered ideal (DNL = 0). A code with more or less occurrences than average will appear as a DNL of greater or less than zero LSB. A missing code has zero occurrences, and will appear as a DNL of -1 LSB.

Integral Nonlinearity

Integral Nonlinearity (INL; also termed Relative Accuracy or just Nonlinearity) is defined as the deviation of the transfer function from an ideal straight line. Bows in the transfer curve generate harmonic distortion. The worst-case condition of bit-weight errors (DNL) has traditionally also defined the point of maximum INL.

Bit-weight errors have a drastic effect on a converter's ac performance. They can be analyzed as step functions superimposed on the input signal. Since bits (and their errors) switch in and out throughout the transfer curve, their effect is signal dependent. That is, harmonic and intermodulation distortion, as well as noise, can vary with different input conditions. Designing a system around characterization data is risky since transfer curves can differ drastically unit-to-unit and lot-to-lot.

The S5016 achieves repeatable signal-to-noise and harmonic distortion performance using an on-chip self-calibration scheme. The S5016 calibrates its bit weights to within ± 1/4 LSB at 16-bits (± 0.0004% FS) yielding peak distortion as low as -105 dB (see Figure 14). Unlike traditional ADC's, the linearity of the S5016 is not limited by bit-weight errors; its performance is therefore extremely repeatable and independent of input signal conditions.

FFT Tests and Windowing

In the factory, the S5016 is tested using Fast Fourier Transform (FFT) techniques to analyze the converter's dynamic performance. A pure sinewave is applied to the S5016, and a "time record" of 1024 samples is captured and processed. The FFT algorithm analyzes the spectral content of the digital waveform and distributes its energy among 512 "frequency bins." Assuming an ideal sinewave, distribution of energy in bins outside of the fundamental and dc can only be due to quantization effects and errors in the S5016.

If sampling is not synchronized to the input sinewave, it is highly unlikely that the time record will contain an

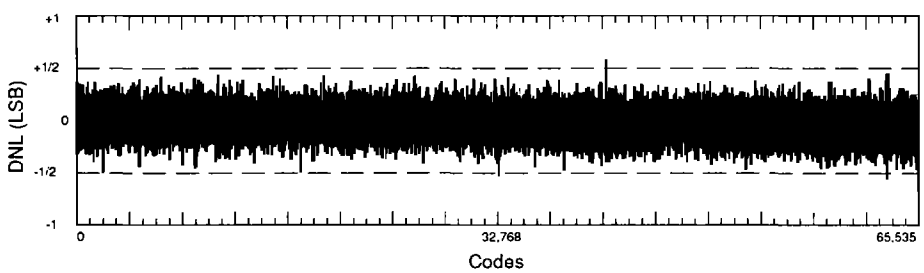


Figure 13. CS5016 Differential Nonlinearity Plot

integer number of periods of the input signal. However, the FFT assumes that the signal is periodic, and will calculate the spectrum of a signal that appears to have large discontinuities, thereby yielding a severely distorted spectrum. To avoid this problem, the time record is multiplied by a window function prior to performing the FFT. The window function smoothly forces the endpoints of the time record to zero, thereby removing the discontinuities. The effect of the window in the frequency-domain is to convolute the spectrum of the window with that of the actual input.

The quality of the window used for harmonic analysis is typically judged by its highest side-lobe level. The Blackman-Harris window used for testing the S5016 has a maximum side-lobe level of -92 dB. Figure 14 shows an FFT computed from an ideal 16-bit sinewave multiplied by a Blackman-Harris window. Artifacts of windowing are discarded from the signal-to-noise calculation using the assumption that quantization noise is white. All FFT plots in this data sheet were derived by averaging the FFT results from ten time records. This filters the spectral variability that can arise from capturing finite time records without disturbing the total energy outside the fundamental. All harmonics and the -92 dB side-lobes from the Blackman-Harris window are therefore clearly visible in the plots. For more information on FFT's and windowing refer to: F.J. HARRIS, "On the use of windows for harmonic analysis with the Discrete Fourier Transform", Proc. IEEE, Vol. 66, No. 1, Jan 1978, pp.51-83. This is available on request from Gould AMI.

Quantization Noise

The error due to quantization of the analog input ultimately dictates the accuracy of any A/D converter. The continuous analog input must be represented by one of a finite number of digital codes, so the best accuracy to which an analog input can be known from its digital code is ± 1/2 LSB. Under circumstances commonly encountered in signal processing applications, this quantization error can be treated as a random variable. The magnitude of the error is limited to ± 1/2 LSB, but any value within this range has equal probability of occurance. Such a probability distribution leads to an error "signal" with an rms value of 1 LSB/$\sqrt{12}$. Using an rms signal value of FS/$\sqrt{8}$ (amplitude = FS/2), this relates to an ideal 16-bit signal-to-noise ratio of 97.7 dB.

Equally important is the spectral content of this error signal. It can be shown to be approximately white, with its energy spread uniformly over the band from dc to one-half the sampling rate. Advantage of this characteristic can be made by judicious use of filtering. If the signal is bandlimited, much of the quantization error can be filtered out, and improved system performance can be attained.

As illustrated in Figures 16 and 17, the S5016's on-chip self-calibration provides very accurate bit weights which yield no degradation in quantization noise with low-level input signals. In fact, quantization noise remains below the noise floor in the S5016 which dictates the converter's signal-to-noise performance.

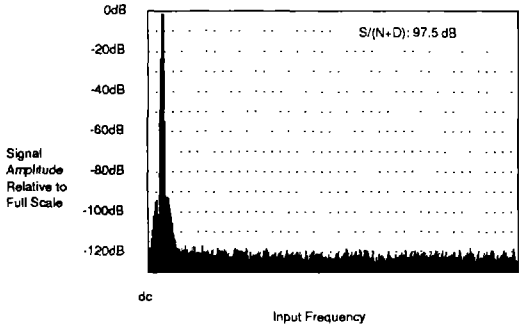


Figure 14. FFT Plot of Ideal 16-bit Signal

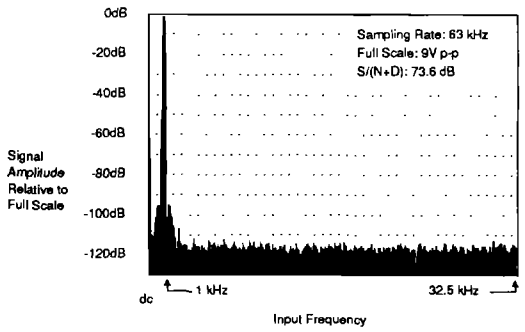


Figure 15. FFT Plot with 1 kHz Full-Scale Input

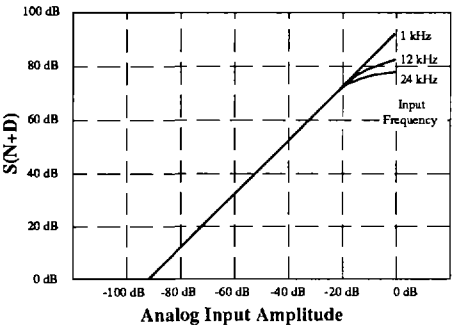


Figure 16. S/(N+D) vs. Input Amplitude (9V p-p Full-Scale Input)

Noise

All analog circuitry in the S5016 is wideband in order to achieve fast conversions and high throughput. Wideband noise in the S5016 integrates to 35 mV rms in unipolar mode (70 µV rms in bipolar mode). This is approximately 1/2 LSB rms with a 4.5V reference in both modes. Figure 18 shows a histogram plot of output code occurrences obtained from 5000 samples taken from a S5016 in the bipolar mode. Hexadecimal code 80CD was arbitrarily selected and the analog input was set close to code center. With a noiseless converter, code 80CD would always appear. The histogram plot of the S5016 has a "bell" shape with all codes other than 80CD due to internal noise.

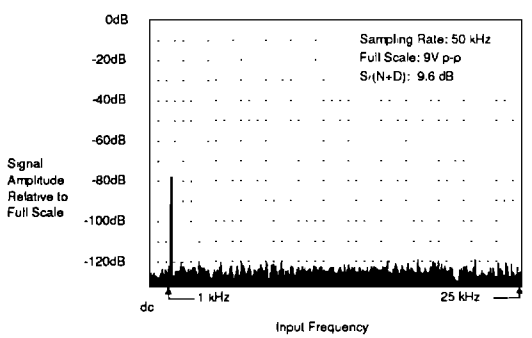


Figure 17. FFT Plot with 1 kHz -80 dB Input

In a sampled data system all information about the analog input applied to the sample/hold appears in the baseband from dc to one-half the sampling rate. This includes high-frequency components which alias into the baseband. Low-pass (anti-alias) filters are therefore used to remove frequency components in the input signal which are above one-half the sample rate. However, all wideband noise introduced by the S5016 still aliases into the baseband. This "white" noise is evenly spread from dc to one-half the sampling rate and integrates to 35 µV rms in unipolar mode.

Noise can be reduced by sampling at higher than the desired word rate and averaging multiple samples for each word. Oversampling spreads the S5016's noise over a wider band (for lower noise density), and averaging applies a low-pass response which filters noise above the desired signal bandwidth. In general, the S5016's noise performance can be maximized in any application by always sampling at the maximum specified rate of 50 kHz (for lowest noise density) and digitally filtering to the desired signal bandwidth.

Sampling Distortion

The ultimate limitation on the S5016's linearity (and distortion) arises from nonideal sampling of the analog input voltage. The calibrated capacitor array used during conversions is also used to track and hold the analog input signal. The conversion is not performed on the analog input voltage per se, but is actually performed on the charge trapped on the capacitor array at the moment the HOLD command is given. The charge on the array is ideally related to the analog input voltage by $Q_{in} = -V_{in} \times C_{tot}$ as shown in Figure 2. Any deviation from this ideal relationship will result in conversion errors even if the conversion process proceeds flawlessly.

At dc, the DAC capacitor array's voltage coefficient dictates the converter's linearity. This variation in capacitance with respect to applied signal voltage yields a nonlinear relationship between charge Q_{in} and the analog input voltage V_{in} and places a bow or wave in the transfer function. This is the dominant source of distortion at low input frequencies (Figure 15).

A/D Converters

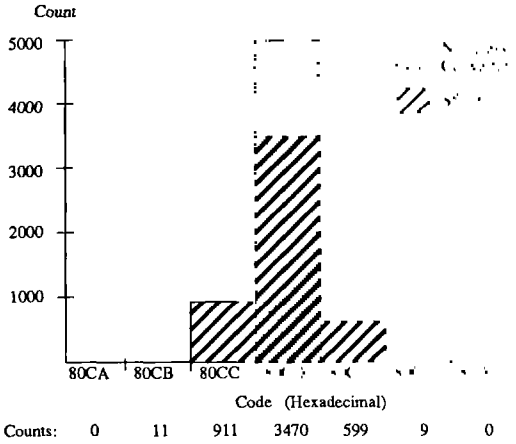


Figure 18. Histogram Plot of 5000 Conversion Inputs

The ideal relationship between Q_{in} and V_{in} can also be distorted at high signal frequencies due to nonlinearities in the internal MOS switches. Dynamic signals cause ac current to flow through the switches connecting the capacitor array to the analog input pin in the track mode. Nonlinear on-resistance in the switches causes a nonlinear voltage drop. This effect worsens with increased signal frequency as shown in Figure 16 since the magnitude of the steady state current increases. First noticeable at 1 kHz, this distortion assumes a linear relationship with input frequency. With signals 20 dB or more below full-scale, it no longer dominates the converter's overall S/(N+D) performance (Figures 19 and 20).

This distortion is strictly an ac sampling phenomenon. If significant energy exists at high frequencies, the effect can be eliminated using an external track-and-hold amplifier to allow the array's charge current to decay, thereby eliminating any voltage drop across the switches. Since the S5016 has a second sampling function on-chip, the external track-and-hold can return to the track mode once the converter's HOLD input falls. It need only acquire the analog input by the time the entire conversion cycle finishes.

Clock Feedthrough

Maintaining the integrity of analog signals in the presence of digital switching noise is a difficult problem. The S5016 can be synchronized to the digital system using the CLKIN input to avoid conversion errors due to asynchronous interference. However, digital interference will still affect sampling purity due to coupling between the S5016's analog input and master clock.

The effect of clock feedthrough depends on the sampling conditions. If the sampling signal at the HOLD input is synchronized to the master clock, clock feedthrough will appear as a dc offset at the S5016's output. The offset could theoretically reach the peak coupling magnitude (Figure 21), but the probability of

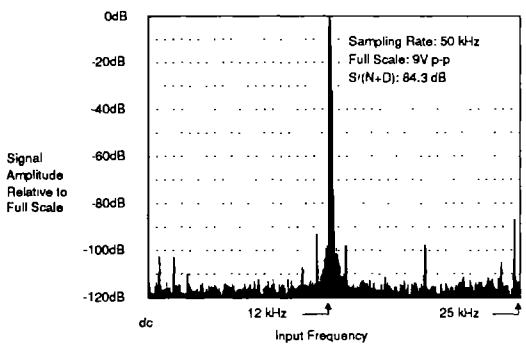


Figure 19. FFT Plot with 12 kHz Full-Scale Input

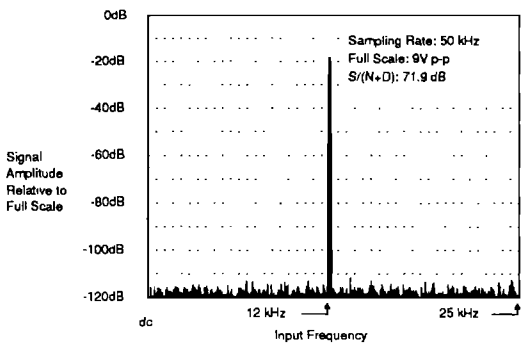


Figure 20. FFT Plot with 12 kHz -20 dB Input

Master Clock		Analog Input	Clock Feedthrough	
Int/Ext	Freq	Source Impedance	RMS	Peak-to-Peak
Internal	2MHz	50 Ω	15uV	70uV
External	2MHz	50 Ω	25uV	110uV
External	4MHz	50 Ω	40uV	150uV
External	4MHz	25 Ω	25uV	110uV
External	4MHz	200 Ω	80uV	325uV

Figure 21. Examples of Measured Clock

this occurring is small since the peaks are spikes of short duration.

If sampling is performed asynchronously with the master clock, clock feedthrough will appear as an ac error at the S5016's output. With a fixed sampling rate, a tone will appear as the clock frequency aliases into the baseband. The tone frequency can be calculated using the equation below and could be selectively filtered in software using DSP techniques.

$$f_{tone} = (N\ f_s - f_{clk})$$

where $N = f_{clk}/f_s$ rounded to the nearest integer

The magnitude of clock feedthrough depends on the master clock conditions and the source impedance applied to the analog input. When operating with the S5016's internally generated clock, the CLKIN input is grounded and the dominant source of coupling is through the device's substrate. As shown in Figure 21, a typical S5016 operating with its internal oscillator at 2 MHz and 50 Ω of analog input source impedance will exhibit only 15 μV rms of clock feedthrough. However, if a 2 MHz external clock is applied to CLKIN under the same conditions, feedthrough increases to 25 μV rms. Feedthrough also increases with clock frequency; a 4 MHz clock yields 40 μV rms.

Clock feedthrough can be reduced by limiting the source impedance applied at the analog input. As shown in Figure 21, reducing source impedance from 50 Ω to 25 Ω yields a 15 μV rms reduction in feedthrough. Therefore, when operating the S5016 with high-frequency external master clocks, it is important to minimize source impedance applied to the S5016's input.

Also, the overall effect of clock feedthrough can be minimized by maximizing the input range and LSB size. The reference voltage applied to VREF can be maximized, and the S5016 can be operated in bipolar mode which inherently doubles the LSB size over the unipolar mode.

Power Supply Rejection

The S5016's power supply rejection performance is enhanced by the on-chip self-calibration and an "auto-zero" process. Drifts in power supply voltages at frequencies less than the calibration rate have negligible effect on the S5016's accuracy. This, of course, is because the S5016 adjusts its offset to within a small fraction of an LSB during calibration. Above the calibration frequency the excellent power supply rejection of the internal amplifiers is augmented by an auto-zero process. Any offsets are stored on the capacitor array and are effectively subtracted once conversion is initiated. Figure 22 shows power supply rejection of the S5016 in the bipolar mode with the analog input grounded and a 300 mV p-p ripple applied to each supply. Power supply rejection improves by 6 dB in the unipolar mode.

Notches of increased rejection arise from the auto-zeroing at the conversion rate. The frequencies at which these notches occur also depend on the value of the captured analog input. The line shows worst-case rejection for all combinations of conversion rates and input conditions in the bipolar mode.

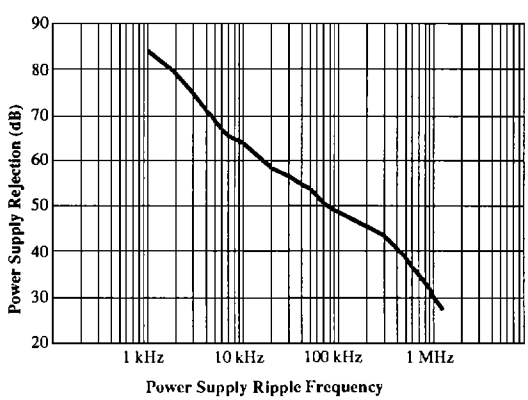


Figure 22. Power Supply Rejection

$\overline{HOLD}$	$\overline{CS}$	CAL	$\overline{INTRLV}$	$\overline{RD}$	A0	RST	Function
↓	X	X	X	X	*	0	Hold and Start Convert
X	0	1	X	X	*	0	Initiate Burst Calibration
1	0	0	X	X	*	0	Stop Burst Cal and Begin Track
X	0	X	0	X	*	0	Initiate Interleave Calibration
X	0	X	1	X	*	0	Terminate Interleave Cal
X	0	X	X	0	1	0	Read Output Data
1	0	X	X	0	0	0	Read Status Register
X	1	X	X	X	*	X	High Impedance Data Bus
X	X	X	X	1	*	X	High Impedance Data Bus
X	X	X	X	X	X	1	Reset
0	0	X	X	X	0	X	Reset

* The status of A0 is not critical to the operation specified. However, A0 should not be low with $\overline{CS}$ and $\overline{HOLD}$ low, or a software reset will result.

Table 3. S5016 Truth Table

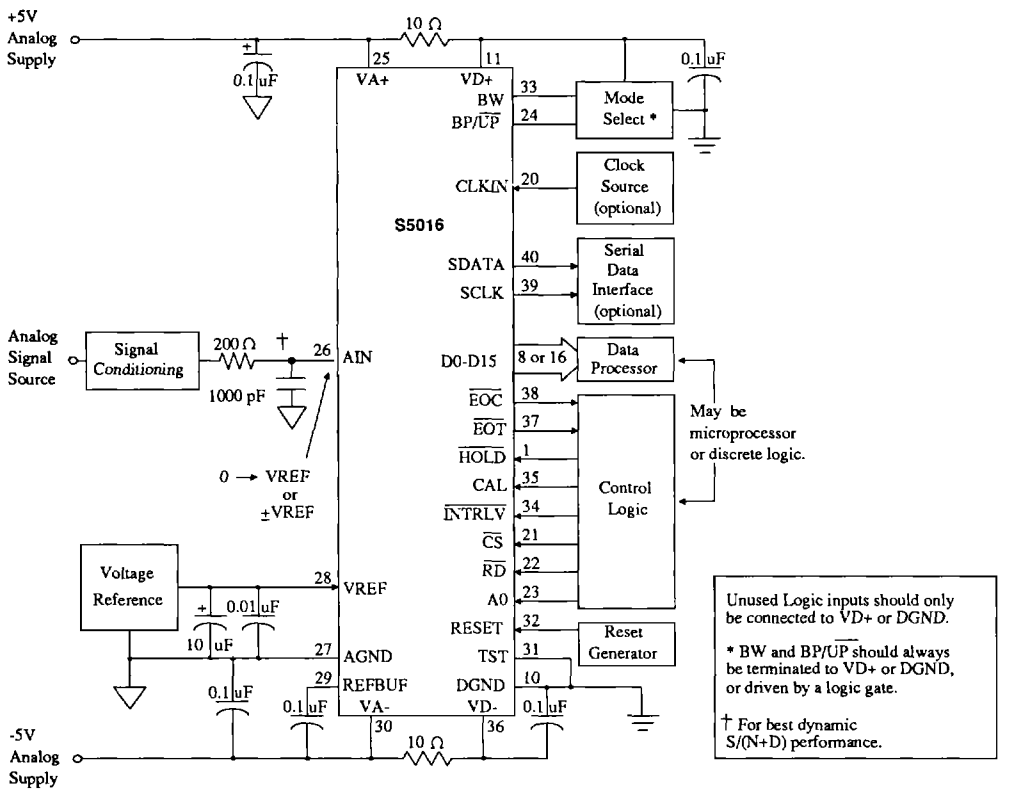
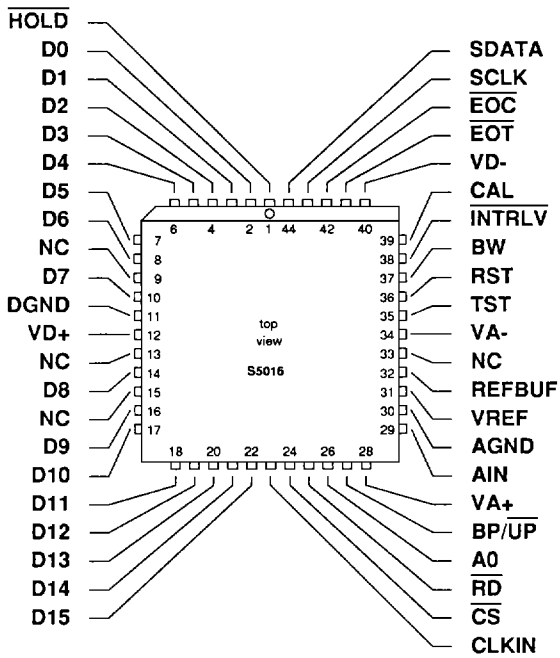


Figure 23. S5016 System Connection Diagram

HOLD	HOLD	1	40	SDATA	SERIAL OUTPUT
(LSB) DATA BUS BIT 0	D0	2	39	SCLK	SERIAL CLOCK
DATA BUS BIT 1	D1	3	38	EOC	END OF CONVERSION
DATA BUS BIT 2	D2	4	37	EOT	END OF TRACK
DATA BUS BIT 3	D3	5	36	VD-	NEGATIVE DIGITAL POWER
DATA BUS BIT 4	D4	6	35	CAL	CALIBRATE
DATA BUS BIT 5	D5	7	34	INTRLV	INTERLEAVE
DATA BUS BIT 6	D6	8	33	BW	BUS WIDTH SELECT
DATA BUS BIT 7	D7	9	32	RST	RESET
DIGITAL GROUND	DGND	10	31	TST	TEST
POSITIVE DIGITAL POWER	VD+	11	30	VA-	NEGATIVE DIGITAL POWER
DATA BUS BIT 8	D8	12	29	REFBUF	REFERENCE BUFFER OUTPUT
DATA BUS BIT 9	D9	13	28	VREF	VOLTAGE REFERENCE
DATA BUS BIT 10	D10	14	27	AGND	ANALOG GROUND
DATA BUS BIT 11	D11	15	26	AIN	ANALOG INPUT
DATA BUS BIT 12	D12	16	25	VA+	POSITIVE ANALOG POWER
DATA BUS BIT 13	D13	17	24	BP/UP	BIPOLAR/UNIPOLAR SELECT
DATA BUS BIT 14	D14	18	23	A0	READ ADDRESS
(MSB) DATA BUS BIT 15	D15	19	22	RD	READ
CLOCK INPUT	CLKIN	20	21	CS	CHIP SELECT



NOTE: All pin references in this data sheet refer to the 40-pin DIP package numbering. Use this figure to determine pin numbers for 44-pin package

Pin Descriptions

Power Supply Connections

VD+ – Positive Digital Power, PIN 11.
Positive digital power supply. Nominally +5 volts.

VD- – Negative Digital Power, PIN 36.
Negative digital power supply. Nominally -5 volts.

DGND – Digital Ground, PIN 10.
Digital ground.

VA+ – Positive Analog Power, PIN 25.
Positive analog power supply. Nominally +5 volts.

VA- – Negative Analog Power, PIN 30.
Negative analog power supply. Nominally -5 volts.

AGND – Analog Ground, PIN 27.
Analog ground.

Oscillator

CLKIN – Clock Input, PIN 20.
All conversions and calibrations are timed from a master clock which can either be supplied by driving this pin with an external clock signal, or can be internally generated by tying this pin to DGND.

Digital Inputs

$\overline{\text{HOLD}}$ – Hold, PIN 1.
A falling transition on this pin sets the S5016 to the hold state and initiates a conversion. This input must remain low at least one master clock cycle plus 50 ns.

$\overline{\text{CS}}$ – Chip Select, PIN 21.
When high, the data bus outputs are held in a high impedance state and the input to CAL and $\overline{\text{INTRLV}}$ are ignored. A falling transition initiates or terminates burst or interleave calibration (depending on the status of CAL and INTRLV) and a rising transition latches both the CAL and INTRLV inputs. If $\overline{\text{RD}}$ is low, the data bus is driven as indicated by BW and A0.

$\overline{\text{RD}}$ – Read, PIN 22.
When $\overline{\text{RD}}$ and $\overline{\text{CS}}$ are both low, data is driven onto the data bus. If either signal is high, the data bus outputs are held in a high impedance state. The data driven onto the bus is determined by BW and A0.

A0 – Read Address, PIN 23.
Determines whether data or status information is placed onto the data bus. When high during the read operation, converted data is placed onto the data bus; when low, the status register is driven onto the bus.

BP/$\overline{\text{UP}}$ – Bipolar/Unipolar Input Select, PIN 24.
When high, the device is configured with a bipolar transfer function ranging from -VREF to +VREF. Encoding is in an offset binary format, with the mid-scale code 100...0000 centered at AGND. When low, the device is configured for a unipolar transfer function from AGND to VREF. Unipolar encoding is in straight binary format. Once calibration has been performed, either bipolar or unipolar may be selected without the need to recalibrate.

RST – Reset, PIN 32.
When taken high for at least 100 ns, all internal digital logic is reset. Upon being taken low, a full calibration sequence is initiated.

BW – Bus Width Select, PIN 33.
When hard-wired high, all 16 data bits are driven onto the bus simultaneously during a data read cycle. When low, the bus is in a byte wide format. On the first read following a conversion, the eight MSB's are driven onto D0-D7. A second read cycle places the eight LSB's on D0-D7. Subsequent reads will toggle the higher/lower order byte. Regardless of BW's status, a read cycle with A0 low yields the status information on D0-D7.

$\overline{\text{INTRLV}}$ – Interleave, PIN 34.
When latched low using $\overline{\text{CS}}$, the device goes into interleave calibration mode. A full calibration will complete every 72,051 conversions. The effective conversion time extends by 20 clock cycles.

CAL – Calibrate, PIN 35. (See Addendum appending this data sheet))
When latched high using $\overline{\text{CS}}$, burst calibration results. The device cannot perform conversions during the calibration period which will terminate only once CAL is latched low again. Calibration picks up where the previous calibration left off, and calibration cycles complete every 1,441,020 master clock cycles. If the device is converting when a calibration is signaled, it will wait until that conversion completes before beginning.

Analog Inputs

AIN – Analog Input, PIN 26.
Input range in the unipolar mode is zero volts to VREF. Input range in bipolar mode is -VREF to +VREF. The output impedance of buffer driving this input should be less than or equal to 200 Ω.

VREF – Voltage Reference, PIN 28.
The analog reference voltage which sets the analog input range. It represents positive full scale for both bipolar and unipolar operation, and its magnitude sets negative full scale in bipolar mode.

Digital Outputs

D0 through D15 – Data Bus Outputs, PINS 2 thru 9, 12 thru 19.
3-state output pins. Enabled by $\overline{\text{CS}}$ and $\overline{\text{RD}}$, they offer the converter's 16-bit output in a format consistent with the state of BW if A0 is high. If A0 is low, bits D0-D7 offer status register.

$\overline{\text{EOT}}$ – End Of Track, PIN 37.
If low, indicates that enough time has elapsed since the last conversion for the device to acquire the analog input signal (3.75 µs for 4 MHz external clock).

$\overline{\text{EOC}}$ – End Of Conversion, PIN 38.
This output indicates the end of a conversion or calibration cycle. It is high during a conversion and will fall to a low state upon completion of the conversion cycle indicating valid data is available at the output. Returns high on the first subsequent read or the start of a new conversion cycle.

SDATA – Serial Output, PIN 40.
Presents each output data bit after it is determined by the successive approximation algorithm. Valid on the rising edge of SCLK, data appears MSB first, LSB last, and each bit remains valid until the next bit appears.

SCLK – Serial Clock Output, PIN 39.
Used to clock converted output data serially from the S5016. Serial data is stable on the rising edge of SCLK.

Analog Outputs

REFBUF – Reference Buffer Output, PIN 29.
Reference buffer output. A 0.1 µF ceramic capacitor must be tied between this pin and VA-.

Miscellaneous

TST – Test, PIN 31.
Allows access to the S5016's test functions which are reserved for factory use. Must be tied to DGND.

Parameter Definitions

Linearity Error
The deviation of a code from a straight line passing through the endpoints of the transfer function after zero- and full-scale errors have been accounted for. "Zero-scale" is a point 1/2 LSB below the first code transition and "full-scale" is a point 1/2 LSB beyond the code transition to all ones. The deviation is measured from the middle of each particular code. Units in % Full-Scale.

Differential Linearity
Minimum resolution for which no missing codes is guaranteed. Units in bits.

Full Scale Error
The deviation of the last code transition from the ideal (VREF-3/2 LSB's).
Units in LSB's.

Unipolar Offset
The deviation of the first code transition from the ideal (1/2 LSB above AGND) when in unipolar mode (BP/UP low). Units in LSB's.

Bipolar Offset
The deviation of the mid-scale transition (011...111 to 100...000) from the ideal (1/2 LSB below AGND) when in bipolar mode (BP/$\overline{UP}$ high). Units in LSB's.

Bipolar Negative Full-Scale Error
The deviation of the first code transition from the ideal when in bipolar mode (BP/$\overline{UP}$ high). The ideal is defined as lying on a straight line which passes through the final and mid-scale code transitions. Units in LSB's.

Peak Harmonic or Spurious Noise (More accurately, Signal to Peak Harmonic or Spurious Noise)
The ratio of the rms value of the signal to the rms value of the next largest spectral component below the Nyquist rate (excepting dc). This component is often an aliased harmonic when the signal frequency is a significant proportion of the sampling rate. Expressed in decibels.

Total Harmonic Distortion
The ratio of the rms sum of all harmonics to the rms value of the signal. Units in percent.

Signal-to-Noise Ratio
The ratio of the rms value of the signal to the rms sum of all other spectral components below the Nyquist rate (excepting dc), including distortion components. Expressed in decibels.

Aperture Time
The time required after the hold command for the sampling switch to open fully. Effectively a sampling delay which can be nulled by advancing the sampling signal. Units in nanoseconds.

Aperture Jitter
The range of variation in the aperture time. Effectively the "sampling window" which ultimately dictates the maximum input signal slew rate acceptable for a given accuracy. Units in picoseconds.

NOTE: Temperatures specified define ambient conditions in free-air during test and do not refer to the junction temperature of the device.

Ordering Guide

Model	Linearity	Signal to Noise Ratio	Conversion Time	Temp. Range	Package
S5016-JP32	.0030%	87 dB	32.50 µs	0 to 70 °C	40-Pin Plastic DIP
S5016-JP16	.0030%	87 dB	16.25 µs	0 to 70 °C	40-Pin Plastic DIP
S5016-KP32	.0015%	90 dB	32.50 µs	0 to 70 °C	40-Pin Plastic DIP
S5016-KP16	.0015%	90 dB	16.25 µs	0 to 70 °C	40-Pin Plastic DIP
S5016-JL32	.0030%	87 dB	32.50 µs	0 to 70 °C	44-Pin PLCC
S5016-JL16	.0030%	87 dB	16.25 µs	0 to 70 °C	44-Pin PLCC
S5016-KL32	.0015%	90 dB	32.50 µs	0 to 70 °C	44-Pin PLCC
S5016-KL16	.0015%	90 dB	16.25 µs	0 to 70 °C	44-Pin PLCC
S5016-AD32	.0030%	87 dB	32.50 µs	-40 to +85 °C	40-Pin CerDIP
S5016-AD16	.0030%	87 dB	16.25 µs	-40 to +85 °C	40-Pin CerDIP
S5016-BD32	.0015%	90 dB	32.50 µs	-40 to +85 °C	40-Pin CerDIP
S5016-BD16	.0015%	90 dB	16.25 µs	-40 to +85 °C	40-Pin CerDIP
S5016-AL32	.0030%	87 dB	32.50 µs	-40 to +85 °C	44-Pin PLCC
S5016-AL16	.0030%	87 dB	16.25 µs	-40 to +85 °C	44-Pin PLCC
S5016-BL32	.0015%	90 dB	32.50 µs	-40 to +85 °C	44-Pin PLCC
S5016-BL16	.0015%	90 dB	16.25 µs	-40 to +85 °C	44-Pin PLCC
S5016-SD16	.0076%	87 dB	16.25 µs	-55 to +125 °C	40-Pin CerDIP
S5016-TD16	.0015%	90 dB	16.25 µs	-55 to +125 °C	40-Pin CerDIP
S5016-SE16	.0076%	87 dB	16.25 µs	-55 to +125 °C	44-Pin Ceramic LCC
S5016-TE16	.0015%	90 dB	16.25 µs	-55 to +125 °C	44-Pin Ceramic LCC

Addendum

Burst Calibration

Burst calibration mode allows control of partial calibration cycles. Due to an unforeseen condition inside the part, asynchronous termination of calibration (CAL brought low) may result in a sub-optimal calibration result. It is recommended that burst calibration is not used, until the silicon is revised to prevent this effect.

Interleave calibration works perfectly, provided it is not used intermittently.

The reset calibration always works perfectly, and typically should be used instead of burst mode. The S5016's very low drift over temperature means that, under most circumstances, calibration need only be performed at power-up, using reset.

If you wish to use burst calibration, then please contact the factory for advice and new part availability information.