# TISP7015D

### TRIPLE ELEMENT THYRISTOR OVERVOLTAGE PROTECTORS

Copyright © 2001, Power Innovations Limited, UK

JULY 2000 - REVISED DECEMBER 2001

### THREE TERMINAL VERY LOW VOLTAGE PROTECTION

Ion-Implanted Breakdown Region - Precise and Stable Voltage

DEVICE	V <sub>DRM</sub>	V <sub>(BO)</sub>
DEVICE	v	v
'7015D	8	15

- Protection for signal, data and control lines - ISDN
  - T1/E1
  - RS232 & RS485
- Low Capacitance ......40 pF max.
- **Rated for International Surge Wave Shapes**

WAVE SHAPE	STANDARD	I <sub>PPSM</sub> A
8/20	IEC 61000-4-5	150
10/700	ITU-T K.20/45/21	40
10/1000	GR-1089-CORE	30



NC - No internal connection

#### device symbol



### description

The TISP7015D is a 3-point overvoltage protector designed for protecting against metallic (differential mode) and simultaneous longitudinal (common mode) impulses.

These devices are designed to limit overvoltages between signal, data and control port conductors, connected to terminals T1 and T2, and a protective ground, G. Each terminal pair has a symmetrical voltagetriggered bidirectional thyristor characteristic (Figure 1). Overvoltages are initially clipped by breakdown clamping until the voltage rises to the breakover level, which causes the device to crowbar into a low-voltage on state. This low-voltage on state causes the current resulting from the overvoltage to be safely diverted through the device. The device switches off when the diverted current falls below the holding current value.

Terminals marked NC do not have any internal connections and may be left floating or tied to some circuit point.

#### HOW TO ORDER

DEVICE	PACKAGE	CARRIER	ORDER #
TISP7015D	D, Small-outline	TAPE AND REEL	TISP7015DR
		TUBE	TISP7015D

#### INFORMATION PRODUCT

Information is current as of publication date. Products conform to specifications in accordance with the terms of Power Innovations standard warranty. Production processing does not necessarily include testing of all parameters.



# TRIPLE ELEMENT THYRISTOR OVERVOLTAGE PROTECTORS

JULY 2000 - REVISED DECEMBER 2001

## absolute maximum ratings, T<sub>A</sub> = 25 °C (unless otherwise noted)

RATING	SYMBOL	VALUE	UNIT
Repetitive peak off-state voltage	V <sub>DRM</sub>	± 8	V
Non-repetitive peak pulse current (see Notes 1 and 2)			
8/20 (IEC 61000-4-5, clause 7.2, R = 0, combination wave generator)		150	А
5/310 (ITU-T recommendation K.44, 10/700 generator used for K.20/45/21)	'PPSM	40	
10/1000 (Telcordia GR-1089-CORE, 10/1000 voltage wave shape)		30	
Non-repetitive peak on-state current (see Notes 1, 2 and 3)	1	4	٨
50/60 Hz, 1 s	'TSM	4	A
Junction temperature	ТJ	-40 to +150	°C
Storage temperature range	T <sub>sta</sub>	-65 to +150	°C

NOTES: 1. Initially the TISP7015D must be in thermal equilibrium at the specified T<sub>A</sub>. The surge may be repeated after the TISP7015D returns to its initial conditions.

2. These non-repetitive rated currents are peak values of either polarity.

3. Total return current,  $I_G$ , value.

# electrical characteristics for any terminal pair, $T_A = 25$ °C (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I <sub>DRM</sub>	Repetitive peak off-				+1	цΔ
	state current	$vD = \pm vDRM$			14	μΛ
V <sub>(BO)</sub>	Breakover voltage	dv/dt = $\pm 250$ V/ms, R <sub>SOURCE</sub> = 300 $\Omega$			±15	V
I <sub>(BO)</sub>	Breakover current	dv/dt = $\pm 250$ V/ms, R <sub>SOURCE</sub> = 300 $\Omega$			±100	mA
VT	On-state voltage	$I_T = \pm 5 \text{ A}, t_W = 100 \ \mu \text{s}$			±4	V
Ι <sub>Η</sub>	Holding current	$I_{T} = \pm 5 \text{ A}, \text{ di/dt} = \pm -30 \text{ mA/ms}$	±30			mA
ID	Off-state current	$V_{\rm D} = \pm 0.85 V_{\rm DRM}, T_{\rm A} = 85 \ ^{\circ}{\rm C}$			±10	μA
Coff	Off-state capacitance	$f = 1 \text{ MHz}$ , $V_d = 30 \text{ mV rms}$ , $V_D = 0$ , (see Note 4)		32	40	pF

NOTE 4: Three-terminal guarded measurement, unmeasured terminal voltage bias is zero.

#### thermal characteristics

PARAMETER		TEST CONDITIONS	MIN	ТҮР	МАХ	UNIT
$R_{\thetaJA}$	Junction to free air thermal resistance	$P_{tot} = 0.8 \text{ W}, T_A = 25 ^{\circ}\text{C}, 5  \text{cm}^2,  \text{FR4 PCB}$			160	°C/W

# **TISP7015D**

# TRIPLE ELEMENT THYRISTOR OVERVOLTAGE PROTECTORS

JULY 2000 - REVISED DECEMBER 2001



Figure 1. VOLTAGE-CURRENT CHARACTERISTIC FOR ANY TERMINAL PAIR



# TRIPLE ELEMENT THYRISTOR OVERVOLTAGE PROTECTORS

JULY 2000 - REVISED DECEMBER 2001

### MECHANICAL DATA

### D008

#### plastic small-outline package

This small-outline package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.



NOTES: A. Leads are within 0,25 (0.010) radius of true position at maximum material condition.

- B. Body dimensions do not include mold flash or protrusion.
- C. Mold flash or protrusion shall not exceed 0,15 (0.006).
- D. Lead tips to be planar within  $\pm 0,051$  (0.002).

# TISP7015D

# TRIPLE ELEMENT THYRISTOR OVERVOLTAGE PROTECTORS

JULY 2000 - REVISED DECEMBER 2001

#### **MECHANICAL DATA**

# D008

### tape dimensions



NOTES: A. Taped devices are supplied on a reel of the following dimensions:-

330 +0,0/-4,0 mm

100 ±2,0 mm

13,0 ±0,2 mm

MDXXATB

B. 2500 devices are on a reel.

Reel diameter: Reel hub diameter:

Reel axial hole:



# TRIPLE ELEMENT THYRISTOR OVERVOLTAGE PROTECTORS

JULY 2000 - REVISED DECEMBER 2001

#### **IMPORTANT NOTICE**

Power Innovations Limited (PI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to verify, before placing orders, that the information being relied on is current.

PI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with PI's standard warranty. Testing and other quality control techniques are utilized to the extent PI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

PI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor is any license, either express or implied, granted under any patent right, copyright, design right, or other intellectual property right of PI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

PI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORISED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS.

Copyright © 2001, Power Innovations Limited