Dual Axis ±1.7 *g* Accelerometer with SPI® Interface

Preliminary Technical Data

ADIS16003

FEATURES

Dual-axis accelerometer
SPI digital output interface
Internal temperature sensor
Highly integrated; minimal external components
Bandwidth externally selectable
1.5 m*g* resolution at 60 Hz
Externally controlled electrostatic self-test
5.2 V to 5.25 V single-supply operation
Low power: < 2 mA
3500 *g* shock survival
7 mm × 7 mm × 3.6 mm package

APPLICATIONS

Industrial vibration/motion sensing
Platform stabilization
Dual-axis tilt sensing
Tracking, recording, analysis devices
Alarms, security devices

GENERAL DESCRIPTION

The ADIS16003 is a low cost, low power, complete dual-axis accelerometer with an integrated serial output port interface (SPI). An integrated temperature sensor is also available on the SPI interface. The ADIS16003 measures acceleration with a full-scale range of ±1.7 *g* (typical). The ADIS16003 can measure both dynamic acceleration (for example, vibration) and static acceleration (for example, gravity).

The typical noise floor is 110 µg/√Hz allowing signals below 2 m*g* (60 Hz bandwidth) to be resolved.

The bandwidth of the accelerometer is set with capacitors C_X and C_Y at the X_{FILT} and Y_{FILT} pins. Selection of the two analog input channels is controlled by the DIN input.

An externally driven self-test pin (ST) allows the user to verify the accelerometer functionality.

The ADIS16003 is available in a 7 mm × 7 mm × 3.6 mm, 12-terminal LGA package.

FUNCTIONAL BLOCK DIAGRAM

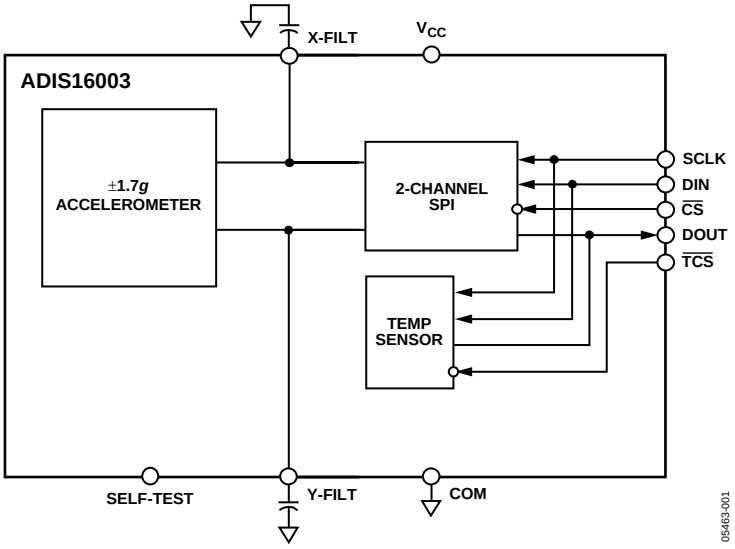

Figure 1.

Rev. PrA

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REVISION HISTORY

3/05—Revision PrA

SPECIFICATIONS

T_A = –40°C to +125°C, V_{CC} = 5 V, C_X = C_Y = 0.1 µF, acceleration = 0 *g*, unless otherwise noted. All minimum and maximum specifications are guaranteed. Typical specifications are not guaranteed.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
ACCELEROMETER SENSOR INPUT	Each axis				
Measurement Range		±1.7			*g*
Nonlinearity	% of full scale		±0.5	±2.5	%
Package Alignment Error			1.5		Degrees
Alignment Error	X sensor to Y sensor[1]		±0.1		Degrees
Cross Axis Sensitivity			±2	±5	%
ACCELEROMETER SENSITIVITY	Each axis				
Sensitivity at X_{FILT}, Y_{FILT}	V_{CC} = 5 V	1.13	1.22	1.30	mg/LSB
Sensitivity Change due to Temperature[2]	Delta from 25°C		±8		LSB
ZERO *g* BIAS LEVEL	Each axis				
0 *g* Voltage at X_{FILT}, Y_{FILT}	V_{CC} = 5 V	1905	2048	2190	LSB
0 *g* Offset vs. Temperature			±0.14		LSB/°C
ACCELEROMETER NOISE PERFORMANCE					
Noise Density	@25°C		110		µ*g*/√Hz rms
ACCELEROMETER FREQUENCY RESPONSE[3]					
C_X, C_Y Range[4]		0		10	µF
R_{FILT} Tolerance		24	32	40	kΩ
Sensor Resonant Frequency			5.5		kHz
ACCELEROMETER SELF TEST[5]					
Logic Input Low				1	V
Logic Input High		4			V
ST Input Resistance to Ground		30	50		kΩ
Output Change at X_{OUT}, Y_{OUT}	Self Test 0 to 1	323	614	904	LSB
TEMPERATURE SENSOR					
Accuracy	V_{CC} = 3 V to 5.25 V		±2		°C
Resolution			10		Bits
Update Rate			400		µs
Temperature Conversion Time			25		µs
DIGITAL INTPUT					
Input High Voltage (V_{INH})	V_{CC} = 5 V	2.4			V
	V_{CC} = 3.3 V	2.1			V
Input Low Voltage (V_{INL})				0.8	V
Input Current	V_{IN}= 0 V to V_{CC}		±10		µA
Input Capacitance			10		pF
DIGITAL OUTPUT					
Output High Voltage (V_{OH})	I_{SOURCE} = 200 µA	V_{CC} – 0.5			V
Output Low Voltage (V_{OL})	I_{SINK} = 200 µA			0.4	V
POWER SUPPLY					
Operating Voltage Range		3.0		5.25	V
Quiescent Supply Current			1.5	2.0	mA
Turn-On Time[6]	C_{FILT} in µF		20		ms

[1] Guaranteed by measurement of initial offset and sensitivity.
[2] Defined as the output change from ambient-to-maximum temperature or ambient-to-minimum temperature.
[3] Actual frequency response controlled by user-supplied external capacitor (C_X, C_Y).
[4] Bandwidth – $1/(2\pi \times 32\ k\Omega \times (2200\ pF + C))$. For C_X, C_Y = 0, bandwidth = 2200 Hz. For C_X, C_Y = 10 µF, bandwidth = 0.5 Hz. Min/max values are not tested.
[5] Self-test response changes as the square of V_S.
[6] Larger values of C_X, C_Y increase turn-on time. Turn-on time is approximately 160 × (2200 pF + C_X or C_Y) + 4 ms, where C_X, C_Y are in µF.

TIMING SPECIFICATIONS

T_A = −40°C to +125°C, acceleration = 0 *g*, unless otherwise noted.

Table 2.

Parameter[1, 2]	V_{CC} = 3.3	V_{CC} = 5	Unit	Description
f_{SCLK}[3]	10	10	kHz min	
	2	2	MHz max	
$t_{CONVERT}$	14.5 t_{SCLK}	14.5 t_{CSLK}		
t_{ACQ}	1.5 t_{SCLK}	1.5 t_{SCLK}		Throughput time = $t_{CONVERT}$ + t_{ACQ} = 16 t_{SCLK}
t_1	10	10	ns min	$\overline{CS}$ to SCLK setup time
t_2[4]	60	30	ns max	Delay from $\overline{CS}$ until DOUT three-state disabled
t_3[4]	100	75	ns max	Data access time after SCLK falling edge
t_4	20	20	ns min	Data setup time prior to SCLK rising edge
t_5	20	20	ns min	Data hold time after SCLK rising edge
t_6	0.4 × t_{SCLK}	0.4 x t_{SCLK}	ns min	SCLK high pulse width
t_7	0.4 × t_{SCLK}	0.4 x t_{SCLK}	ns min	SCLK low pulse width
t_8[5]	80	80	ns max	$\overline{CS}$ rising edge to DOUT high impedance
t_9	5	5	us typ	Power-up time from shutdown
t_{10}	0	0	ns min	$\overline{TCS}$ to SCLK setup time
t_{11}	50	50	ns min	SCLK high pulse width
t_{12}	50	50	ns min	SCLK low pulse width
t_{13}[4]	35	35	ns max	Data access time after SCLK falling edge
t_{14}	20	20	ns min	Data setup time prior to SCLK rising edge
t_{15}	0	0	ns min	Data Hold time after SCLK rising edge
t_{16}	0	0	ns min	$\overline{TCS}$ to SCLK hold time
t_{17}	40	40	ns max	$\overline{TCS}$ to DOUT high impedance

[1] Guaranteed by design. All input signals are specified with tr and tf = 5ns (10% to 90% of V_{CC}) and timed from a voltage level of 1.6 V. The 3.3 V operating range spans from 3.0 V to 3.6 V. The 5 V operating range spans from 4.75 V to 5.25 V.

[2] See Figure 3 and Figure 4.

[3] Mark/space ratio for the SCLK input is 40/60 to 60/40.

[4] Measured with the load circuit in Figure 2 and defined as the time required for the output to cross 0.4 V or 2.0 V with V_{CC} = 3.3 V and time for an output to cross 0.8 V or 2.4 V with V_{CC} = 5.0 V.

[5] t_8 is derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit in Figure 2. The measured number is then extrapolated back to remove the effects of charging or discharging the 50 pF capacitor. This means that the time, t_8, quoted in the timing characteristics is the true bus relinquish time of the part and is independent of the bus loading.

CIRCUIT AND TIMING DIAGRAMS

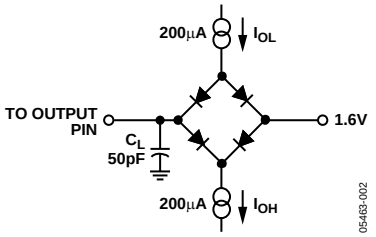

Figure 2. Load Circuit for Digital Output Timing Specifications

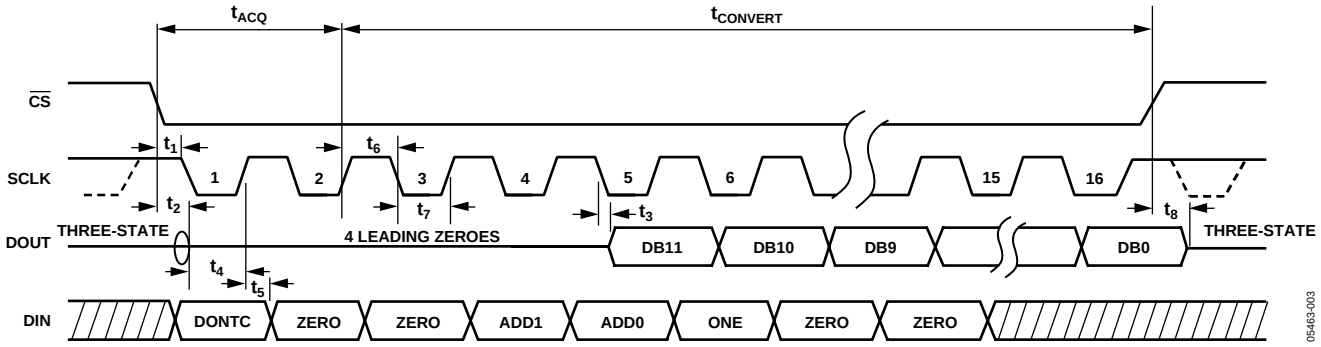

Figure 3. Accelerometer Serial Interface Timing Diagram

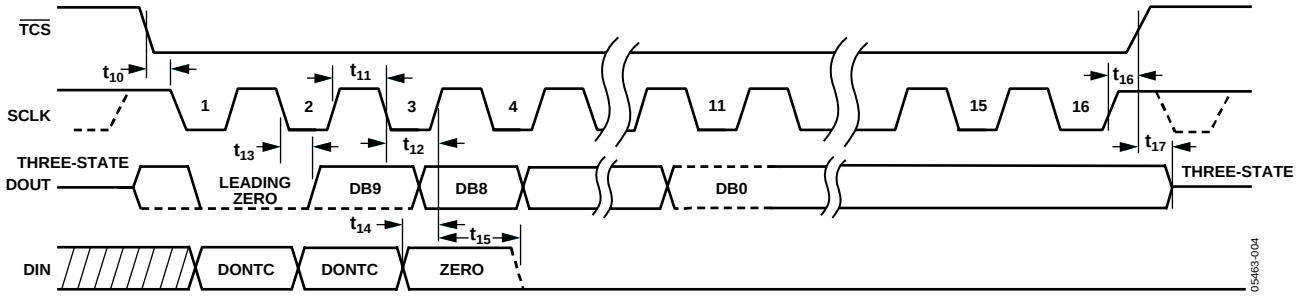

Figure 4. Temperature Serial Interface Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Acceleration (Any Axis, Unpowered)	3,500 *g*
Acceleration (Any Axis, Powered)	3,500 *g*
V_{CC}	–0.3 V to +7.0 V
All Other Pins	(COM – 0.3 V) to (V_{CC} + 0.3 V)
Output Short-Circuit Duration (Any Pin to Common)	Indefinite
Operating Temperature Range	–40°C to +125°C
Storage Temperature	–65°C to +150°C

Table 4. Package Characteristics

Package Type	θ_{JA}	θ_{JC}	Device Weight
12-Lead LGA			0.3 grams

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

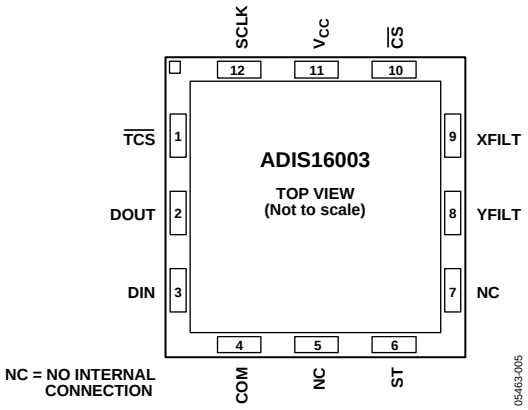

Figure 5. ADIS16003 12-Terminal LGA

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$\overline{TCS}$	Temperature Chip Select. Active low logic input. This input frames the serial data transfer for the temperature sensor output.
2	DOUT	Data Out. Logic Output. The conversion of the ADIS16003 is provided on this output as a serial data stream. The bits are clocked out on the falling edge of the SCLK input. The data stream consists of four leading zeroes followed by the 12 bits of conversion data, which is provided MSB first.
3	DIN	Data In. Logic Input. Data to be written into the ADIS16003's control register is provided on this input and is clocked into the register on the rising edge of SCLK.
4	COM	Common. Reference point for all circuitry on the ADIS16003.
5,7	NC	No Connect.
6	ST	Self Test Input. Active high logic input. Simulates a nominal 0.75 *g* test input for diagnostic purpose.
8	YFILT	Y Channel Filter Node. Used in conjunction with an optional external capacitor to band limit the ac signal from the accelerometer.
9	XFILT	X Channel Filter Node. Used in conjunction with an optional external capacitor to band limit the ac signal from the accelerometer.
10	$\overline{CS}$	Chip Select. Active low logic input. This input provides the dual function of initiating the accelerometer conversions on the ADIS16003 and also frames the serial data transfer for the accelerometer output.
11	V_{CC}	Power Supply Input. The V_{CC} range for the ADIS16003 is from 3.0 V to 5.25 V.
12	SCLK	Serial Clock. Logic Input. SCLK provides the serial clock for accessing data from the part and writing serial data to the control register. This clock input is also used as the clock source for the ADIS16003's conversion process.

OUTLINE DIMENSIONS

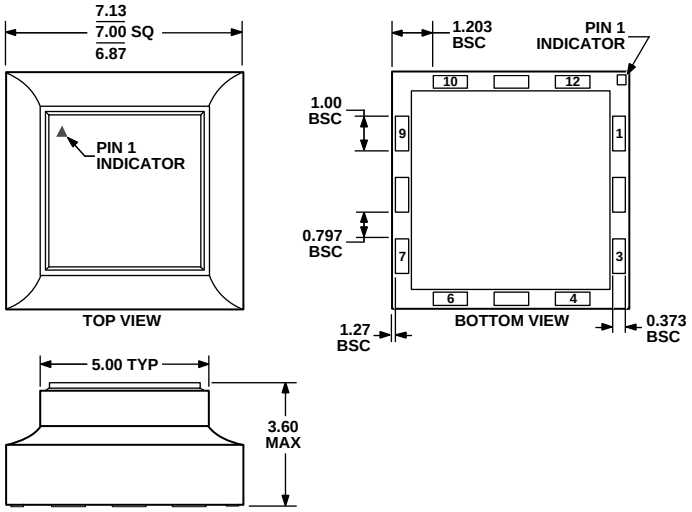

Figure 6. 12-Terminal Land Grid Array [LGA]
(CC-12)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADIS16003CCC	–40°C to +125°C	12-Terminal Land Grid Array (LGA)	CC-12
ADIS16003/PCB	25°C	Evaluation Board	

PR05463–0–3/05(PrA)