NTSC/PAL AUDIO CLOCK

CONFIDENTIAL

ICS662-02

Description

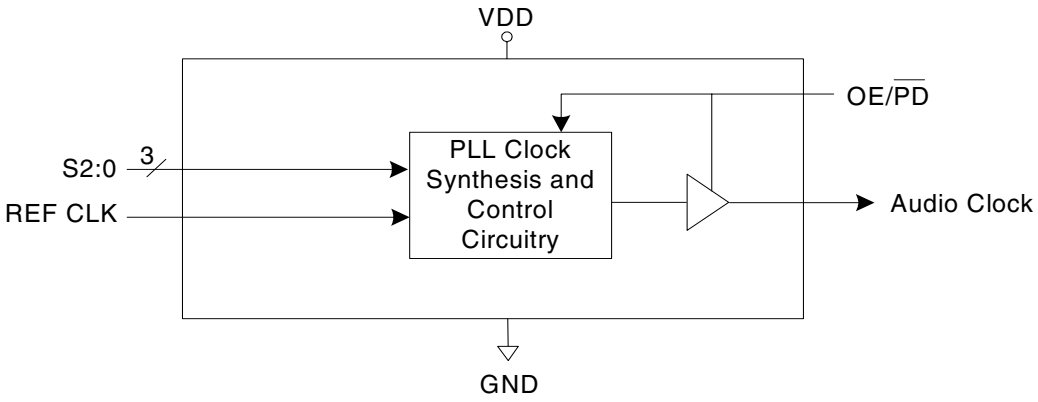
The ICS662-02 is a low cost, low jitter, high performance PLL clock synthesizer designed to replace oscillators and PLL circuits in set-top box and multimedia systems. Using ICS' patented analog Phase Locked Loop (PLL) techniques, the device uses a NTSC/PAL reference clock input to produce a selectable audio clock.

ICS manufactures the largest variety of Set-Top Box and multimedia clock synthesizers for all applications. Consult ICS to eliminate VCXOs, crystals and oscillators from your board.

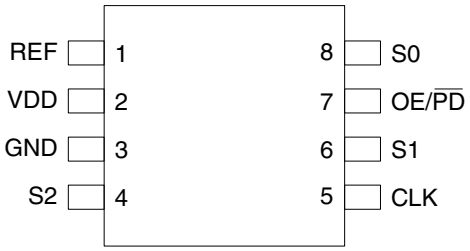
Features

- Packaged in 8 pin SOIC
- Locks to NTSC and PAL colorburst frequencies (4x)
- Audio sampling rate outputs
- Low synthesis error in all clocks
- All frequencies are frequency locked
- Advanced, low power, sub-micron CMOS process
- Operating voltage of 3.3 V

Block Diagram



Pin Assignment



8 pin (150 mil) SOIC

CLOCK OUTPUT SELECT TABLE

S2	S1	S0	Input Frequency	Output Frequency	Video Std.
0	0	0	14.318$\overline{18}$	8.192	NTSC
0	0	1	14.318$\overline{18}$	11.2896	NTSC
0	1	0	14.318$\overline{18}$	12.288	NTSC
0	1	1	14.318$\overline{18}$	24.576	NTSC
1	0	0	17.73447205*	8.192	PAL
1	0	1	17.73447205*	11.2896	PAL
1	1	0	17.73447205*	12.288	PAL
1	1	1	17.73447205*	24.576	PAL

* -0.16 ppm compared to PAL specification

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	REF	Input	Reference clock input.
2	VDD	Power	Connect to +3.3 V.
3	GND	Power	Connect to ground.
4	S2	Input	Output frequency selection Pin 2. Determines output frequency as per table above.
5	CLK	Output	Clock output per table above.
6	S1	Input	Output frequency selection Pin 1. Determines output frequency as per table above.
7	OE/$\overline{PD}$	Input	Output enable. Powers down PLL and tri-states output with weak pull-down when low.
8	S0	Input	Output frequency selection Pin 0. Determines output frequency as per table above.

External Components

Decoupling Capacitor

As with any high performance mixed-signal IC, the ICS662-02 must be isolated from system power supply noise to perform optimally.

A decoupling capacitor of 0.01µF must be connected between VDD and GND on pins 2 and 3. It must be connected close to the ICS662-02 to minimize lead inductance. No external power supply filtering is required for the ICS662-02.

Series Termination Resistor

A 33Ω terminating resistor can be used next to the clock outputs for trace lengths over one inch.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS662-02. These ratings, which are standard values for ICS commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	-0.5 V to 4 V
All Inputs and Outputs	-0.5 V to VDD+0.5 V
Ambient Operating Temperature	0 to +70°C
Storage Temperature	-65 to +150°C
Soldering Temperature	260°C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	0		+70	°C
Power Supply Voltage (measured in respect to GND)	+3.0		+3.6	V

DC Electrical Characteristics

VDD=3.3 V ±10% , Ambient temperature 0 to +70°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.0		3.6	V
Supply Current	IDD	No Load, OE/$\overline{PD}$=1, first 4 modes		20		mA
		No Load, OE/$\overline{PD}$=1, last 4 modes		25		mA
	IDDPD	No load, OE/$\overline{PDTS}$=0		125		µA
Input High Voltage	V_{IH}	OE/$\overline{PD}$ pin only	VDD - 0.5			V
Input Low Voltage	V_{IL}	OE/$\overline{PD}$ pin only			0.5	V
Input High Voltage	V_{IH}	S2:S0, REF pins	2.0			V
Input Low Voltage	V_{IL}	S2:S0, REF pins			0.8	V
Output High Voltage	V_{OH}	I_{OH} = -12 mA	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 12 mA			0.4	V
Output High Voltage, CMOS level	V_{OH}	I_{OH} = -4 mA	VDD-0.4			V
Short Circuit Current	I_{OS}	CLK outputs		±50		mA
Input Capacitance	C_{IN}			5		pF
Nominal Output Impedance	Z_{OUT}			20		Ω
Internal pull-up resistor	R_{PU}	S2 pin		510		kΩ
		S1, S0 OE/$\overline{PD}$		120		kΩ
Internal pull-down resistor	R_{PD}	CLK pin		240		kΩ

AC Electrical Characteristics

VDD = 3.3 V ±10%, Ambient Temperature 0 to +70° C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Crystal or Clock Frequency	F_{IN}		10		20	MHz
Frequency Synthesis Error		NTSC Clocks			0	ppm
		PAL Clocks	-0.16			ppm
Output Clock Rise Time	t_{OR}	20% to 80%, Note 1			1.5	ns
Output Clock Fall Time	t_{OF}	80% to 20%, Note 1			1.5	ns
Output Clock Duty Cycle		at VDD/2, Note 1	45		55	%
Maximum Absolute Jitter, short term		Deviation from mean, Note 1		±100		ps
Maximum Absolute Jitter, long term		Deviation from mean, Note 1, 10 μs delay		±400		ps

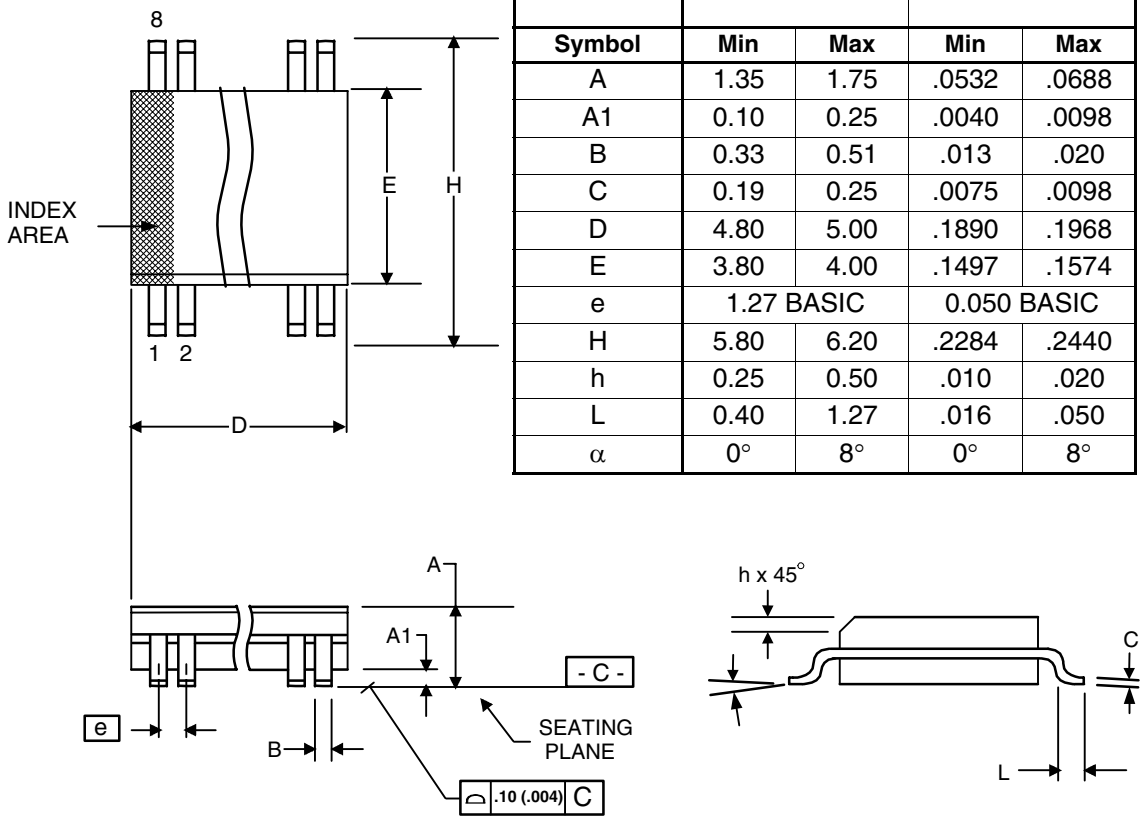
Note 1: Measured with 15 pF load.

Thermal Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		150		°C/W
	θ_{JA}	1 m/s air flow		140		°C/W
	θ_{JA}	3 m/s air flow		120		°C/W
Thermal Resistance Junction to Case	θ_{JC}			40		°C/W

Package Outline and Package Dimensions (8 pin SOIC, 150 Mil. Narrow Body)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters		Inches	
Symbol	**Min**	**Max**	**Min**	**Max**
A	1.35	1.75	.0532	.0688
A1	0.10	0.25	.0040	.0098
B	0.33	0.51	.013	.020
C	0.19	0.25	.0075	.0098
D	4.80	5.00	.1890	.1968
E	3.80	4.00	.1497	.1574
e	1.27 BASIC		0.050 BASIC	
H	5.80	6.20	.2284	.2440
h	0.25	0.50	.010	.020
L	0.40	1.27	.016	.050
α	0°	8°	0°	8°

Ordering Information

Part / Order Number (Note 1)	Marking	Shipping packaging	Package	Temperature
ICS662M-02	662M-02	Tubes	8 pin SOIC	0 to +70° C
ICS662M-02TR	662M-02	Tape and Reel	8 pin SOIC	0 to +70° C

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