ICS93727 **Preliminary Product Preview**

DDR Phase Lock Loop Zero Delay Clock Buffer (patent pending)

Recommended Application:

DDR Zero Delay Clock Buffer

Product Description/Features:

- Low skew, low jitter PLL clock driver
- I²C for functional and output control
- Spread Spectrum tolerant inputs
- Input to output skew control (RFIX, RSTEP) (patent pending)
- Northbridge reference clock for output delay control

Switching Characteristics:

- PEAK PEAK jitter (66MHz): <120ps
- PEAK PEAK jitter (>100MHz): <75ps
- CYCLE CYCLE jitter (66MHz):<120ps
- CYCLE CYCLE jitter (>100MHz):<65ps
- OUTPUT OUTPUT skew: <100ps
- Output Rise and Fall Time: 450ps 950ps
- **DUTY CYCLE: 49% 51%**

Functionality

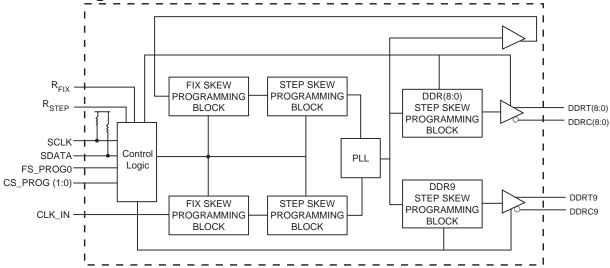
IN	OUTPUTS			PLL State	
AVDD	CLKIN	DDRT	DDRT DDRC FB		PLL State
2.5V (NOM)	AVERAGE VOLTAGE > 0.4V	IN PHASE WITH CLKIN			ON
2.5V (NOM)	2.5V (NOM) AVERAGE VOLTAGE < 0.4V HI Z		HI Z	HI Z	OFF
GND	Ь	L	Н	L	BYPASSED/OFF
GND	Н	H L H			BYPASSED/OFF

Pin Configuration

			-						
GND	1	48	GND						
DDRC0	2	47	DDRC5						
DDRT0	3	46	DDRT5						
VDD2.5	4	45	VDD2.5						
DDRT1	5	44	DDRT6						
DDRC1	6	43	DDRC6						
GND	7	42	GND						
GND	8	41	GND						
DDRC2	9	40	DDRC7						
DDRT2	10	> 39	DDRT7						
VDD2.5	11	N 38	VDD2.5						
SCLK	12	\mathfrak{S} 37	SDATA						
CLK_IN	13	CS93727	CS_PROG1*						
**FS_PROG0	14	35	R _{FIX}						
VDD2.5	15	⊆ 34	VDD2.5						
AVDD	16	33	R _{STEP}						
AGND	17	32	CS_PROG0**						
GND	18	31	GND						
DDRC3	19	30	DDRC8						
DDRT3	20	29	DDRT8						
VDD2.5	21	28	VDD2.5						
DDRT4	22	27	DDRT9						
DDRC4	23	26	DDRC9						
GND	24	25	GND						
•	48-SSOP								

48-SSOF

Block Diagram



0711B-10/10/02

^{*} Internal Pull-Up Resistor

^{**} Internal Pull-Down Resistor



Preliminary Product Preview

Pin Descriptions

Name	PIN	PIN	DIN	
GND			PIN	DESCRIPTION
DDRC0			_	Cround nin
3 DDRT0				·
4				
5 DDRT1				·
6 DDRC1 OUT Complementary* Clock of differential pair output. 7 GND PVR Ground pin. 8 GND PVR Ground pin. 9 DDRC2 OUT **Complementary** Clock of differential pair output. 10 DDRT2 OUT **True** Clock of differential pair output. 11 VDD2.5 PVR Power supply, nominal 2.5V 12 SCLK IN Clock pin of 12C circuitry SV tolerant 13 CLK.IN IN Reference clock put. 14 **FS_PROG0 IN Latch input pin to change Byte 1 bit 7 Fine Skew Programming default polarity (Pulling this bit low will set DDR output to be advance vs the input). 15 VDD2.5 PWR Power supply, nominal 2.5V 4 AVDD PVR Power supply, nominal 2.5V 16 AVDD PVR Rod Ground pin. 17 ASDN PVR Rod Ground pin. 21 VDD2.5 PVR Power supply, nominal 2.5V 21 VDD2.5 PVR Power supply, nominal 2.5V			_	****
7 GND PWR Ground pin. 8 GND PWR Ground pin. 9 DDRC2 OUT Tong-injementary* Clock of differential pair output. 10 DDRT2 OUT True* Clock of differential pair output. 11 VDD2.5 PWR Power supply, nominal 2.5V 12 SCLK IN Clock pin of I2C circuity SV tolerant 13 CLK,IN IN Reference clock input. 14 "FS_PRG0 IN Reference clock input. 15 VDD2.5 PWR PWR PWR 16 AVDD PWR PWR PWR 17 A6ND PWR Pwer supply, nominal 2.5V 18 GND PWR Analog Ground pin for Core PLL 17 A6ND PWR Analog Ground pin. 18 GND PWR Analog Ground pin. 20 DDRT3 OUT True* Clock of differential pair output. 21 NDD2.5 PWR Power supply, nominal 2.5V				·
8 GND PWR Ground pin. 9 DDRC2 OUT "True" Clock of differential pair output. 111 VDD2.5 PWR Power supply, nominal 2.5V 122 SCLK IN Clock pin of I2C circuitry 5V tolerant 13 CLK_IN IN Reference clock hiput. 14 "FS_PROGO II Latch input pin to change Byte 1 bit 7 Fine Skew Programming default polarity (Pulling this bit liby VDD2.5 PWR Power supply, nominal 2.5V 15 VDD2.5 PWR Power supply, nominal 2.5V 16 AVDD PWR Analog Ground pin for Core PLL 17 AGNID PWR Analog Ground pin for Core PLL 18 GND PWR Ground pin. 19 DDRC3 OUT "Complementary" Clock of differential pair output. 20 DDRT3 OUT "True" Clock of differential pair output. 21 VDD2.5 PWR Power supply, nominal 2.5V 22 DDRT4 OUT "True" Clock of differential pair output. 23 DDRC4 OUT "Complementary" Clock of differential pair output. 24 GND PWR Ground pin. 25 GND PWR Ground pin. 26 DDRC3 OUT "Complementary" Clock of differential pair output. 27 VDD2.5 PWR Ground pin. 28 VDD2.5 PWR Ground pin. 29 DDRT4 OUT "True" Clock of differential pair output. 30 DDRC4 OUT "Complementary" Clock of differential pair output. 31 DDRC4 OUT "Complementary" Clock of differential pair output. 32 DDRC5 OUT "Complementary" Clock of differential pair output. 33 DDRC6 OUT "True" Clock of differential pair output. 34 VDD2.5 PWR Power supply, nominal 2.5V 35 GND PWR Ground pin. 36 VDD2.6 PWR Power supply, nominal 2.5V 37 DDRT9 OUT "True" Clock of differential pair output. 38 VDD2.5 PWR Power supply, nominal 2.5V 39 DDRT8 OUT "True" Clock of differential pair output. 30 DDRC8 OUT "Complementary" Clock of differential pair output. 31 GND PWR Ground pin. 32 CS_PROGO** 33 RSTEP IN Externa pull-down resistor can be set on this pin to program input vs DDR clocks skew. 34 VDD2.5 PWR Power supply, nominal 2.5V 35 RFIX IN Externa pull-down resistor can be set on this pin to program input vs DDR clocks skew. 36 CS_PROGO** 37 DDRT9 OUT "True" Clock of differential pair output. 38 DDRT9 OUT "True" Clock of differential pair output. 39 DDRT9 OUT "True" Clock of differential pair output. 40 DDRC5 OUT "Comp				
9 DDRC2 OUT 'Complementary' Clock of differential pair output. 10 DDRT2 OUT 'True' Clock of differential pair output. 11 VDD2.5 PWR Power supph, normal 2.5V 12 SCLK IN Clock pin of I2C circuitry 5V tolerant 13 CLK.IN IN Reference clock input. 14 "FS.PROG0 IN Reference clock input. 15 VDD2.5 PWR Power supph, normal 2.5V 16 AVDD PWR Power supph, normal 2.5V 17 AGND PWR Analog Ground pin for Core PLL 18 GND PWR Analog Ground pin for Core PLL 19 DDRC3 OUT 'Complementary' Clock of differential pair output. 19 DDRC3 OUT 'True' Clock of differential pair output. 20 DDRT3 OUT 'True' Clock of differential pair output. 21 VDD2.5 PWR Power supph, normal 2.5V 22 DDRT4 OUT 'True' Clock of differential pair output. 23 DDRC4 OUT 'Complementary' Clock of differential pair output. 24 GND PWR Ground pin. 25 GND PWR Ground pin. 26 DDRC3 OUT 'Complementary' Clock of differential pair output. 27 DDRT9 OUT 'True' Clock of differential pair output. 28 VDD2.5 PWR Power supph, normal 2.5V 29 DDRT8 OUT 'True' Clock of differential pair output. 20 DDRT9 OUT 'True' Clock of differential pair output. 27 DDRT9 OUT 'True' Clock of differential pair output. 28 VDD2.5 PWR Power supph, normal 2.5V 29 DDRT8 OUT 'True' Clock of differential pair output. 30 DDRC3 OUT 'Complementary' Clock of differential pair output. 31 GND PWR Ground pin. 32 CS_PROG0" IN Externary Clock of differential pair output. 33 DDRC4 OUT 'Complementary' Clock of differential pair output. 34 VDD2.5 PWR Power supph, normal 2.5V 35 RFIX IN Externary Lindown resistor can be set on this pin to program input vs DDR clocks skew. 36 CS_PROG0" IN Externary Lindown resistor can be set on this pin to program input vs DDR clocks skew. 37 SDATA IN DATE of the put pin to change Byte 3 bit 5 Coarse Skew Programming default (Pulling this bit high will advance the DDR output vs the input, refer to table 1 for trining details). 38 FIX IN Externary Lindown resistor can be set on this pin to program input vs DDR clocks skew. 39 DDRT9 OUT 'True' Clock of diff				·
10 DDRT2 OUT True" Clock of differential pair output. 11 VDD2.5 PWR Power supply, nominal 2.5V 12 SCLK IN Clock pin of 122 critority 5V tolerant 13 CLK_IN IN Reference clock input. 14 "FS_PROGO IN Reference clock input. 15 VDD2.5 PWR Power supply, nominal 2.5V 16 AVDD PWR 25V Analog Power pin for Core PLL 17 AGND PWR Analog Ground pin for Core PLL 18 GND PWR Ground pin. 19 DDRC3 OUT "Complementary" Clock of differential pair output. 20 DDRT3 OUT "True" Clock of differential pair output. 21 DDRC4 OUT "Complementary" Clock of differential pair output. 22 DDRT4 OUT "Complementary" Clock of differential pair output. 23 DDRC4 OUT "Complementary" Clock of differential pair output. 24 GND PWR Ground pin. 25 GND PWR Ground pin. 26 DDRC9 OUT "Complementary" Clock of differential pair output. 27 DDRT9 OUT "True" Clock of differential pair output. 28 VDD2.5 PWR Ground pin. 29 DDRC4 OUT "Complementary" Clock of differential pair output. 20 DDRT9 OUT "True" Clock of differential pair output. 26 DDRC9 OUT "Complementary" Clock of differential pair output. 27 DDRT9 OUT "True" Clock of differential pair output. 28 VDD2.5 PWR Power supply, nominal 2.5V 29 DDRT9 OUT "True" Clock of differential pair output. 30 DDRC9 OUT "Complementary" Clock of differential pair output. 31 GND PWR Ground pin. 32 CS_PROGO" IN Latch input pin to change Byte 3 bit 5 Coarse Skew Programming default (Puling this bit high will advance the DDR output vs the input, refer to table 1 for timing details). 31 SRTEP IN Extrema pull-down resistor can be set on this pin to program input vs DDR clocks skew. 32 SDATA IN Extrema pull-down resistor can be set on this pin to program input vs DDR clocks skew. 33 VDD2.5 PWR Power supply, nominal 2.5V 34 VDD2.5 PWR Power supply, nominal 2.5V 35 GND PWR Power supply, on the put vs the input, refer to table 1 for timing details). 36 CS_PROGO1* IN Extrema pull-down resistor can be set on this pin to program input vs DDR clocks skew. 39 DDRT6 OUT "True" Clock of differential pair output. 40 DDRC5 OUT "Complementary" Clock				·
11 VDD2.5 PWR Power supply, nominal 2.5V 12 SCLK IN Clock pin of I2C circuitry 5V tolerant 13 CLK_IN IN Reference clock input. 14 "FS_PROGO IN Latch input pin to change Byte 1 bit 7 Fine Skew Programming default polarity (Pulling this bit low will set DDR output to be advance vs the input). 15 VDD2.5 PWR Power supply, nominal 2.5V 16 AVDD PWR 2.5V Analog Power pin for Core PLL 18 GND PWR Analog Ground pin for Core PLL 19 DDRC3 OUT "Complementary" Clock of differential pair output. 20 DDRT3 OUT "True" Clock of differential pair output. 21 VDD2.5 PWR Power supply, nominal 2.5V 22 DDRT4 OUT "True" Clock of differential pair output. 22 DDRC4 OUT "Complementary" Clock of differential pair output. 23 DDRC4 OUT "True" Clock of differential pair output. 24 GND PWR Ground pin. 25 GND PWR Ground pin. 26 DDRC9 OUT "True" Clock of differential pair output. 27 DDRT9 OUT "True" Clock of differential pair output. 28 VDD2.5 PWR Ground pin. 30 DDRC9 OUT "Complementary" Clock of differential pair output. 31 GND PWR Ground pin. 32 DDRC9 OUT "True" Clock of differential pair output. 33 DDRC9 OUT "Complementary" Clock of differential pair output. 34 DDRC9 OUT "True" Clock of differential pair output. 35 DDRC9 OUT "Complementary" Clock of differential pair output. 36 DDRC9 OUT "Complementary" Clock of differential pair output. 37 DDRT8 OUT "True" Clock of differential pair output. 38 VDD2.5 PWR Power supply, nominal 2.5V 39 DDRT8 OUT "Complementary" Clock of differential pair output. 30 DDRC8 OUT "Complementary" Clock of differential pair output. 31 GND PWR Ground pin. 32 CS_PROG0* IN Latch input pin to change Byte 3 bit 5 Coarse Skew Programming default (Pulling this bit high will advance the DDR output vs the input, refer to table 1 for timing details). 31 RSTEP IN Extrema pull-down resistor can be set on this pin to program input vs DDR clocks skew. 34 VDD2.5 PWR Power supply, nominal 2.5V 35 RFIX IN Extrema pull-down resistor can be set on this pin to program input vs DDR clocks skew. 36 VDD2.5 PWR Power supply, nominal 2.5V 37				
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13 CLK_IN IN Reference clock input. 14 "FS_PROGO IN Latch input pin to change Byte 1 bit 7 Fine Skew Programming default polarity (Pulling this bit wow will set DDR output to be advance vs the input). 15 VDD2.5 PVR Power supply, nominal 2.5V 16 AVDD PVR 2.5V Analog Power pin for Core PLL 17 AGND PVR Analog Ground pin for Core PLL 18 GND PVR Ground pin. 19 DDRC3 OUT "Complementary" Clock of differential pair output. 20 DDRT3 OUT "True" Clock of differential pair output. 21 VDD2.5 PVR Power supply, nominal 2.5V 22 DDRT4 OUT "True" Clock of differential pair output. 23 DDRC4 OUT "Complementary" Clock of differential pair output. 24 GND PVR Ground pin. 25 GND PVR Ground pin. 26 DDRC9 OUT "True" Clock of differential pair output. 27 DDRT9 OUT "True" Clock of differential pair output. 28 VDD2.5 PVR Ground pin. 29 DDRT8 OUT "True" Clock of differential pair output. 20 DDRC9 OUT "Complementary" Clock of differential pair output. 27 DDRT9 OUT "True" Clock of differential pair output. 28 VDD2.5 PVR Power supply, nominal 2.5V 29 DDRT8 OUT "True" Clock of differential pair output. 30 DDRC8 OUT "Complementary" Clock of differential pair output. 31 GND PVR Ground pin. 32 CS_PROGO** 33 DDRC8 OUT "Complementary" Clock of differential pair output. 34 VDD2.5 PVR Power supply, nominal 2.5V 35 RFIX IN Latch input pin to change Byte 3 bit 5 Coarse Skew Programming default (Pulling this bit high will advance the DDR output vs the input, refer to table 1 for timing details). 36 CS_PROGO** 37 SDATA IV OD Data pin for IZC Clock of differential pair output. 38 VDD2.5 PVR Power supply, nominal 2.5V 19 DDRT9 OUT "True" Clock of differential pair output. 39 DDRT7 OUT "True" Clock of differential pair output. 40 DDRC9 OUT "Complementary" Clock of differential pair output. 41 GND PVR Power supply, nominal 2.5V 42 SDATA IV OD Data pin for IZC Clock of differential pair output. 43 DDRC6 OUT "Complementary" Clock of differential pair output. 44 DDRT6 OUT "True" Clock of differential pair output. 45 DDRC6 OUT				
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15 VDD2.5	13	CLK_IIN	IIN	•
15	14	**FS_PROG0	IN	
16 AVDD	15	VDD2.5	PWR	
17 AGND PWR Analog Ground pin for Core PLL 18 GND PWR Ground pin. 20 DDRT3 OUT "Complementary" Clock of differential pair output. 21 VDD2.5 PWR Power supply, nominal 2.5V 22 DDRT4 OUT "True" Clock of differential pair output. 23 DDRC4 OUT "Complementary" Clock of differential pair output. 24 GND PWR Ground pin. 25 GND PWR Ground pin. 26 DDRC9 OUT "Complementary" Clock of differential pair output. 27 DDRT9 OUT "True" Clock of differential pair output. 28 VDD2.5 PWR Power supply, nominal 2.5V 29 DDRT9 OUT "True" Clock of differential pair output. 20 DDRC9 OUT "Complementary" Clock of differential pair output. 27 DDRT9 OUT "True" Clock of differential pair output. 28 VDD2.5 PWR Power supply, nominal 2.5V 29 DDRTB OUT "True" Clock of differential pair output. 30 DDRC8 OUT "Complementary" Clock of differential pair output. 31 GND PWR Ground pin. 32 CS_PROG0" IN Latch input pin to change Byte 3 bit 5 Coarse Skew Programming default (Pulling this bit high will advance the DDR output vs the input, refer to table 1 for timing details). 33 RSTEP IN Extnerna pull-down resistor can be set on this pin to program input vs DDR clocks skew. 34 VDD2.5 PWR Power supply, nominal 2.5V 35 RFIX IN Extnerna pull-down resistor can be set on this pin to program input vs DDR clocks skew. 36 CS_PROG1" IN Extnerna pull-down resistor can be set on this pin to program input vs DDR clocks skew. 37 SDATA I/O Data pin for I2C circuitry 5V tolerant 38 DDRT7 OUT "True" Clock of differential pair output. 49 DDRC6 OUT "Complementary" Clock of differential pair output. 40 DDRC7 OUT "Complementary" Clock of differential pair output. 41 GND PWR GROUND PWR G	16		PWR	
18 GND PWR Ground pin. 19 DDRC3 OUT "Complementary" Clock of differential pair output. 20 DDRT3 OUT "True" Clock of differential pair output. 21 VDD2.5 PWR Power supply, nominal 2.5V 22 DDRT4 OUT "True" Clock of differential pair output. 23 DDRC4 OUT "Complementary" Clock of differential pair output. 24 GND PWR Ground pin. 25 GND PWR Ground pin. 26 DDRC9 OUT "Complementary" Clock of differential pair output. 27 DDRT9 OUT "True" Clock of differential pair output. 28 VDD2.5 PWR Power supply, nominal 2.5V 29 DDRT8 OUT "True" Clock of differential pair output. 30 DDRC8 OUT "True" Clock of differential pair output. 31 GND PWR Ground pin. 32 CS_PROG0** 31 Latch input pin to change Byte 3 bit 5 Coarse Skew Programming default (Pulling this bit high will advance the DDR output vs the input, refer to table 1 for timing details). 33 RSTEP IN Exnterna pull-down resistor can be set on this pin to program input vs DDR clocks skew. 34 VDD2.5 PWR Power supply, nominal 2.5V 35 RFIX IN Exnterna pull-down resistor can be set on this pin to program input vs DDR clocks skew. 36 CS_PROG1* 37 SDATA I/O Data pin for I2C circuitry 5V tolerant 38 DDRT7 OUT "True" Clock of differential pair output. 40 DDRC7 OUT "Complementary" Clock of differential pair output. 41 GND PWR Ground pin. 42 GND PWR Ground pin. 43 DDRC6 OUT "Complementary" Clock of differential pair output. 44 DDRT6 OUT "True" Clock of differential pair output. 45 DDRC6 OUT "Complementary" Clock of differential pair output. 46 DDRT6 OUT "True" Clock of differential pair output. 47 DDRC5 OUT "True" Clock of differential pair output.	17		PWR	Analog Ground pin for Core PLL
DDRC3 OUT "Complementary" Clock of differential pair output. DDRT3 OUT "True" Clock of differential pair output. PWR Power supply, nominal 2.5V DDRT4 OUT "True" Clock of differential pair output. DDRC4 OUT "Complementary" Clock of differential pair output. SDRC4 OUT "Complementary" Clock of differential pair output. GRID PWR Ground pin. DDRC9 OUT "Complementary" Clock of differential pair output. DDRC9 OUT "True" Clock of differential pair output. PWR OFTEN OUT "True" Clock of differential pair output. DDRC9 OUT "True" Clock of differential pair output. DDRC9 OUT "True" Clock of differential pair output. DDRC9 OUT "True" Clock of differential pair output. DDRC8 OUT "True" Clock of differential pair output. DDRC8 OUT "Complementary" Clock of differential pair output. CS_PROG0** OUT "Complementary" Clock of differential pair output. CS_PROG0** IN Latch input pin to change Byte 3 bit 5 Coarse Skew Programming default (Pulling this bit high will advance the DDR output vs the input, refer to table 1 for timing details). RFIX IN Exnterna pull-down resistor can be set on this pin to program input vs DDR clocks skew. DDRC9 OUT "Complementary" Clock of differential pair output. Latch input pin to change Byte 3 bit 7 Coarse Skew Programming default (Pulling this bit high will advance the DDR output vs the input, refer to table 1 for timing details). RFIX IN Exnterna pull-down resistor can be set on this pin to program input vs DDR clocks skew. Latch input pin to change Byte 3 bit 7 Coarse Skew Programming default (Pulling this bit high will advance the DDR output vs the input, refer to table 1 for timing details). DDRC6 OUT "True" Clock of differential pair output. ODRC7 OUT "True" Clock of differential pair output. DDRC6 OUT "Complementary" Clock of differential pair output. DDRC6 OUT "True" Clock of differential pair output. DDRC7 OUT "True" Clock of differential pair output.	18		PWR	Ground pin.
DDRT3 OUT "True" Clock of differential pair output. PWR Power supply, nominal 2.5V DDRT4 OUT "Complementary" Clock of differential pair output. DDRC4 OUT "Complementary" Clock of differential pair output. DDRC4 OUT "Complementary" Clock of differential pair output. DDRC9 OUT "Complementary" Clock of differential pair output. DDRC9 OUT "Complementary" Clock of differential pair output. DDRC9 OUT "True" Clock of differential pair output. DDRC9 OUT "True" Clock of differential pair output. DDRT9 OUT "True" Clock of differential pair output. DDRC8 OUT "Complementary" Clock of differential pair output. CS_PRO60" IN Latch input pin to change Byte 3 bit 5 Coarse Skew Programming default (Pulling this bit high will advance the DDR output vs the input, refer to table 1 for timing details). RSTEP IN Exnterna pull-down resistor can be set on this pin to program input vs DDR clocks skew. CS_PRO61" IN Exnterna pull-down resistor can be set on this pin to program input vs DDR clocks skew. CS_PRO61" IN Exnterna pull-down resistor can be set on this pin to program input vs DDR clocks skew. CS_PRO61" IN Exnterna pull-down resistor can be set on this pin to program input vs DDR clocks skew. CS_PRO61" IN Exnterna pull-down resistor can be set on this pin to program input vs DDR clocks skew. CS_PRO61" IN Exnterna pull-down resistor can be set on this pin to program input vs DDR clocks skew. CS_PRO61" IN Exnterna pull-down resistor can be set on this pin to program input vs DDR clocks skew. DDRC5 PWR Power supply, nominal 2.5V DDRC6 OUT "True" Clock of differential pair output. DDRC7 OUT "True" Clock of differential pair output. TUP Clock of differential pair output. DDRC6 OUT "True" Clock of differential pair output. DDRC7 OUT "True" Clock of differential pair output.	19		OUT	·
21				
DRT4 OUT "True" Clock of differential pair output. OUT "Complementary" Clock of differential pair output. Ground pin. FWR Ground pin. DRC9 OUT "Complementary" Clock of differential pair output. DRC9 OUT "Complementary" Clock of differential pair output. DRC9 OUT "True" Clock of differential pair output. PWR Power supply, nominal 2.5V DRT9 OUT "True" Clock of differential pair output. DRC9 OUT "True" Clock of differential pair output. DRC8 OUT "Complementary" Clock of differential pair output. GRND PWR Ground pin. CS_PROG0** IN Latch input pin to change Byte 3 bit 5 Coarse Skew Programming default (Pulling this bit high will advance the DDR output vs the input, refer to table 1 for timing details). RESTEP IN Exnterna pull-down resistor can be set on this pin to program input vs DDR clocks skew. WDD2.5 PWR Power supply, nominal 2.5V IN Exnterna pull-down resistor can be set on this pin to program input vs DDR clocks skew. CS_PROG1* IN Exnterna pull-down resistor can be set on this pin to program input vs DDR clocks skew. CS_PROG1* IN Latch input pin to change Byte 3 bit 7 Coarse Skew Programming default (Pulling this bit high will advance the DDR output vs the input, refer to table 1 for timing details). SDATA I/O Data pin for I2C circuitry 5V tolerant Power supply, nominal 2.5V True" Clock of differential pair output. GROND PWR Ground pin. GROUND PWR Ground pin. GROND PWR Ground pin. GROUND PWR Ground pin. Complementary" Clock of differential pair output. DDRC6 OUT "Complementary" Clock of differential pair output. True" Clock of differential pair output.				·
DDRC4 OUT "Complementary" Clock of differential pair output. QND PWR Ground pin. Ground pin. Ground pin. Ground pin. Complementary" Clock of differential pair output. DDRC9 OUT "Complementary" Clock of differential pair output. POWER Supply, nominal 2.5V DDRT8 OUT "True" Clock of differential pair output. CS_PROG0** IN Latch input pin to change Byte 3 bit 5 Coarse Skew Programming default (Pulling this bit high will advance the DDR output vs the input, refer to table 1 for timing details). RES_PROG1* IN Externa pull-down resistor can be set on this pin to program input vs DDR clocks skew. POWER Supply, nominal 2.5V Externa pull-down resistor can be set on this pin to program input vs DDR clocks skew. Externa pull-down resistor can be set on this pin to program input vs DDR clocks skew. SS_PROG1* IN Externa pull-down resistor can be set on this pin to program input vs DDR clocks skew. Latch input pin to change Byte 3 bit 7 Coarse Skew Programming default (Pulling this bit high will advance the DDR output vs the input, refer to table 1 for timing details). SDATA I/O Data pin for I2C circuitry 5V tolerant DDRC7 OUT "True" Clock of differential pair output. DDRC7 OUT "True" Clock of differential pair output. Tomplementary" Clock of differential pair output. True" Clock of differential pair output.			-	
24 GND PWR Ground pin. 25 GND PWR Ground pin. 26 DDRC9 OUT "Complementary" Clock of differential pair output. 27 DDRT9 OUT "True" Clock of differential pair output. 28 VDD2.5 PWR Power supply, nominal 2.5V 29 DDRT8 OUT "Complementary" Clock of differential pair output. 30 DDRC8 OUT "Complementary" Clock of differential pair output. 31 GND PWR Ground pin. 32 CS_PROG0** 33 RSTEP IN Exnterna pull-down resistor can be set on this pin to program input vs DDR clocks skew. 34 VDD2.5 PWR Power supply, nominal 2.5V 35 RFIX IN Exnterna pull-down resistor can be set on this pin to program input vs DDR clocks skew. 36 CS_PROG1* 37 SDATA I/O Data pin for I2C circuitry 5V tolerant 38 VDD2.5 PWR Power supply, nominal 2.5V 39 DDRT7 OUT "True" Clock of differential pair output. 40 DDRC7 OUT "Complementary" Clock of differential pair output. 41 GND PWR Ground pin. 42 GND PWR Ground pin. 43 DDRC6 OUT "Complementary" Clock of differential pair output. 44 DDRC6 OUT "Complementary" Clock of differential pair output. 45 VDD2.5 PWR Power supply, nominal 2.5V 46 DDRT5 OUT "True" Clock of differential pair output. 47 DDRC5 OUT "True" Clock of differential pair output. 48 DDRT5 OUT "True" Clock of differential pair output. 49 DDRT6 OUT "True" Clock of differential pair output. 40 DDRT6 OUT "True" Clock of differential pair output. 41 DDRT5 OUT "True" Clock of differential pair output. 42 DDRT5 OUT "True" Clock of differential pair output. 44 DDRT5 OUT "True" Clock of differential pair output.				·
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DDRC9 OUT "Complementary" Clock of differential pair output. DDRT9 OUT "True" Clock of differential pair output. PWR Power supply, nominal 2.5V DDRT8 OUT "True" Clock of differential pair output. Complementary" Clock of differential pair output. DDRC8 OUT "Complementary" Clock of differential pair output. CS_PROG0** IN Latch input pin to change Byte 3 bit 5 Coarse Skew Programming default (Pulling this bit high will advance the DDR output vs the input, refer to table 1 for timing details). RSTEP IN Exnterna pull-down resistor can be set on this pin to program input vs DDR clocks skew. PWR Power supply, nominal 2.5V IN Exnterna pull-down resistor can be set on this pin to program input vs DDR clocks skew. CS_PROG1* IN Exnterna pull-down resistor can be set on this pin to program input vs DDR clocks skew. CS_PROG1* IN Exnterna pull-down resistor can be set on this pin to program input vs DDR clocks skew. Latch input pin to change Byte 3 bit 7 Coarse Skew Programming default (Pulling this bit high will advance the DDR output vs the input, refer to table 1 for timing details). DDRT7 OUT "True" Clock of differential pair output. PWR Power supply, nominal 2.5V OUD PWR Ground pin. GND PWR Ground pin. Complementary" Clock of differential pair output. DDRT6 OUT "True" Clock of differential pair output. DDRT6 OUT "True" Clock of differential pair output. DDRT6 OUT "True" Clock of differential pair output. True" Clock of differential pair output. DDRT6 OUT "True" Clock of differential pair output. True" Clock of differential pair output.			_	·
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DDRT8 OUT "True" Clock of differential pair output. OUT "Complementary" Clock of differential pair output. OUT "Complementary" Clock of differential pair output. IN Latch input pin to change Byte 3 bit 5 Coarse Skew Programming default (Pulling this bit high will advance the DDR output vs the input, refer to table 1 for timing details). RSTEP IN Exnterna pull-down resistor can be set on this pin to program input vs DDR clocks skew. PWR Power supply, nominal 2.5V Exnterna pull-down resistor can be set on this pin to program input vs DDR clocks skew. IN Exnterna pull-down resistor can be set on this pin to program input vs DDR clocks skew. CS_PROG1* IN Latch input pin to change Byte 3 bit 7 Coarse Skew Programming default (Pulling this bit high will advance the DDR output vs the input, refer to table 1 for timing details). Data pin for I2C circuitry 5V tolerant VDD2.5 PWR Power supply, nominal 2.5V PWR Power supply, nominal 2.5V OUT "True" Clock of differential pair output. OUT "Complementary" Clock of differential pair output. AUD DDRC7 OUT "Complementary" Clock of differential pair output. OUT "Complementary" Clock of differential pair output. OUT "True" Clock of differential pair output.				• •
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37 SDATA I/O Data pin for I2C circuitry 5V tolerant 38 VDD2.5 PWR Power supply, nominal 2.5V 39 DDRT7 OUT "True" Clock of differential pair output. 40 DDRC7 OUT "Complementary" Clock of differential pair output. 41 GND PWR Ground pin. 42 GND PWR Ground pin. 43 DDRC6 OUT "Complementary" Clock of differential pair output. 44 DDRT6 OUT "True" Clock of differential pair output. 45 VDD2.5 PWR Power supply, nominal 2.5V 46 DDRT5 OUT "True" Clock of differential pair output. 47 DDRC5 OUT "Complementary" Clock of differential pair output.	36		IN	Latch input pin to change Byte 3 bit 7 Coarse Skew Programming default (Pulling this bit high will
39 DDRT7 OUT "True" Clock of differential pair output. 40 DDRC7 OUT "Complementary" Clock of differential pair output. 41 GND PWR Ground pin. 42 GND PWR Ground pin. 43 DDRC6 OUT "Complementary" Clock of differential pair output. 44 DDRT6 OUT "True" Clock of differential pair output. 45 VDD2.5 PWR Power supply, nominal 2.5V 46 DDRT5 OUT "True" Clock of differential pair output. 47 DDRC5 OUT "Complementary" Clock of differential pair output.	37	SDATA	I/O	
39 DDRT7 OUT "True" Clock of differential pair output. 40 DDRC7 OUT "Complementary" Clock of differential pair output. 41 GND PWR Ground pin. 42 GND PWR Ground pin. 43 DDRC6 OUT "Complementary" Clock of differential pair output. 44 DDRT6 OUT "True" Clock of differential pair output. 45 VDD2.5 PWR Power supply, nominal 2.5V 46 DDRT5 OUT "True" Clock of differential pair output. 47 DDRC5 OUT "Complementary" Clock of differential pair output.	38	VDD2.5	PWR	Power supply, nominal 2.5V
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42 GND PWR Ground pin. 43 DDRC6 OUT "Complementary" Clock of differential pair output. 44 DDRT6 OUT "True" Clock of differential pair output. 45 VDD2.5 PWR Power supply, nominal 2.5V 46 DDRT5 OUT "True" Clock of differential pair output. 47 DDRC5 OUT "Complementary" Clock of differential pair output.	40	DDRC7	OUT	"Complementary" Clock of differential pair output.
42 GND PWR Ground pin. 43 DDRC6 OUT "Complementary" Clock of differential pair output. 44 DDRT6 OUT "True" Clock of differential pair output. 45 VDD2.5 PWR Power supply, nominal 2.5V 46 DDRT5 OUT "True" Clock of differential pair output. 47 DDRC5 OUT "Complementary" Clock of differential pair output.	41	GND	PWR	Ground pin.
43 DDRC6 OUT "Complementary" Clock of differential pair output. 44 DDRT6 OUT "True" Clock of differential pair output. 45 VDD2.5 PWR Power supply, nominal 2.5V 46 DDRT5 OUT "True" Clock of differential pair output. 47 DDRC5 OUT "Complementary" Clock of differential pair output.	42		PWR	Ground pin.
44 DDRT6 OUT "True" Clock of differential pair output. 45 VDD2.5 PWR Power supply, nominal 2.5V 46 DDRT5 OUT "True" Clock of differential pair output. 47 DDRC5 OUT "Complementary" Clock of differential pair output.	43		OUT	
45 VDD2.5 PWR Power supply, nominal 2.5V 46 DDRT5 OUT "True" Clock of differential pair output. 47 DDRC5 OUT "Complementary" Clock of differential pair output.	44			
46 DDRT5 OUT "True" Clock of differential pair output. 47 DDRC5 OUT "Complementary" Clock of differential pair output.			_	· ·
47 DDRC5 OUT "Complementary" Clock of differential pair output.			_	
			-	
			_	



Preliminary Product Preview

I²C Table: Reserved Register

BYTE		Affected Pin	Control Function	Туре	Bit Control		
0	Pin#	Name	Control i dilettori	Туре	0	1	PWD
Bit 7	-	-	(reserved)	R/W	-	-	1
Bit 6	-	-	(reserved)	R/W	-	-	1
Bit 5	-	-	(reserved)	R/W	-	-	1
Bit 4	-	-	(reserved)	R/W	-	-	1
Bit 3	-	-	(reserved)	R/W	-	-	1
Bit 2	-	-	(reserved)	R/W	-	-	1
Bit 1	-	-	(reserved)	R/W	-	-	1
Bit 0	-	-	(reserved)	R/W	-	-	1

I²C Table: Fix Delay Control Register

BYTE		Affected Pin	Control Function	Туре	e Bit Control		
1	Pin #	Name	Control i direttori		0	1	PWD
Bit 7	-	-	Fix Delay Polarity Selection	R/W	DDR Outputs Advance	DDR Outputs Delay	Latch
Bit 6	-	-	Fix Delay Enable	R/W	Enable	Bypass	0
Bit 5	-	-	(reserved)	R/W	-	-	1
Bit 4	-	-	(reserved)	R/W	-	-	1
Bit 3	-	-	(reserved)	R/W	-	-	1
Bit 2	-	-	(reserved)	R/W	-	-	1
Bit 1	-	-	(reserved)	R/W	-	-	1
Bit 0	-	-	(reserved)	R/W	-	-	1

I²C Table: Output Drive Strength Control Register

BYTE	Affected Pin		Control Function	Туре	Bit Control		
2	Pin #	Name	Control i dilettori	Type	0	1	PWD
Bit 7	-	-	(reserved)	R/W	-	-	0
Bit 6	•	=	DDR output driver strength	R/W	1X	1.5X	0
Bit 5	-	-	(reserved)	R/W	-	-	0
Bit 4	-	-	(reserved)	R/W	-	-	0
Bit 3	-	-	(reserved)	R/W	-	-	0
Bit 2	-	-	(reserved)	R/W	-	-	0
Bit 1	-	-	(reserved)	R/W	-	-	0
Bit 0	-	-	(reserved)	R/W	-	-	0

I²C Table: Step Delay Control Register

		<u> </u>				
BYTE		Affected Pin	Control Function	Type	Bit Control	
3	Pin #	Name	Control Function	туре	DIL COLLIO	PWD
Bit 7	-	-		R/W	Latch	
Bit 6	-	-	Step Advance Skew Programming	R/W	SEE TABLE 1	0
Bit 5	-	-	for DDR Outputs	R/W	OLL TABLE T	Latch
Bit 4	-	-		R/W		0
Bit 3	-	-		R/W		0
Bit 2	-	-	Step Delay Skew Programming for	R/W	SEE TABLE 2	0
Bit 1	-	-	DDR Outputs	R/W	OLL TABLE 2	0
Bit 0	-	-		R/W		0



Preliminary Product Preview

I²C Table: Step Delay Control Register

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BYTE		Affected Pin	Control Function	Type	Bit Control		
4	Pin #	Name	Control i dilettori	туре	Dit Control	PWD	
Bit 7	-	-		R/W	R/W		
Bit 6	-	-	Step Delay Skew Programming for		SEE TABLE 2	0	
Bit 5	-	-	DDR (8:0) Outputs	R/W	OLL TABLE 2	0	
Bit 4	-	-		R/W		0	
Bit 3	-	-		R/W		0	
Bit 2	-	-	Step Delay Skew Programming for	R/W	SEE TABLE 2	0	
Bit 1	-	-	DDR 9 Outputs	DDR 9 Outputs R/W		0	
Bit 0	-	-		R/W		0	

I²C Table: Output Control Register

BYTE		Affected Pin	Control Function	Туре	Bit Co	ontrol	
5	Pin #	Name	Control i dilettori	Type	0	1	PWD
Bit 7	2, 3	DDRC0, DDRT0	Output Enable	R/W	Stop	Run	1
Bit 6	5, 6	DDRC1, DDRT1	Output Enable	R/W	Stop	Run	1
Bit 5	9, 10	DDRC2, DDRT2	Output Enable	R/W	Stop	Run	1
Bit 4	19, 20	DDRC3, DDRT3	Output Enable	R/W	Stop	Run	1
Bit 3	22, 23	DDRC4, DDRT4	Output Enable	R/W	Stop	Run	1
Bit 2	27,26	DDRC9, DDRT9	Output Enable	R/W	Stop	Run	1
Bit 1	-	-	(reserved)	R/W	-	-	1
Bit 0			(reserved)	R/W	-	-	1

I²C Table: Output Control Register

BYTE	Affected Pin		Control Function	Туре	Bit Control		
6	Pin#	Name	Control 1 direttori	Туре	0	1	PWD
Bit 7	-	-	(reserved)	R/W	-	-	1
Bit 6	-	-	(reserved)	R/W	•	-	1
Bit 5	-	-	(reserved)	R/W	-	-	1
Bit 4	30, 29	DDRC8, DDRT8	Output Enable	R/W	Stop	Run	1
Bit 3	40, 39	DDRC7, DDRT7	Output Enable	R/W	Stop	Run	1
Bit 2	44, 43	DDRC6, DDRT6	Output Enable	R/W	Stop	Run	1
Bit 1	47, 46	DDRC5, DDRT5	Output Enable	R/W	Stop	Run	1
Bit 0	-	-	(reserved)	R/W	-	-	1

I²C Table: Reserved Register

BYTE	Affected Pin		Control Function	Type	Bit Control		
7	Pin #	Name	Control i dilettori	Туре	0	1	PWD
Bit 7	-	-	(reserved)	R/W	-	-	1
Bit 6	-	-	(reserved)	R/W	-	-	1
Bit 5	-	-	(reserved)	R/W	•	-	1
Bit 4	-	-	(reserved)	R/W	•	-	1
Bit 3	-	-	(reserved)	R/W	•	-	1
Bit 2	-	-	(reserved)	R/W	ı	-	1
Bit 1	-	-	(reserved)	R/W	•	-	1
Bit 0	-	•	(reserved)	R/W	ı	•	1



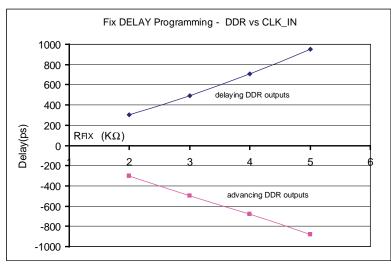


Table 1: Step Advance Skew Programming

1 4010 1	Otop	71010			. og. ammin	Table 1: Otop Advance Okew 1 Togramming											
BIT	Bit7 CSP1	Bit6	Bit5 CSP0	Bit4	R _{STEP} =1K	R _{STEP} =2K	R _{STEP} =3K										
	0	0	0	0	0	0	0										
	0	0	0	1	-200	-250	-350										
	0	0	1	0	-400	-500	-700										
	0	0	1	1	-600	-750	-1050										
	0	1	0	0	-800	-1000	-1400										
	0	1	0	1	-1000	-1250	-1750										
	0	1	1	0	-1200	-1500	-2100										
BYTE 3	0	1	1	1	-1400	-1750	-2450										
DITES	1	0	0	0	-1600	-2000	-2800										
	1	0	0	1	-1800	-2250	-3150										
	1	0	1	0	-2000	-2500	-3500										
	1	0	1	1	(reserved)	(reserved)	(reserved)										
	1	1	0	0	(reserved)	(reserved)	(reserved)										
	1	1	0	1	(reserved)	(reserved)	(reserved)										
	1	1	1	0	(reserved)	(reserved)	(reserved)										
	1	1	1	1	(reserved)	(reserved)	(reserved)										

Table 2: Step Delay Skew Programming

BIT	Bit7/3	Bit6/2	Bit5/1 CSP0	Bit4/0	R _{STEP} =1K	R _{STEP} =2K	R _{STEP} =3K
	0	0	0	0	0	0	0
		_	_	_	-	_	
	0	0	0	1	200	250	350
	0	0	1	0	400	500	700
	0	0	1	1	600	750	1050
	0	1	0	0	800	1000	1400
	0	1	0	1	1000	1250	1750
BYTE 3 BYTE 4	0	1	1	0	1200	1500	2100
	0	1	1	1	1400	1750	2450
	1	0	0	0	1600	2000	2800
	1	0	0	1	1800	2250	3150
	1	0	1	0	2000	2500	3500
	1	0	1	1	(reserved)	(reserved)	(reserved)
	1	1	0	0	(reserved)	(reserved)	(reserved)
	1	1	0	1	(reserved)	(reserved)	(reserved)
	1	1	1	0	(reserved)	(reserved)	(reserved)
	1	1	1	1	(reserved)	(reserved)	(reserved)





Preliminary Product Preview

Absolute Maximum Ratings

Supply Voltage (VDD & AVDD).....--0.5V to 3.6V

Logic Inputs GND -0.5 V to V_{DD} +0.5 V

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input / Supply / Common Output Parameters

 $T_A = 0 - 70$ °C; Supply Voltage $V_{DD} = 2.5 \text{ V} + /-0.2 \text{V}$ (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS		TYP	MAX	UNITS
Input High Current	I _{IH}	$V_I = V_{DD}$ or GND		((/)/	>	mA
Input Low Current	I _{IL}	$V_{I} = V_{DD}$ or GND	(7//		mA
Operating Supply Current	I _{DD2.5}	C _L = 0 pF at 133 MHz		245	300	mA
Operating Supply Current	I _{DDPD}	C _L = 0 pF			200	μΑ
Output High Current	I _{OH}	$V_{DD} = 2.3V$, $V_{OUT} = 1V$	7/~~	-43	-18	mA
Output High Current	I _{OL}	$V_{DD} = 2.3V, V_{OUT} = 1.2V$	26	43		mA
High Impedance Output Current	l _{oz}	$V_{DD} = 2.7V$, $V_{OUT} = V_{DD}$ or GND			±10	μΑ
Input Clamp Voltage	V _{IK}	lin = -18 mA;				V
Lligh lovel Output Voltage	M	V _{DD} = min to max, I _{OH} = -1mA	2.1	2.42		V
High-level Output Voltage	V _{OH}	$V_{DD} = 2.3V, I_{OH} = -12mA$		1.87		V
Low-level Output Voltage	VoL	V_{DD} = min to max, I_{OH} = 1mA		0.04	0.1	V
		$V_{DD} = 2.3V$, $I_{OH} = 12mA$	<i>></i> ′	0.35	0.6	V
Input Capacitance ¹	C _{IN}	$V_I = V_{DD}$ or GND				pF
Output Capacitance ¹	C _{OUT}	$V_I = V_{DD}$ or GND		3		pF

^{1.} Guaranteed by design, not 100% tested in production.

Recommended Operating Conditions

 $T_A = 0 - 70$ °C; Supply Voltage AV_{DD}, $V_{DD} = 2.5 \text{ V} + /-0.2 \text{V}$ (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Analog / Core Supply Voltage	AV _{DD}		2.3	2.5	2.7	V
Input Voltage Level	V_{IN}					V
Output Differential Pair Crossing Voltage	V _{oc}		1.05	1.25	1.45	V



Preliminary Product Preview

Timing Requirements

 $T_A = 0 - 70^{\circ}C$; Supply Voltage AV_{DD} , $V_{DD} = 2.5 \text{ V} + /-0.2 \text{V}$ (unless otherwise stated)

	0 00,	DD (
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Clock Frequency ¹	freq _{op}		66	>	170	MHz
Input Clock Duty Cycle ¹	d_{tin}		40	2/>	60	%
Clock Stabilization ¹	t _{STAB}	from $V_{DD} = 2.5V$ to 1% target frequency			100	μs

^{1.} Guaranteed by design, not 100% tested in production.

Switching Characteristics

 $T_A = 0 - 70$ °C; Supply Voltage $V_{DD} = 2.5 \text{ V} + /-0.2 \text{V}$ (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Absolute Jitter ¹	(T)	66 MHz	\Diamond		120	ps
Absolute Sitter	t _{jabs}	100 / 125 / 133 / 167 MHz		\rightarrow	75	ρS
Cycle to cycle Jitter ^{1,2}	+ ^	66 MHz		50	110	nc
Cycle to cycle Jitter	t _{c-c}	100 / 125 / 133 / 167 MHz		35	65	ps
Phase Error ¹	t _{pe}	See programmable information				
Output to output Skew ¹	T _{skew}					
Low-to-high level		CLV (N) to any output Local 1200				
Propagation Delay Time,	t _{PLH}	CLK_IN to any output, Load = 120Ω	4	4.5	6	ns
Bypass Mode ¹	(0)	12pF	27 ₁			
Duty Cycle (differential)1.3		no loads, 66 MHz to 167 MHz	40	50	51	%
Duty Cycle (differential) ^{1,3}	Dc	TIO loads, 66 WINZ 10 167 WINZ	49 50		31	70
Die a Time Fall Time 1		Single-ended 20 - 80 %; Load = 120Ω +	450	EEO	050	no
Rise Time, Fall Time ¹	t_{R}, t_{F}	12 pF	450	550	950	ps

- 1. Guaranteed by design, not 100% tested in production.
- 2. Refers to transistion on non-inverting period.
- 3. While the pulse skew is almost constant over frequency, the duty cycle error increases at higher frequencies. This is due to the formula: duty cycle = t_{WH} / t_{C} , where the cycle time (t_{C}) decreases as the frequency increases.



Preliminary Product Preview

General I²C serial interface information

The information in this section assumes familiarity with I^2C programming. For more information, contact ICS for an I^2C programming application note.

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D4 (H)
- ICS clock will *acknowledge*
- Controller (host) sends a dummy command code
- ICS clock will acknowledge
- Controller (host) sends a dummy byte count
- ICS clock will acknowledge
- Controller (host) starts sending first byte (Byte 0) through byte 6
- ICS clock will *acknowledge* each byte *one at a time*.
- Controller (host) sends a Stop bit

How to Write:					
Controller (Host)	ICS (Slave/Receiver)				
Start Bit					
Address					
D4 _(H)					
	ACK				
Dummy Command Code					
	ACK				
Dummy Byte Count					
	ACK				
Byte 0					
	ACK				
Byte 1					
	ACK				
Byte 2					
	ACK				
Byte 3					
	ACK				
Byte 4					
	ACK				
Byte 5					
	ACK				
Byte 6					
	ACK				
Stop Bit					

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the read address D5 (H)
- ICS clock will acknowledge
- ICS clock will send the *byte count*
- Controller (host) acknowledges
- ICS clock sends first byte (Byte 0) through byte 6
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a stop bit

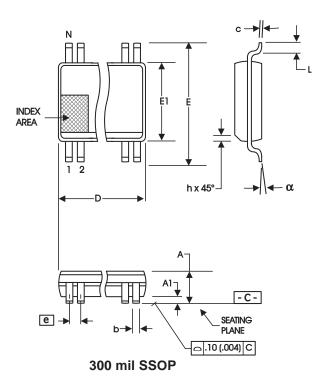
How to Read:					
Controller (Host)	ICS (Slave/Receiver)				
Start Bit					
Address					
D5 _(H)					
	ACK				
	Byte Count				
ACK					
	Byte 0				
ACK					
	Byte 1				
ACK					
	Byte 2				
ACK					
	Byte 3				
ACK					
	Byte 4				
ACK					
	Byte 5				
ACK					
	Byte 6				
ACK					
Stop Bit					

Notes:

- 1. The ICS clock generator is a slave/receiver, I²C component. It can read back the data stored in the latches for verification. **Read-Back will support Intel PIIX4 "Block-Read" protocol**.
- 2. The data transfer rate supported by this clock generator is 100K bits/sec or less (standard mode)
- 3. The input is operating at 3.3V logic levels.
- 4. The data byte format is 8 bit bytes.
- 5. To simplify the clock generator I²C interface, the protocol is set to use only "**Block-Writes**" from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The Command code and Byte count shown above must be sent, but the data is ignored for those two bytes. The data is loaded until a Stop sequence is issued.
- 6. At power-on, all registers are set to a default condition, as shown.



Preliminary Product Preview



SYMBOL	In Millin		In Ind COM		
	COMMON DIMENSIONS		DIMENSIONS		
	MIN	MAX	MIN	MAX	
Α	2.413	2.794	.095	.110	
A1	0.203	0.406	.008	.016	
b	0.203	0.343	.008	.0135	
С	0.127	0.254	.005	.010	
D	SEE VAR	IATIONS	SEE VAR	E VARIATIONS	
Е	10.033	10.668	.395	.420	
E1	7.391	7.595	.291	.299	
е	0.635	BASIC	0.025	BASIC	
h	0.381	0.635	.015	.025	
L	0.508	1.016	.020	.040	
N	SEE VAR	IATIONS	SEE VARIATIONS		
а	0°	8°	0° 8°		

VARIATIONS

N	D m	nm.	D (inch)		
14	MIN	MAX	MIN	MAX	
48	15.748	16.002	.620	.630	
			JEDEC MO-118	6/1/00	

JEDEC MO-118 6/1/00 DOC# 10-0034 REVB

Ordering Information

ICS93727_⊻F-T

