Integrated Circuit Systems, Inc.

ICS93727
Preliminary Product Preview

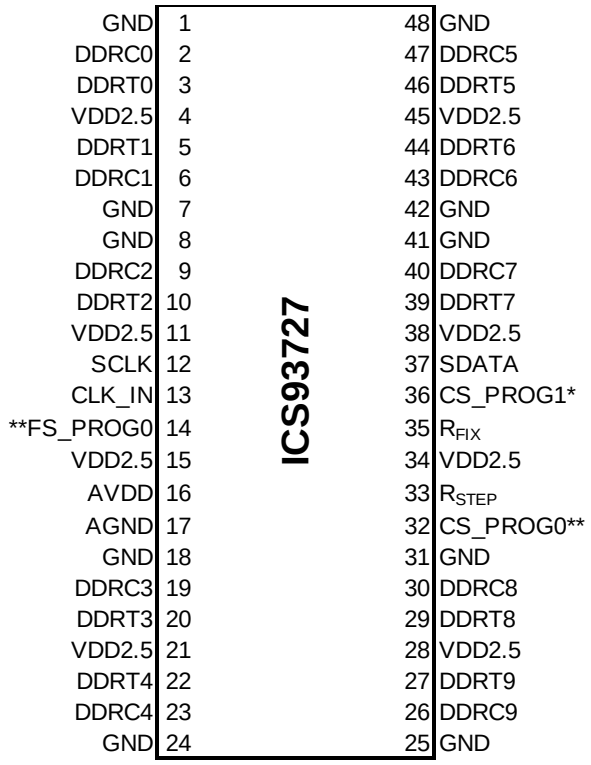
DDR Phase Lock Loop Zero Delay Clock Buffer (patent pending)

Recommended Application:
DDR Zero Delay Clock Buffer

Product Description/Features:
- Low skew, low jitter PLL clock driver
- I^2C for functional and output control
- Spread Spectrum tolerant inputs
- Input to output skew control (R_{FIX}, R_{STEP}) (patent pending)
- Northbridge reference clock for output delay control

Switching Characteristics:
- PEAK - PEAK jitter (66MHz): <120ps
- PEAK - PEAK jitter (>100MHz): <75ps
- CYCLE - CYCLE jitter (66MHz):<120ps
- CYCLE - CYCLE jitter (>100MHz):<65ps
- OUTPUT - OUTPUT skew: <100ps
- Output Rise and Fall Time: 450ps - 950ps
- DUTY CYCLE: 49% - 51%

Pin Configuration



48-SSOP

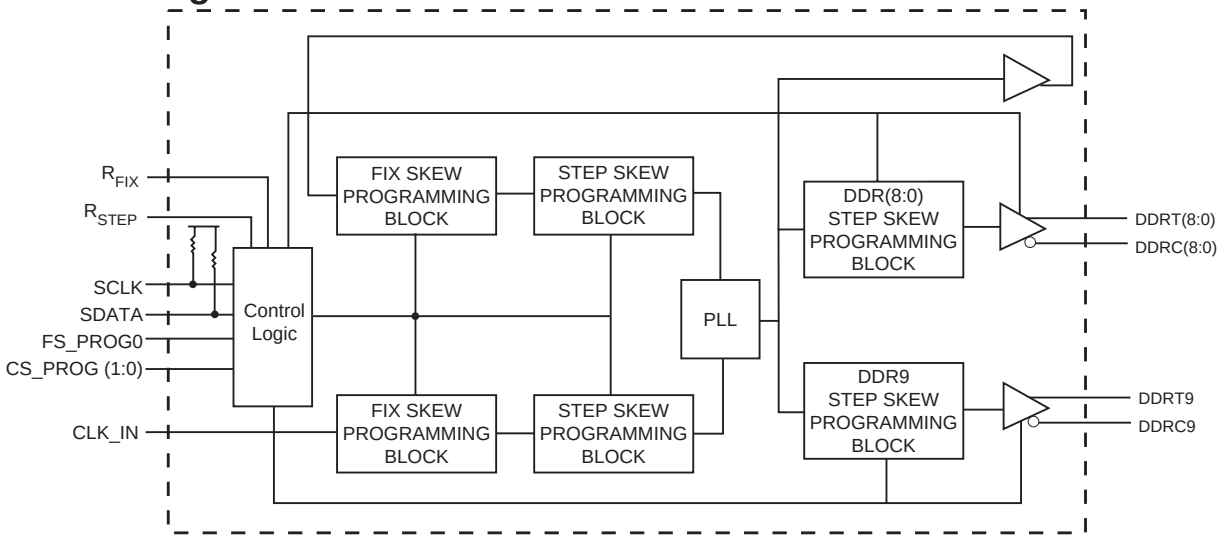
* Internal Pull-Up Resistor

** Internal Pull-Down Resistor

Functionality

INPUTS		OUTPUTS			PLL State
AVDD	CLKIN	DDRT	DDRC	FB	
2.5V (NOM)	AVERAGE VOLTAGE > 0.4V	IN PHASE WITH CLKIN			ON
2.5V (NOM)	AVERAGE VOLTAGE < 0.4V	HI Z	HI Z	HI Z	OFF
GND	L	L	H	L	BYPASSED/OFF
GND	H	H	L	H	BYPASSED/OFF

Block Diagram



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Pin Descriptions

PIN #	PIN NAME	PIN TYPE	DESCRIPTION
1	GND	PWR	Ground pin.
2	DDRC0	OUT	"Complementary" Clock of differential pair output.
3	DDRT0	OUT	"True" Clock of differential pair output.
4	VDD2.5	PWR	Power supply, nominal 2.5V
5	DDRT1	OUT	"True" Clock of differential pair output.
6	DDRC1	OUT	"Complementary" Clock of differential pair output.
7	GND	PWR	Ground pin.
8	GND	PWR	Ground pin.
9	DDRC2	OUT	"Complementary" Clock of differential pair output.
10	DDRT2	OUT	"True" Clock of differential pair output.
11	VDD2.5	PWR	Power supply, nominal 2.5V
12	SCLK	IN	Clock pin of I2C circuitry 5V tolerant
13	CLK_IN	IN	Reference clock input.
14	**FS_PROG0	IN	Latch input pin to change Byte 1 bit 7 Fine Skew Programming default polarity (Pulling this bit low will set DDR output to be advance vs the input).
15	VDD2.5	PWR	Power supply, nominal 2.5V
16	AVDD	PWR	2.5V Analog Power pin for Core PLL
17	AGND	PWR	Analog Ground pin for Core PLL
18	GND	PWR	Ground pin.
19	DDRC3	OUT	"Complementary" Clock of differential pair output.
20	DDRT3	OUT	"True" Clock of differential pair output.
21	VDD2.5	PWR	Power supply, nominal 2.5V
22	DDRT4	OUT	"True" Clock of differential pair output.
23	DDRC4	OUT	"Complementary" Clock of differential pair output.
24	GND	PWR	Ground pin.
25	GND	PWR	Ground pin.
26	DDRC9	OUT	"Complementary" Clock of differential pair output.
27	DDRT9	OUT	"True" Clock of differential pair output.
28	VDD2.5	PWR	Power supply, nominal 2.5V
29	DDRT8	OUT	"True" Clock of differential pair output.
30	DDRC8	OUT	"Complementary" Clock of differential pair output.
31	GND	PWR	Ground pin.
32	CS_PROG0**	IN	Latch input pin to change Byte 3 bit 5 Coarse Skew Programming default (Pulling this bit high will advance the DDR output vs the input, refer to table 1 for timing details).
33	RSTEP	IN	Exnterna pull-down resistor can be set on this pin to program input vs DDR clocks skew.
34	VDD2.5	PWR	Power supply, nominal 2.5V
35	RFIX	IN	Exnterna pull-down resistor can be set on this pin to program input vs DDR clocks skew.
36	CS_PROG1*	IN	Latch input pin to change Byte 3 bit 7 Coarse Skew Programming default (Pulling this bit high will advance the DDR output vs the input, refer to table 1 for timing details).
37	SDATA	I/O	Data pin for I2C circuitry 5V tolerant
38	VDD2.5	PWR	Power supply, nominal 2.5V
39	DDRT7	OUT	"True" Clock of differential pair output.
40	DDRC7	OUT	"Complementary" Clock of differential pair output.
41	GND	PWR	Ground pin.
42	GND	PWR	Ground pin.
43	DDRC6	OUT	"Complementary" Clock of differential pair output.
44	DDRT6	OUT	"True" Clock of differential pair output.
45	VDD2.5	PWR	Power supply, nominal 2.5V
46	DDRT5	OUT	"True" Clock of differential pair output.
47	DDRC5	OUT	"Complementary" Clock of differential pair output.
48	GND	PWR	Ground pin.

I²C Table: Reserved Register

BYTE 0	Affected Pin		Control Function	Type	Bit Control		
	Pin #	Name			0	1	PWD
Bit 7	-	-	(reserved)	R/W	-	-	1
Bit 6	-	-	(reserved)	R/W	-	-	1
Bit 5	-	-	(reserved)	R/W	-	-	1
Bit 4	-	-	(reserved)	R/W	-	-	1
Bit 3	-	-	(reserved)	R/W	-	-	1
Bit 2	-	-	(reserved)	R/W	-	-	1
Bit 1	-	-	(reserved)	R/W	-	-	1
Bit 0	-	-	(reserved)	R/W	-	-	1

I²C Table: Fix Delay Control Register

BYTE 1	Affected Pin		Control Function	Type	Bit Control		
	Pin #	Name			0	1	PWD
Bit 7	-	-	Fix Delay Polarity Selection	R/W	DDR Outputs Advance	DDR Outputs Delay	Latch
Bit 6	-	-	Fix Delay Enable	R/W	Enable	Bypass	0
Bit 5	-	-	(reserved)	R/W	-	-	1
Bit 4	-	-	(reserved)	R/W	-	-	1
Bit 3	-	-	(reserved)	R/W	-	-	1
Bit 2	-	-	(reserved)	R/W	-	-	1
Bit 1	-	-	(reserved)	R/W	-	-	1
Bit 0	-	-	(reserved)	R/W	-	-	1

I²C Table: Output Drive Strength Control Register

BYTE 2	Affected Pin		Control Function	Type	Bit Control		
	Pin #	Name			0	1	PWD
Bit 7	-	-	(reserved)	R/W	-	-	0
Bit 6	-	-	DDR output driver strength	R/W	1X	1.5X	0
Bit 5	-	-	(reserved)	R/W	-	-	0
Bit 4	-	-	(reserved)	R/W	-	-	0
Bit 3	-	-	(reserved)	R/W	-	-	0
Bit 2	-	-	(reserved)	R/W	-	-	0
Bit 1	-	-	(reserved)	R/W	-	-	0
Bit 0	-	-	(reserved)	R/W	-	-	0

I²C Table: Step Delay Control Register

BYTE 3	Affected Pin		Control Function	Type	Bit Control	
	Pin #	Name				PWD
Bit 7	-	-	Step Advance Skew Programming for DDR Outputs	R/W	SEE TABLE 1	Latch
Bit 6	-	-		R/W		0
Bit 5	-	-		R/W		Latch
Bit 4	-	-		R/W		0
Bit 3	-	-	Step Delay Skew Programming for DDR Outputs	R/W	SEE TABLE 2	0
Bit 2	-	-		R/W		0
Bit 1	-	-		R/W		0
Bit 0	-	-		R/W		0

I²C Table: Step Delay Control Register

BYTE 4	Affected Pin		Control Function	Type	Bit Control	
	Pin #	Name				PWD
Bit 7	-	-	Step Delay Skew Programming for DDR (8:0) Outputs	R/W	SEE TABLE 2	0
Bit 6	-	-		R/W		0
Bit 5	-	-		R/W		0
Bit 4	-	-		R/W		0
Bit 3	-	-	Step Delay Skew Programming for DDR 9 Outputs	R/W	SEE TABLE 2	0
Bit 2	-	-		R/W		0
Bit 1	-	-		R/W		0
Bit 0	-	-		R/W		0

I²C Table: Output Control Register

BYTE 5	Affected Pin		Control Function	Type	Bit Control		
	Pin #	Name			0	1	PWD
Bit 7	2, 3	DDRC0, DDRT0	Output Enable	R/W	Stop	Run	1
Bit 6	5, 6	DDRC1, DDRT1	Output Enable	R/W	Stop	Run	1
Bit 5	9, 10	DDRC2, DDRT2	Output Enable	R/W	Stop	Run	1
Bit 4	19, 20	DDRC3, DDRT3	Output Enable	R/W	Stop	Run	1
Bit 3	22, 23	DDRC4, DDRT4	Output Enable	R/W	Stop	Run	1
Bit 2	27,26	DDRC9, DDRT9	Output Enable	R/W	Stop	Run	1
Bit 1	-	-	(reserved)	R/W	-	-	1
Bit 0	-	-	(reserved)	R/W	-	-	1

I²C Table: Output Control Register

BYTE 6	Affected Pin		Control Function	Type	Bit Control		
	Pin #	Name			0	1	PWD
Bit 7	-	-	(reserved)	R/W	-	-	1
Bit 6	-	-	(reserved)	R/W	-	-	1
Bit 5	-	-	(reserved)	R/W	-	-	1
Bit 4	30, 29	DDRC8, DDRT8	Output Enable	R/W	Stop	Run	1
Bit 3	40, 39	DDRC7, DDRT7	Output Enable	R/W	Stop	Run	1
Bit 2	44, 43	DDRC6, DDRT6	Output Enable	R/W	Stop	Run	1
Bit 1	47, 46	DDRC5, DDRT5	Output Enable	R/W	Stop	Run	1
Bit 0	-	-	(reserved)	R/W	-	-	1

I²C Table: Reserved Register

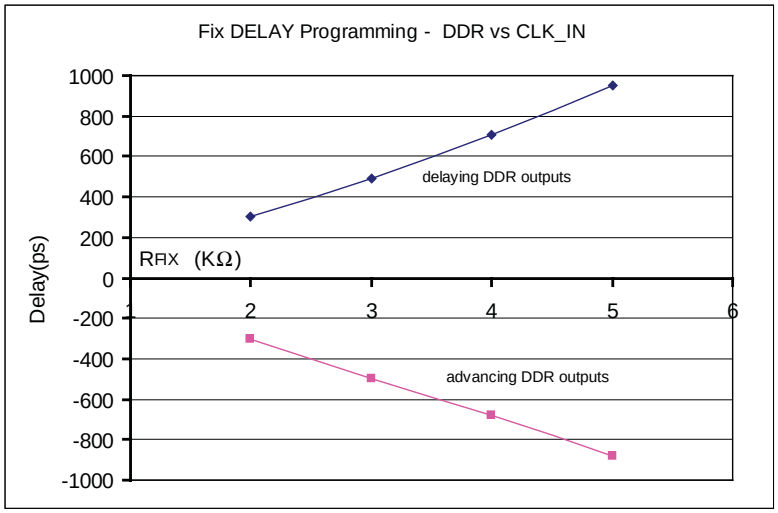
BYTE 7	Affected Pin		Control Function	Type	Bit Control		
	Pin #	Name			0	1	PWD
Bit 7	-	-	(reserved)	R/W	-	-	1
Bit 6	-	-	(reserved)	R/W	-	-	1
Bit 5	-	-	(reserved)	R/W	-	-	1
Bit 4	-	-	(reserved)	R/W	-	-	1
Bit 3	-	-	(reserved)	R/W	-	-	1
Bit 2	-	-	(reserved)	R/W	-	-	1
Bit 1	-	-	(reserved)	R/W	-	-	1
Bit 0	-	-	(reserved)	R/W	-	-	1

Table 1: Step Advance Skew Programming

BIT	Bit7 / CSP1	Bit6	Bit5 / CSP0	Bit4	R_{STEP} =1K	R_{STEP} =2K	R_{STEP} =3K
BYTE 3	0	0	0	0	0	0	0
	0	0	0	1	-200	-250	-350
	0	0	1	0	-400	-500	-700
	0	0	1	1	-600	-750	-1050
	0	1	0	0	-800	-1000	-1400
	0	1	0	1	-1000	-1250	-1750
	0	1	1	0	-1200	-1500	-2100
	0	1	1	1	-1400	-1750	-2450
	1	0	0	0	-1600	-2000	-2800
	1	0	0	1	-1800	-2250	-3150
	1	0	1	0	-2000	-2500	-3500
	1	0	1	1	(reserved)	(reserved)	(reserved)
	1	1	0	0	(reserved)	(reserved)	(reserved)
	1	1	0	1	(reserved)	(reserved)	(reserved)
	1	1	1	0	(reserved)	(reserved)	(reserved)
	1	1	1	1	(reserved)	(reserved)	(reserved)

Table 2: Step Delay Skew Programming

BIT	Bit7/3 / CSP1	Bit6/2	Bit5/1 / CSP0	Bit4/0	R_{STEP} =1K	R_{STEP} =2K	R_{STEP} =3K
BYTE 3 BYTE 4	0	0	0	0	0	0	0
	0	0	0	1	200	250	350
	0	0	1	0	400	500	700
	0	0	1	1	600	750	1050
	0	1	0	0	800	1000	1400
	0	1	0	1	1000	1250	1750
	0	1	1	0	1200	1500	2100
	0	1	1	1	1400	1750	2450
	1	0	0	0	1600	2000	2800
	1	0	0	1	1800	2250	3150
	1	0	1	0	2000	2500	3500
	1	0	1	1	(reserved)	(reserved)	(reserved)
	1	1	0	0	(reserved)	(reserved)	(reserved)
	1	1	0	1	(reserved)	(reserved)	(reserved)
	1	1	1	0	(reserved)	(reserved)	(reserved)
	1	1	1	1	(reserved)	(reserved)	(reserved)



Absolute Maximum Ratings

Supply Voltage (VDD & AVDD) . . . . . -0.5V to 3.6V
Logic Inputs . . . . . GND –0.5 V to V_{DD} +0.5 V
Ambient Operating Temperature . . . . . 0°C to +85°C
Storage Temperature . . . . . –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input / Supply / Common Output Parameters

T_A = 0 - 70°C; Supply Voltage V_{DD} = 2.5 V +/-0.2V (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Current	I_{IH}	$V_I = V_{DD}$ or GND				mA
Input Low Current	I_{IL}	$V_I = V_{DD}$ or GND				mA
Operating Supply Current	$I_{DD2.5}$	C_L = 0 pF at 133 MHz		245	300	mA
	I_{DDPD}	C_L = 0 pF			200	µA
Output High Current	I_{OH}	V_{DD} = 2.3V, V_{OUT} = 1V		-43	-18	mA
Output High Current	I_{OL}	V_{DD} = 2.3V, V_{OUT} = 1.2V	26	43		mA
High Impedance Output Current	I_{OZ}	V_{DD} = 2.7V, $V_{OUT} = V_{DD}$ or GND			±10	µA
Input Clamp Voltage	V_{IK}	Iin = -18 mA;				V
High-level Output Voltage	V_{OH}	V_{DD} = min to max, I_{OH} = -1mA	2.1	2.42		V
		V_{DD} = 2.3V, I_{OH} = -12mA		1.87		V
Low-level Output Voltage	V_{OL}	V_{DD} = min to max, I_{OH} = 1mA		0.04	0.1	V
		V_{DD} = 2.3V, I_{OH} = 12mA		0.35	0.6	V
Input Capacitance[1]	C_{IN}	$V_I = V_{DD}$ or GND				pF
Output Capacitance[1]	C_{OUT}	$V_I = V_{DD}$ or GND		3		pF

1. Guaranteed by design, not 100% tested in production.

Recommended Operating Conditions

T_A = 0 - 70°C; Supply Voltage AV_{DD}, V_{DD} = 2.5 V +/-0.2V (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Analog / Core Supply Voltage	AV_{DD}		2.3	2.5	2.7	V
Input Voltage Level	V_{IN}					V
Output Differential Pair Crossing Voltage	V_{OC}		1.05	1.25	1.45	V

Timing Requirements

T_A = 0 - 70°C; Supply Voltage AV_{DD}, V_{DD} = 2.5 V +/-0.2V (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Clock Frequency[1]	$freq_{op}$		66		170	MHz
Input Clock Duty Cycle[1]	d_{tin}		40		60	%
Clock Stabilization[1]	t_{STAB}	from V_{DD} = 2.5V to 1% target frequency			100	µs

1. Guaranteed by design, not 100% tested in production.

Switching Characteristics

T_A = 0 - 70°C; Supply Voltage V_{DD} = 2.5 V +/-0.2V (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Absolute Jitter[1]	t_{jabs}	66 MHz			120	ps
		100 / 125 / 133 / 167 MHz			75	
Cycle to cycle Jitter[1,2]	t_{c-c}	66 MHz		50	110	ps
		100 / 125 / 133 / 167 MHz		35	65	
Phase Error[1]	t_{pe}	See programmable information				
Output to output Skew[1]	T_{skew}					
Low-to-high level Propagation Delay Time, Bypass Mode[1]	t_{PLH}	CLK_IN to any output, Load = 120Ω 12pF	4	4.5	6	ns
Duty Cycle (differential)[1,3]	D_C	no loads, 66 MHz to 167 MHz	49	50	51	%
Rise Time, Fall Time[1]	t_R, t_F	Single-ended 20 - 80 %; Load = 120Ω + 12 pF	450	550	950	ps

1. Guaranteed by design, not 100% tested in production.
2. Refers to transistion on non-inverting period.
3. While the pulse skew is almost constant over frequency, the duty cycle error increases at higher frequencies. This is due to the formula: duty cycle = t_{wH} / t_C, where the cycle time (t_C) decreases as the frequency increases.

General I^2C serial interface information

The information in this section assumes familiarity with I^2C programming.
For more information, contact ICS for an I^2C programming application note.

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address $D4_{(H)}$
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy command code
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy byte count
- ICS clock will ***acknowledge***
- Controller (host) starts sending first byte (Byte 0) through byte 6
- ICS clock will ***acknowledge*** each byte ***one at a time***.
- Controller (host) sends a Stop bit

How to Write:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address $D4_{(H)}$	
	ACK
Dummy Command Code	
	ACK
Dummy Byte Count	
	ACK
Byte 0	
	ACK
Byte 1	
	ACK
Byte 2	
	ACK
Byte 3	
	ACK
Byte 4	
	ACK
Byte 5	
	ACK
Byte 6	
	ACK
Stop Bit	

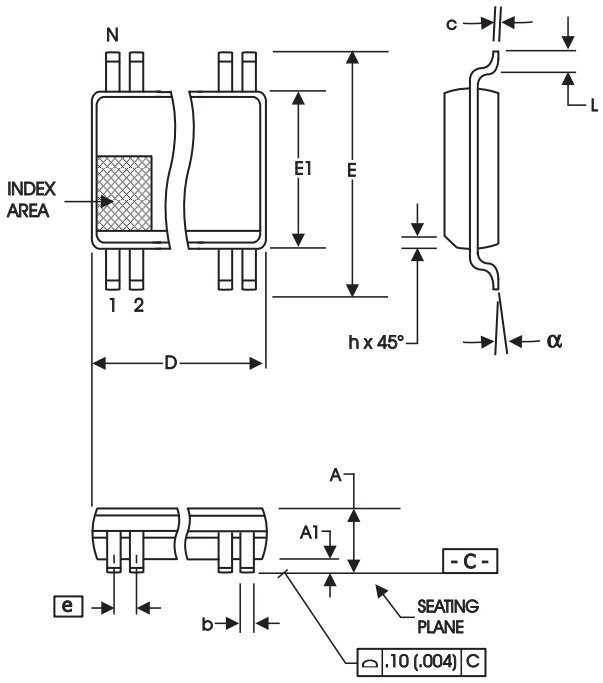
How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the read address $D5_{(H)}$
- ICS clock will ***acknowledge***
- ICS clock will send the ***byte count***
- Controller (host) acknowledges
- ICS clock sends first byte ***(Byte 0) through byte 6***
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a stop bit

How to Read:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address $D5_{(H)}$	
	ACK
	Byte Count
ACK	
	Byte 0
ACK	
	Byte 1
ACK	
	Byte 2
ACK	
	Byte 3
ACK	
	Byte 4
ACK	
	Byte 5
ACK	
	Byte 6
ACK	
Stop Bit	

Notes:

1. The ICS clock generator is a slave/receiver, I^2C component. It can read back the data stored in the latches for verification. **Read-Back will support Intel PIIX4 "Block-Read" protocol**.
2. The data transfer rate supported by this clock generator is 100K bits/sec or less (standard mode)
3. The input is operating at 3.3V logic levels.
4. The data byte format is 8 bit bytes.
5. To simplify the clock generator I^2C interface, the protocol is set to use only "**Block-Writes**" from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The Command code and Byte count shown above must be sent, but the data is ignored for those two bytes. The data is loaded until a Stop sequence is issued.
6. At power-on, all registers are set to a default condition, as shown.



300 mil SSOP

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	2.413	2.794	.095	.110
A1	0.203	0.406	.008	.016
b	0.203	0.343	.008	.0135
c	0.127	0.254	.005	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	10.033	10.668	.395	.420
E1	7.391	7.595	.291	.299
e	0.635 BASIC		0.025 BASIC	
h	0.381	0.635	.015	.025
L	0.508	1.016	.020	.040
N	SEE VARIATIONS		SEE VARIATIONS	
a	0°	8°	0°	8°

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
48	15.748	16.002	.620	.630

JEDEC MO-118 6/1/00
DOC# 10-0034 REVB

Ordering Information

ICS93727yF-T

Example:

ICS XXXX y F - PPP - T

- **Designation for tape and reel packaging**
- **Pattern Number (2 or 3 digit number for parts with ROM code patterns)**
- **Package Type**
  F = SSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type (consists of 3 or 4 digit numbers)**
- **Prefix**
  ICS, AV = Standard Device

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