Q High-Speed CMOS 512 x 9, 1K x 9 FIFO Buffer Memories

QS7201
QS7202

2

FEATURES

- 12-ns flag and data access times
- Fully asynchronous read and write
- Zero fall-through time
- Expandable in depth with no speed loss
- TTL compatible input and output levels

- Low power with industry-standard pinouts
- Retransmit capability
- Dual-port RAM-based cell technology
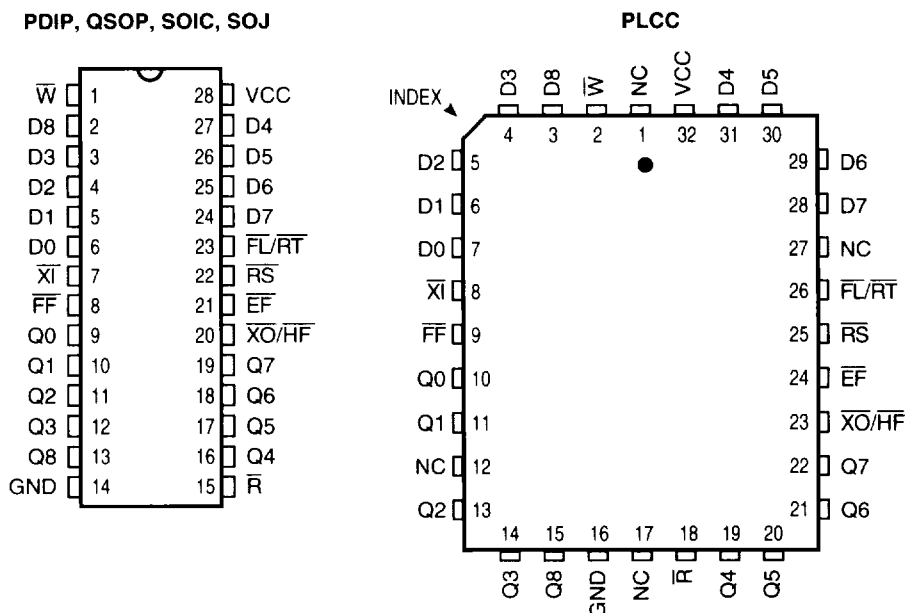- Available in PDIP, SOIC, SOJ, PLCC, and QSOP

DESCRIPTION

The QS7201 and QS7202 are 512 x 9 and 1K x 9 FIFOs, respectively. These FIFOs use a dual-port RAM-based architecture and have independent read and write pointers. This allows high speed with zero fall-through time. The read and write pointers are incremented on the rising edges of the read and write lines. The flag circuitry is based on a patented high-speed design, giving precise half-full, full, and empty conditions. These flags also prevent the FIFO from being written into when full or being read from when empty. These FIFOs are easily cascadable to any depth and expandable to any width without any speed penalty. Retransmit resets the read pointer to memory location zero and is useful for data communications, digital filtering, and video line-doubling applications.

FIGURE 1. FUNCTIONAL BLOCK DIAGRAM
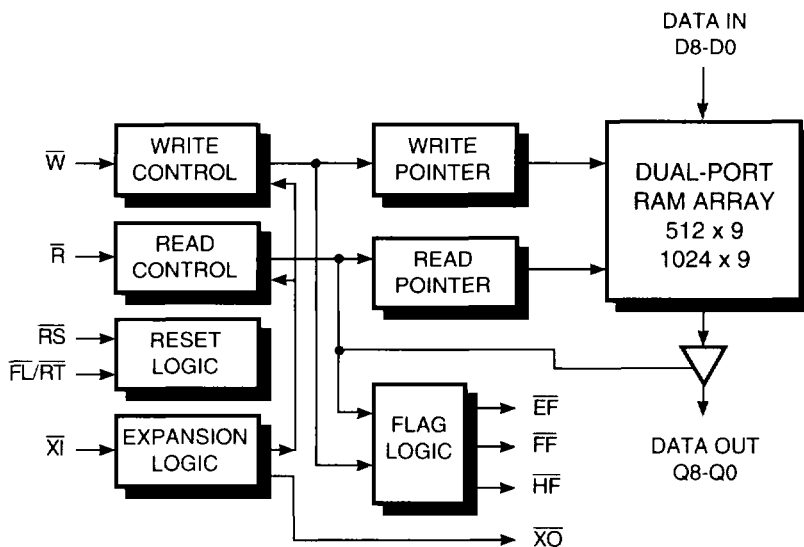
Note: $\overline{XO}$ and $\overline{HF}$ share the same pin, so the Half-Full flag is available only in standalone, not depth-expansion mode.

FIGURE 2. PINOUTS (All pins top view)

PDIP, QSOP, SOIC, SOJ

$\overline{W}$	1		28	VCC
D8	2		27	D4
D3	3		26	D5
D2	4		25	D6
D1	5		24	D7
D0	6		23	$\overline{FL/RT}$
$\overline{XI}$	7		22	$\overline{RS}$
$\overline{FF}$	8		21	$\overline{EF}$
Q0	9		20	$\overline{XO/HF}$
Q1	10		19	Q7
Q2	11		18	Q6
Q3	12		17	Q5
Q8	13		16	Q4
GND	14		15	$\overline{R}$

PLCC

PIN DESCRIPTIONS

Name	I/O	Description
Di	I	Data Inputs
Qi	O	Data Outputs
$\overline{R}$	I	Read Clock
$\overline{W}$	I	Write Clock
$\overline{EF}$	O	Empty Flag
$\overline{FF}$	O	Full Flag
$\overline{RS}$	I	Reset
$\overline{FL/RT}$	I	First Load/Retransmit
$\overline{XI}$	I	Expansion Clock In
$\overline{XO/HF}$	O	Expansion Clock Out/ Half-Full Flag

QUALITY SEMICONDUCTOR, INC.

OPERATIONAL DESCRIPTION AND APPLICATION INFORMATION

The QS7201 and QS7202 are 512 x 9 and 1K x 9 FIFOs, respectively. These FIFOs use a dual-port RAM-based architecture and have independent read and write pointers. This allows high speed with zero fall-through time. The write line causes data to be written into the FIFO. The read line causes data to be read from the FIFO. The read line also activates the three-state outputs to present the read data. The read and write pointers are incremented on the rising edges of the read and write lines. The flag circuitry is based on a reliable sequential design giving precise half-full, full, and empty conditions. These flags also prevent the FIFO from being written into when full or being read from when empty. Depth-expansion pins are provided which allow these FIFOs to be expanded in depth without speed penalty. Retransmit capability is provided. Activating the retransmit pin resets the read pointer to zero and is useful for data communications and digital filtering applications.

2

SIGNAL DESCRIPTION

DATA INPUTS

D8-D0
The Data In lines D8 to D0 provide data to be written into the FIFO.
Note: Unused inputs must be tied to Vcc or GND.

CONTROL INPUTS

Reset ($\overline{RS}$)
The reset input resets the read and write pointers and the flags to zero. The FIFO must be reset at power-up to ensure proper operation of the pointers and flags. This is done by asserting the reset line to a LOW state, which causes the FIFO flags to be set to empty. This causes the Empty flag to be asserted and the Full and Half-Full flags to be deasserted. Read and write lines must be HIGH for t_{RSS} before and t_{RSR} after the rising edge of the reset signal for a valid reset operation.

Write ($\overline{W}$)
The write line causes data to be written into the FIFO. A write cycle is initiated by the falling edge of the write signal. A write will occur if the full flag was not asserted, indicative of at least one empty location in the FIFO. Data is stored in the FIFO on the rising edge of the write signal using the data setup and hold times specified. Data is stored in a sequential manner in the FIFO, and the read and write operations can be asynchronous. The falling edge of the write signal asserts the Half-Full and Full flags when the next word after half-full is written and when the last word has been written, respectively. The rising edge of the write line de-asserts the Empty flag when the first write is performed after an empty or reset condition. When the Full flag is asserted, subsequent writes are blocked. The user can apply a write pulse after the full condition is deasserted.

Read ($\overline{R}$)
The read signal causes data to be read from the FIFO. A read cycle is initiated by the falling edge of the read signal. A read is performed if the Empty flag is not asserted, indicative of at least one word being present in the FIFO. The data is accessed on a first-in-first-out basis asynchronous to the write operations. After the read control is deasserted, the data outputs go from a valid state into high impedance. The outputs remain in high impedance until the next read cycle. When all the data is read on the last read cycle, the Empty flag is asserted, and will inhibit any subsequent reads. The outputs will be in high impedance for subsequent read operations until a write occurs that deasserts the Empty flag, allowing a read cycle to begin. The outputs may also be in high impedance when the FIFOs are cascaded in depth. In this case, only the active FIFO asserts data, and the other FIFO data outputs are in high impedance. The falling edge of the read signal will set the Empty flag during the read of the last word in the FIFO. The rising edge of the read signal will deassert the Half-Full and the Full flags when the FIFO has reached half-full and when the FIFO is full, respectively.

First Load/Retransmit ($\overline{FL}/\overline{RT}$)

This is a dual-purpose input. In the depth-expansion mode, this pin indicates the first FIFO device that will be loaded or read from after a reset operation. In the standalone or width-expansion mode (when the expansion input is grounded), this pin initiates the retransmit function.

Retransmit resets the read pointer to zero. The read and write signals must be HIGH before and after the rising edge of the retransmit pulse. The retransmit feature is useful when the same data needs to be read again without rewriting it into the FIFO. Pulsing the retransmit pin will cause the read pointer to be reset to zero, and the previously read data can be read again. The flags will change according to the relative location of the pointers after the retransmit pulse.

Expansion In ($\overline{XI}$)

This is a dual-purpose pin. When it is grounded, it indicates that the FIFO is a standalone device. When it is not grounded, it indicates that the FIFO is in the depth-expansion mode. In the depth-expansion mode, this pin is connected to the $\overline{XO}$ pin of the previous device.

DATA OUTPUTS

Data Outputs Q8-Q0

The 9-bit data output bus Q8-Q0 receives the read data from the FIFO. It is active whenever the read signal is LOW. It is in a high-impedance state when the read signal is HIGH. It is also in high impedance when the FIFO Empty flag is active (i.e., when the FIFO is empty).

CONTROL OUTPUTS

Full Flag ($\overline{FF}$)

The Full flag indicates that the FIFO is full. The Full flag is asserted when there is only one empty location in the FIFO and a falling edge of the write signal initiates the last write operation. The rising edge of the read signal de-asserts the flag, as at least one location has become available.

Empty Flag ($\overline{EF}$)

The Empty flag indicates the FIFO is empty. It is asserted when there is only one word in the FIFO, and a falling edge of the read signal initiates the last read operation. The rising edge of the write signal de-asserts the flag, as one word is now present in the FIFO.

Expansion Out/Half-Full Flag ($\overline{XO}/\overline{HF}$)

This is a dual-purpose flag. In the single-device mode, the expansion in ($\overline{XI}$) is grounded, and the Half-Full flag output is present on this pin. Whenever the FIFO is more than half-full, the flag remains asserted. When the FIFO is exactly half-full and the next falling edge of the write signal asserts the flag. The rising edge of read that causes the FIFO to be half-full will de-assert the Half-Full flag. It will remain asserted until the FIFO is half-full or less than half-full. The name given to the flag is Half-Full, but it is asserted on the one plus the half-full condition.

In the depth-expansion mode, the expansion out ($\overline{XO}$) is connected to the expansion in ($\overline{XI}$) of the next device. This causes the next device to perform write or read operations.

FUNCTION TABLES

RESET AND RETRANSMIT FUNCTION TABLE

	INPUTS			INTERNAL STATUS		OUTPUTS		
Mode	$\overline{RS}$	$\overline{FL}/\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	L	X	L	Location Zero	Location Zero	L	H	H
Retransmit	H	L	L	Location Zero	Unchanged	(3)	(3)	(3)
Read/Write	H	H	L	Increment[1]	Increment[2]	(4)	(4)	(4)

Notes:
1. The read pointer will increment if the FIFO is not empty.
2. The write flag will increment if the FIFO is not full.
3. The flags will change after the retransmit operation and will correspond to the read pointer
   being at location zero.
4. The flags will reflect the relative locations of the read and write pointers.

RESET AND FIRST-LOAD FUNCTION TABLE

	INPUTS			INTERNAL STATUS		OUTPUTS		
Mode	$\overline{RS}$	$\overline{FL}/\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	L	L	(1)	Location Zero	Location Zero	L	H	H
Retransmit	L	H	(1)	Location Zero	Location Zero	(3)	(3)	(3)
Read/Write	H	(2)	(1)	Increment[1]	Increment[2]	(4)	(4)	(4)

Notes:
1. The expansion in ($\overline{XI}$) is connected to the expansion out ($\overline{XO}$) of the previous device.
2. The device with $\overline{FL}$ tied LOW will receive the first N writes and first N reads, where N is the FIFO size. On the Nth write,
   the $\overline{XO}$ pulse is sent to the next device to indicate that it will receive the (N+1)th write. Similarly, on the Nth read, another
   $\overline{XO}$ pulse is sent to the next device to indicate that it will output the (N+1)th read.
3. The read and write pointers will be activated according to whether the FIFO received an $\overline{XO}$ pulse, or whether they were
   the first device in the daisy chain. The flags will reflect the empty or full conditions for the individual FIFOs. To create
   the composite Full and Empty flags, an OR-ing of the individual flags is required.
4. The flags will reflect the relative locations of the read and write pointers.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground .... −0.5 to +7.0V
DC Output Voltage V_{OUT} .... −0.5 to Vcc + 0.5V
DC Input Voltage V_{IN} .... −0.5 to Vcc + 0.5V
AC Input Voltage (Pulse Width ≤ 20 ns) .... −3.0V
DC Input Diode Current with V_{IN} < 0 .... −20 mA
DC Output Current with V_{IN} > Vcc .... 20 mA
DC Output Diode Current with V_{OUT} < 0 .... −50 mA
DC Output Current with V_{OUT} > Vcc .... 50 mA
DC Output Current Max Sink Current/Pin .... +70 mA
DC Output Current Max Source Current/Pin .... −30 mA
Total DC Ground Current .... (NxI$_{OL}$ + MxΔIcc) mA
Total DC Vcc Power Supply Current .... (NxI$_{OH}$ + MxΔIcc) mA
   (N = Number of Outputs, M = Number of Inputs)
T_{STG} StorageTemperature .... −65°C to +150°C

Note: Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to this device, resulting in functional- or reliability-type failures.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Commercial Vcc = 5V ± 10%, Ta = 0°C to +70°C

Symbol	Parameter	Test Conditions	Min	Max	Units
V_{IH}	Input HIGH Voltage	Logic HIGH for All Inputs	2.0	6.0	V
V_{IL}	Input LOW Voltage	Logic LOW for All Inputs	—	0.8	V
V_{OH}	Output HIGH Voltage	I_{OH} = –2 mA, Vcc = 4.5V	2.4	—	V
V_{OL}	Output LOW Voltage	I_{OL} = 8 mA, Vcc = 4.5V	—	0.4	V
$|I_{OZ}|$	Output Leakage	Vcc = 5.5V, Vout = Vcc or 0V	—	10	μA
$|I_{I}|$[1]	Input Leakage	Vcc = 5.5V, GND < V_{IN} < Vcc	—	1	μA

Note: $I_I = I_{IH} = I_{IL}$

CAPACITANCE

Ta = 25°C, f = 1.0 MHz

Name	Description	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	V_{IN} = 0V	5	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5	8	pF

Note: Capacitance is guaranteed but not tested.

POWER-SUPPLY CHARACTERISTICS

Symbol	Parameter	Com	Units
I_{CC1}[1]	Operating Current Vcc = Max, Outputs Open	100	mA
I_{CC2}	Standby Current $\overline{R} = \overline{W} = \overline{RS} = \overline{FL}/\overline{RT} = V_{IH}$	15	mA
I_{SB}	Power-Down Current All Inputs at V_{HC} or V_{IC} $\overline{R} = \overline{W} = \overline{RS} = \overline{FL}/\overline{RT} = V_{HC}$	5	mA

Note:
1. Icc is tested at 30 MHz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial Vcc = 5V ± 10%, TA = 0°C to +70°C

READ CYCLE TIMING

Sym	Parameter	-12	-15	-20	-25	-35	-50	-80	Unit	Type
tRF	Read Frequency, MHz[2]	50	40	33	28	22	15	10	MHz	Min
tRC	Read Cycle Time	20	25	30	35	45	65	100	ns	Min
tA	Read Access Time	12	15	20	25	35	50	80	ns	Max
tRR	Read Recovery Time	8	10	10	10	10	15	20	ns	Min
tRPW	Read Pulse Width[1]	12	15	20	25	35	50	80		
tRLZ	$\overline{R}$ Data Bus Low-Z[2]	3	3	3	3	3	3	3		
tWLZ	$\overline{W}$ Data Bus Low-Z[2,3]	3	3	3	3	3	3	3		
tDV	$\overline{R}$ HIGH to Data Hold Time	5	5	5	5	5	5	5		
tRHZ	$\overline{R}$ to Data High-Z[2]	12	14	18	18	20	30	35		

WRITE CYCLE TIMING

Sym	Parameter	-12	-15	-20	-25	-35	-50	-80	Unit	Type
tWF	Write Frequency, MHz[2]	50	40	33	28	22	15	10	ns	Min
tWC	Write Cycle Time	20	25	30	35	45	65	100		
tWPW	Write Pulse Width[1]	12	15	20	25	35	50	80		
tWR	Write Recovery Time	8	10	10	10	10	15	20		
tDS	Write Data Setup Time	7	9	12	15	18	30	40		
tDH	Write Data Hold Time	0	0	0	0	0	0	0		

RESET AND RETRANSMIT CYCLE TIMING

Sym	Parameter	-12	-15	-20	-25	-35	-50	-80	Unit	Type
tRSC	Reset Cycle Time	20	25	30	35	45	65	100	ns	Min
tRS	Reset Pulse Width[1]	12	15	20	25	35	50	80		
tRSS	Reset Setup Time	12	15	20	25	35	50	80		
tRSR	Reset Recovery Time	8	10	10	10	10	15	20		
tRTC	Reset Cycle Time	20	25	30	35	45	65	100		
tRT	Retransmit Pulse Width[1]	12	15	20	25	35	50	80		
tRTS	Retransmit Setup Time	12	15	20	25	35	50	80		
tRTR	Retransmit Recovery Time	8	10	10	10	10	15	20		

Notes: These timings are measured as defined in AC Test Conditions.

1. Pulse widths less than the specified minimum value may upset the internal pointers and are not allowed.
2. These values are guaranteed by design and not tested.
3. This applies to the read data flow-through mode only.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial Vcc = 5V ± 10%, TA = 0°C to +70°C

FLAG TIMING

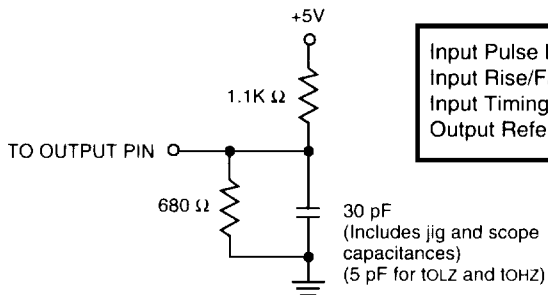| Sym	Parameter	-12	-15	-20	-25	-35	-50	-80	Unit	Type
tREF	Read Low to $\overline{EF}$ Low	12	15	20	25	30	45	60	ns	Max
tRFF	Read High to $\overline{FF}$ High	12	15	20	25	30	45	60		
tRHF	Read High to $\overline{HF}$ High	12	15	20	25	35	45	60		
tRPE	Read Pulse After $\overline{EF}$ High	12	15	20	25	35	50	80	ns	Min
tWEF	Write Low to $\overline{EF}$ Low	12	15	20	25	30	45	60	ns	Max
tWFF	Write High to $\overline{FF}$ High	12	15	20	25	30	45	60		
tWHF	Write High to $\overline{HF}$ High	12	15	20	25	35	45	60		
tWPE	Write Pulse After $\overline{EF}$ High	12	15	20	25	35	50	80	ns	Min
tEFL	Reset Low to $\overline{EF}$ Low	12	15	20	25	35	45	60	ns	Max
tFFH	Reset High to $\overline{FF}$ High	12	15	20	25	35	45	60		
tHFH	Reset High to $\overline{HF}$ High	12	15	20	25	35	45	60		

EXPANSION TIMING

Sym	Parameter	-12	-15	-20	-25	-35	-50	-80	Unit	Type
tXOL	Read/Write to $\overline{XO}$ Low	12	15	20	25	35	50	80	ns	Min
tXOH	Read/Write to $\overline{XO}$ High	12	15	20	25	35	50	80		
tXI	$\overline{XI}$ Pulse Width	12	15	20	25	35	50	80		
tXIR	$\overline{XI}$ Recovery Time	8	10	10	10	10	10	10		
tXIS	$\overline{XI}$ Setup Time	8	10	15	15	15	15	15		

FIGURE 3. AC TEST CONDITIONS

+5V

1.1K Ω

TO OUTPUT PIN

680 Ω

30 pF
(Includes jig and scope capacitances)
(5 pF for tOLZ and tOHZ)

Input Pulse Levels .... GND to 3.0V
Input Rise/Fall Times .... 3 ns
Input Timing Reference Levels 1.5V
Output Reference Levels 1.5V

TIMING DIAGRAMS

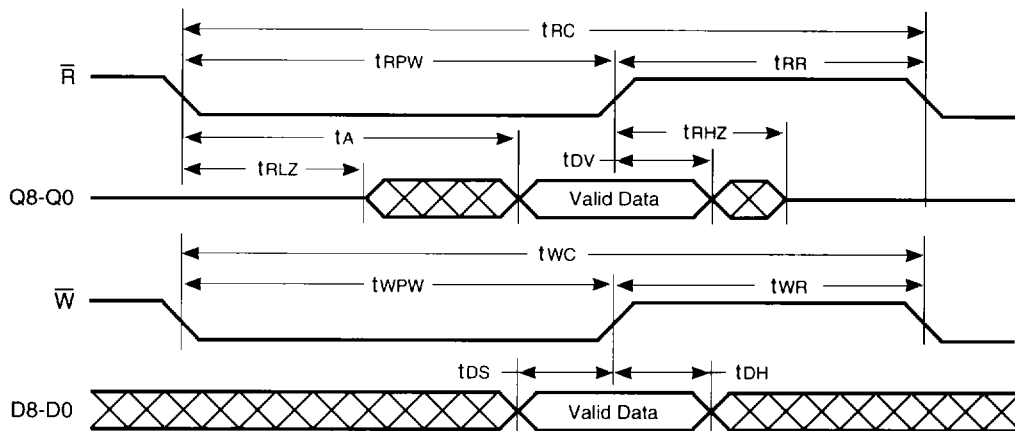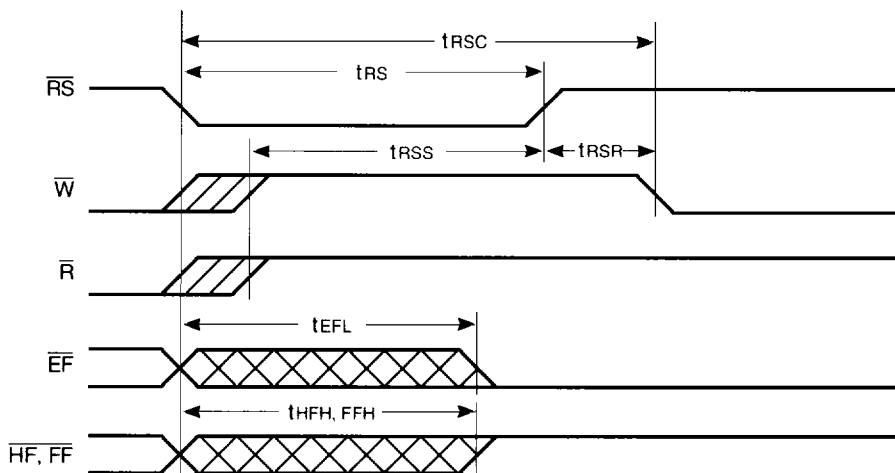### FIGURE 4. ASYNCHRONOUS READ AND WRITE OPERATIONS

FIGURE 5. RESET TIMING

Notes:

1. Read and write have to be at a HIGH level around the rising edge of reset. The flags may change during reset but are valid at t_{RSC}.

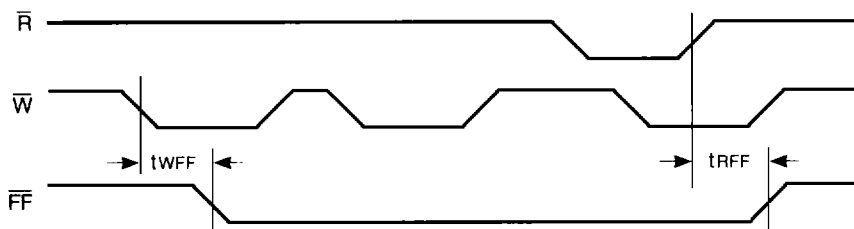## FIGURE 6. FULL FLAG BEHAVIOR FROM LAST WRITE TO FIRST READ

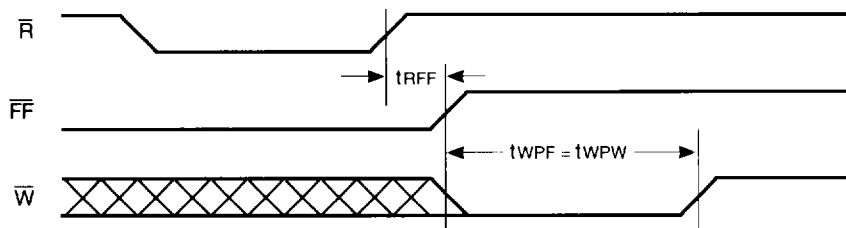## FIGURE 7. FULL FLAG AND REQUIRED WRITE PULSE AT FULL CONDITION
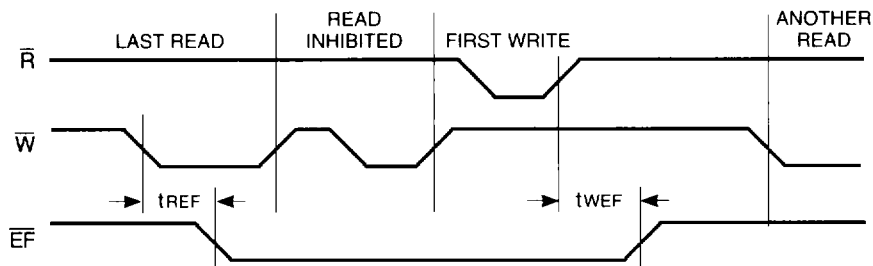

FIGURE 8. EMPTY FLAG BEHAVIOR FROM LAST READ TO FIRST WRITE

FIGURE 9. EMPTY FLAG AND REQUIRED WRITE PULSE AT EMPTY CONDITION
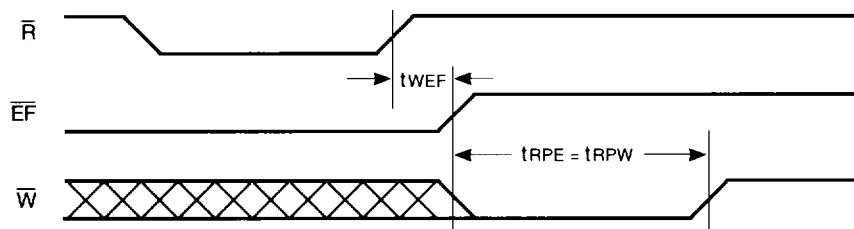
FIGURE 10. HALF-FULL FLAG TIMING

| | HALF FULL | MORE THAN HALF FULL | HALF FULL | MORE THAN HALF FULL |

$\overline{W}$

$\overline{R}$

t_{WHF} t_{RHF}

$\overline{HF}$
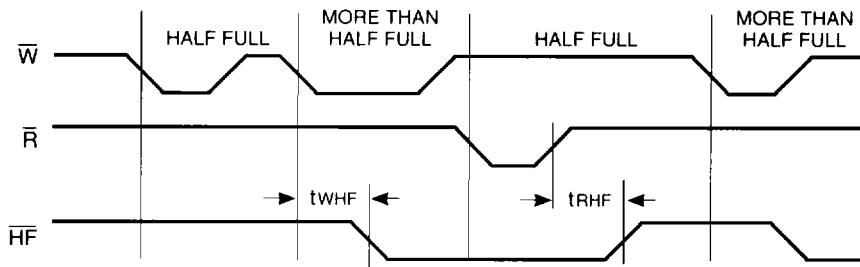
FIGURE 11. RETRANSMIT FUNCTION TIMING

t_{RTC}

t_{RT}

$\overline{RT}$

t_{RTS} t_{RTR}

$\overline{R}, \overline{W}$

$\overline{EF}, \overline{FF}, \overline{HF}$ VALID FLAGS
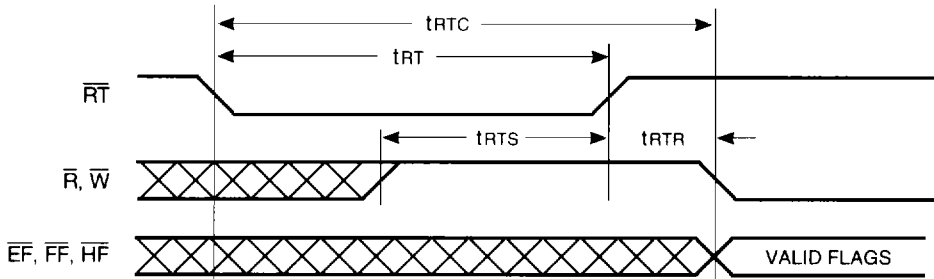
FIGURE 12. EXPANSION-OUT TIMING

WRITE OR READ TO LAST PHYSICAL LOCATION OF DEVICE 1 | WRITE OR READ TO FIRST PHYSICAL LOCATION OF DEVICE 2

$\overline{W}, \overline{R}$

t_{XOL} t_{XOH}

$\overline{XO1}, (\overline{XI2})$
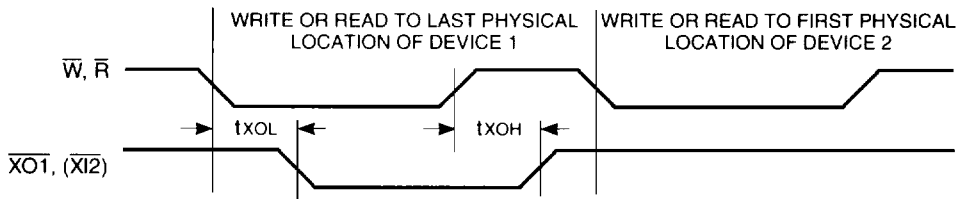
Note:
1. The expansion out ($\overline{XO}$) of device 1 is connected to the expansion in ($\overline{XI}$) of device 2.
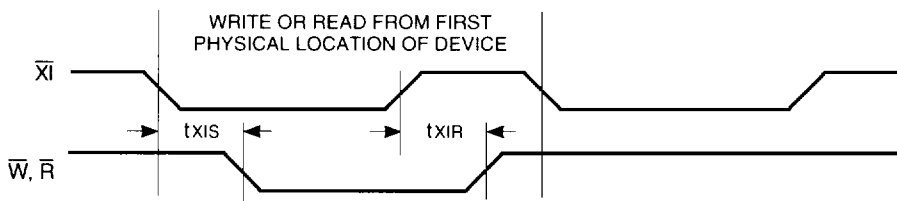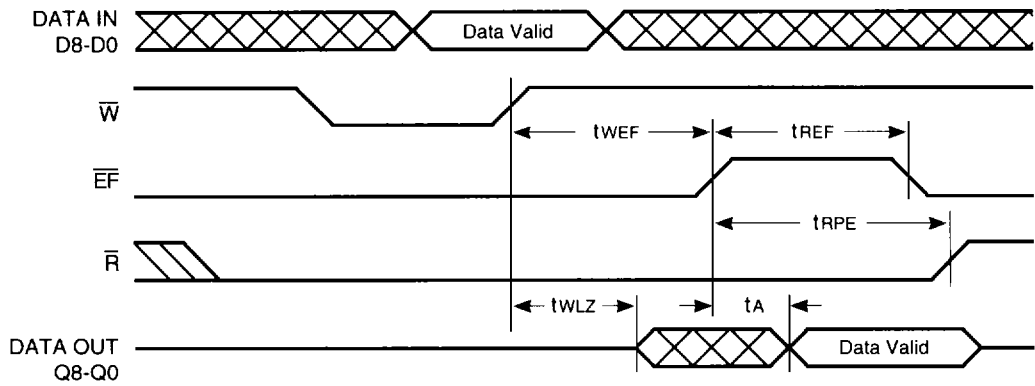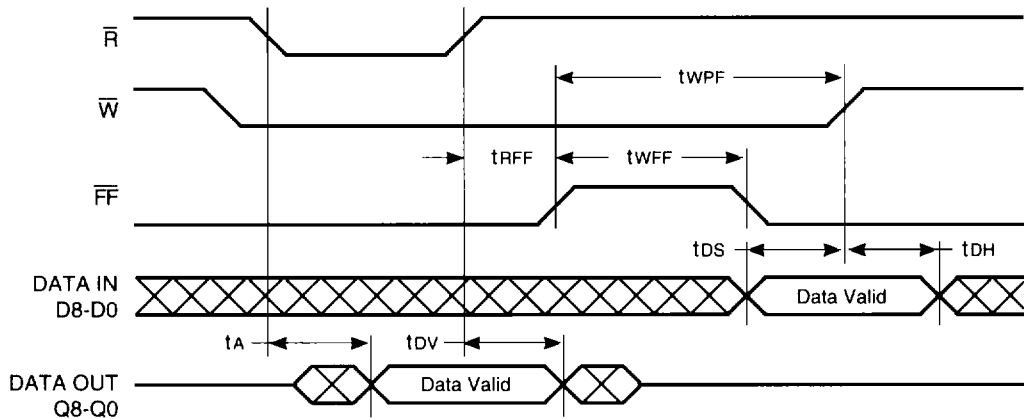
FIGURE 13. EXPANSION-IN TIMING

WRITE OR READ FROM FIRST PHYSICAL LOCATION OF DEVICE

$\overline{XI}$

t_{XIS} t_{XIR}

$\overline{W}, \overline{R}$

FIGURE 14. READ DATA FLOW-THROUGH MODE

FIGURE 15. WRITE DATA FLOW-THROUGH MODE

QUALITY SEMICONDUCTOR, INC.

OPERATING MODES

SINGLE-DEVICE MODE

A FIFO is in standalone mode when the expansion in ($\overline{XI}$) control is grounded. In this mode the Half-Full flag is available on the shared $\overline{XO}/\overline{HF}$ line. Figure 16 shows the standalone mode, and this applies to FIFO width expansion, as shown in Figure 17.

DEPTH-EXPANSION MODE

A FIFO is in the depth-expansion mode when the expansion-in ($\overline{XI}$) control is not grounded but tied to the expansion-out ($\overline{XO}$) pin of the previous FIFO. Using the depth-expansion mode, the QS7201/02 can be easily cascaded to create FIFOs of larger depth. The devices are cascaded as shown in Figure 18. In the depth-expansion mode, the device that receives the first word of data has its first load input grounded. The other devices have their first load inputs in the HIGH state. Two 4-input OR gates are required to create the composite Full and Empty flags for the FIFO array. In using the depth-expansion mode, care must be taken to keep the traces short from the expansion in ($\overline{XI}$) of one device to the expansion out ($\overline{XO}$) of the next device to minimize crosstalk noise.

FLOW-THROUGH MODES

Flow-through modes refer to the internal operation of the FIFO in empty and full conditions. Flow-through modes allow data to flow directly through the FIFO from input to output under the appropriate empty and full conditions.

Two types of flow-through modes, a read flow-through and a write flow-through, are supported by the FIFO. In the read flow-through mode, the FIFO is empty and the read side is waiting for data from a write. Read flow-through is represented by an empty FIFO that has its read line held LOW, and a write occurs. This rising edge of the write would de-assert the Empty flag and cause valid data to appear on the outputs after a certain time delay of $t_{WEF} + t_A$. The read line being LOW would cause the data to be read and also assert the Empty flag once again. The user must raise the read line in order to increment the read pointer.

In the write flow-through mode, the FIFO is full and the write side is waiting for a word location to be made available by a read. A write flow-through operation permits the writing of a single word of data immediately after reading one word of data from a full FIFO. This is similar to the read flow-through case, and the write line must toggled to increment the write pointer.
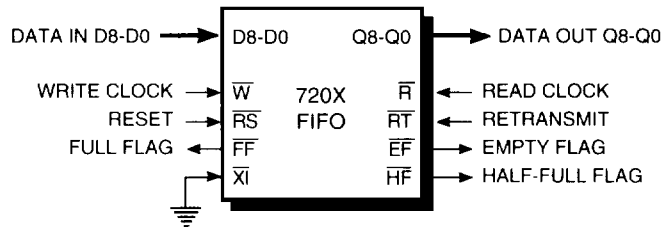
FIGURE 16. THE FIFO IN STANDALONE MODE

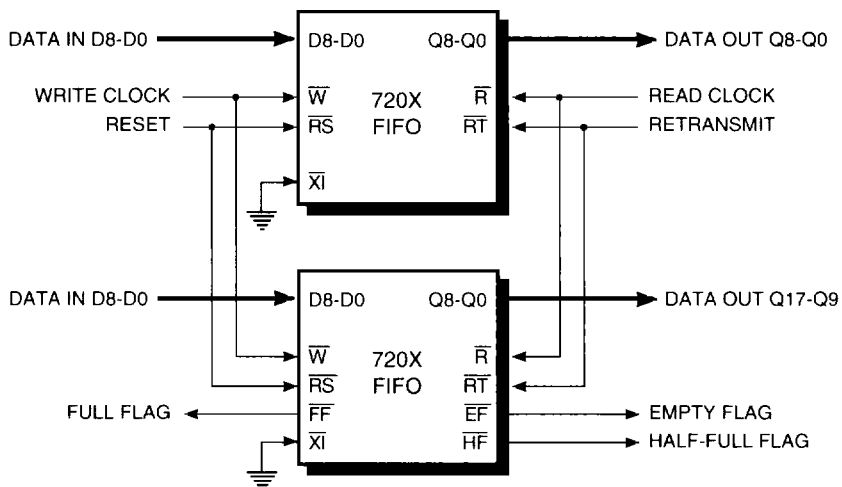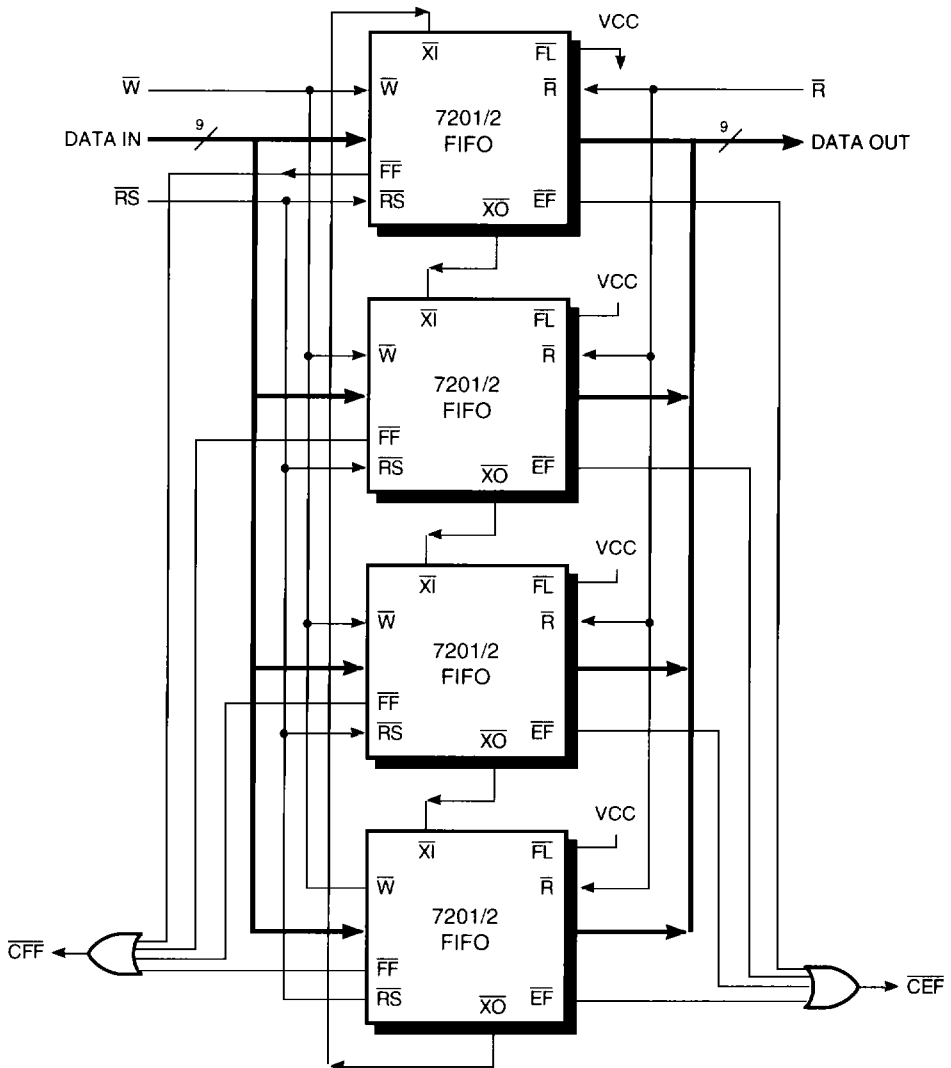## FIGURE 17. AN 18-BIT-WIDE FIFO USING TWO FIFOs

FIGURE 18. BUILDING A 4N-DEEP FIFO USING FOUR N-DEEP FIFOs

Note: The composite Empty and Full flags require the OR-ing of the individual Empty and Full flags, respectively.

ORDERING INFORMATION
Example:

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                    QS72 01 - 12 JR
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Specialty Memory
Product Prefix
(QS72)

Part Number
01 (512 x 9)
02 (1K x 9)

Package
JR (32-Pin PLCC)
P (28-Pin PDIP)
Q (28-Pin QSOP)
SO (28-Pin SOIC)
V (28-Pin SOJ)

Speed
-12 ns
-15 ns
-20 ns
-25 ns
-35 ns
-50 ns
-80 ns