Contents

The S-29453A Series is high speed, low power 8K-bit serial E2PROM with a wide operating voltage range. It is organized as 512-word×16-bit. It is capable of sequential read, where addresses are automatically incremented in 16-bit blocks. The instruction code is compatible with the M6M800X1 Series.

■ Features

- Low power consumption
  Standby : 1 μA Max.
  Operating : 1.2 mA Max. (V_{CC}=5.5 V)
  0.4 mA Max. (V_{CC}=2.5 V)
- Wide operating voltage range
  Write : 2.5 to 5.5 V
  Read : 1.8 to 5.5 V
- Sequential read capable
- Endurance : 10^5 cycles/word
- Data retention : 10 years

■ Pin Assignment

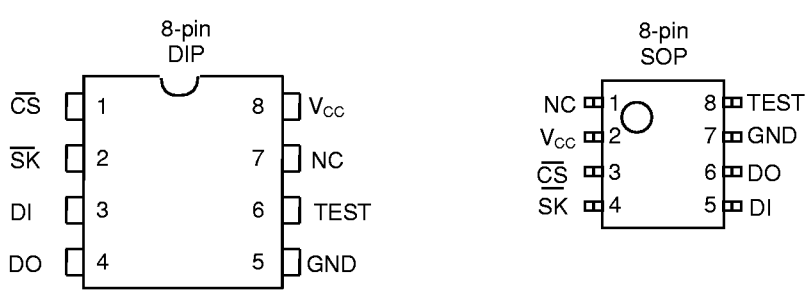


Figure 1

$\overline{CS}$	Chip select input
$\overline{SK}$	Serial clock input
DI	Serial data input
DO	Serial data output
GND	Ground (0 V)
V_{CC}	Power supply
TEST	Test pin (normally kept open) (can be connected to GND or Vcc)

■ Block Diagram

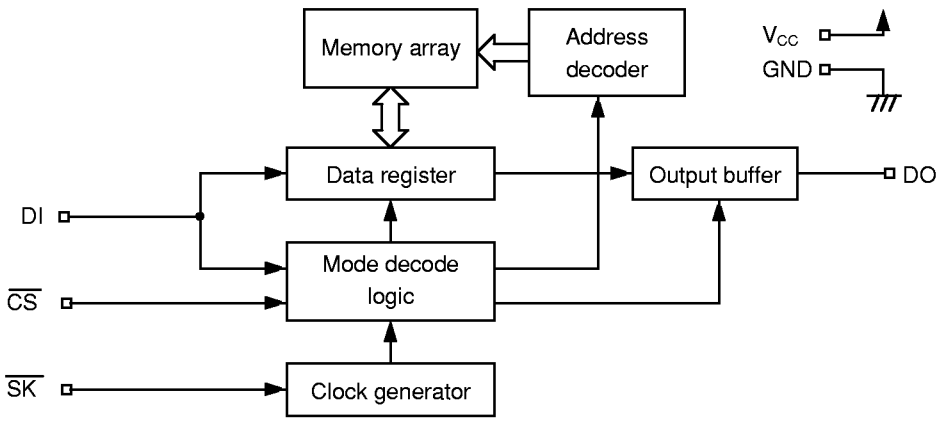


Figure 2

■ Instruction Set

Table 1

Instruction	Operation block	Address	Data
READ (Read data)	$1010100A_8$	A_7 to A_0	D_{15} to D_0 output*
PROGRAM (Write data)	$1010010A_8$	A_7 to A_0	D_{15} to D_0
EWEN (Program enable)	10100011	xxxxxxxx	—
EWDS (Program disable)	10100000	xxxxxxxx	—

x : Doesn't matter.

* : When 16-bit data of the specified address is output, the data of the next address is output.

■ Absolute Maximum Ratings

Table 2

Parameter	Symbol	Ratings	Unit
Power supply voltage	V_{CC}	-0.3 to +7.0	V
Input voltage	V_{IN}	-0.3 to V_{CC}+0.3	V
Output voltage	V_{OUT}	-0.3 to V_{CC}	V
Storage temperature under bias	T_{bias}	-50 to +95	°C
Storage temperature	T_{stg}	-65 to +150	°C

■ Recommended Operating Conditions

Table 3

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power supply voltage	V_{CC}	Read Operation	1.8	—	5.5	V
		Write Operation	2.5	—	5.5	V
High level input voltage	V_{IH}	V_{CC}=2.5 to 5.5V	0.8×V_{CC}	—	V_{CC}	V
		V_{CC}=1.8 to 2.5V	0.8×V_{CC}	—	V_{CC}	V
Low level input voltage	V_{IL}	V_{CC}=2.5 to 5.5V	0.0	—	0.2×V_{CC}	V
		V_{CC}=1.8 to 2.5V	0.0	—	0.15×V_{CC}	V
Operating temperature	T_{opr}		-40	—	+85	°C

■ DC Electrical Characteristics

Table 4

Parameter	Symbol	Conditions	V_{CC}=5.0 V±10 %			V_{CC}=2.5 to 3.3 V			V_{CC}=1.8 to 2.5 V			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Current consumption (READ)	I_{CC1}	DO unloaded	—	—	1.2	—	—	0.5	—	—	0.4	mA
Current consumption (PROGRAM)	I_{CC2}	DO unloaded	—	—	5.0	—	—	2.0	—	—	—	mA

Parameter	Symbol	Conditions	V_{CC}=5.0 V±10 %			V_{CC}=2.5 to 4.5 V			V_{CC}=1.8 to 2.5 V			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Standby current consumption	I_{SB}	Input: V_{CC} or GND	—	—	1.0	—	—	1.0	—	—	1.0	μA
Input leakage current	I_{LI}	V_{IN}=GND to V_{CC}	—	0.1	1.0	—	0.1	1.0	—	0.1	1.0	μA
Output leakage current	I_{LO}	V_{OUT}=GND to V_{CC}	—	0.1	1.0	—	0.1	1.0	—	0.1	1.0	μA
Low level output voltage	V_{OL}	CMOS I_{OL}=100 μA	—	—	0.1	—	—	0.1	—	—	0.1	V
		TTL I_{OL}=2.1 mA	—	—	0.45	—	—	—	—	—	—	V
High level output voltage	V_{OH}	CMOS V_{CC}=2.5 to 5.5 V : I_{OH}=-100 μA V_{CC}=1.8 to 2.5 V : I_{OH}=-10 μA	V_{CC}-0.7	—	—	V_{CC}-0.7	—	—	V_{CC}-0.3	—	—	V
		TTL, I_{OH}=-400 μA	2.4	—	—	—	—	—	—	—	—	V
Write enable latch data hold voltage	V_{DH}		1.5	—	—	1.5	—	—	1.5	—	—	V

■ Endurance

Table 6

Parameter	Symbol	Min.	Typ.	Max.	Unit
Endurance	N_W	10^5	—	—	cycles/word

■ Pin Capacitance

Table 7

(Ta=25°C, f=1.0 MHz, V_{CC}=5 V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input Capacitance	C_{IN}	V_{IN}=0 V	—	—	8	pF
Output Capacitance	C_{OUT}	V_{OUT}=0 V	—	—	10	pF

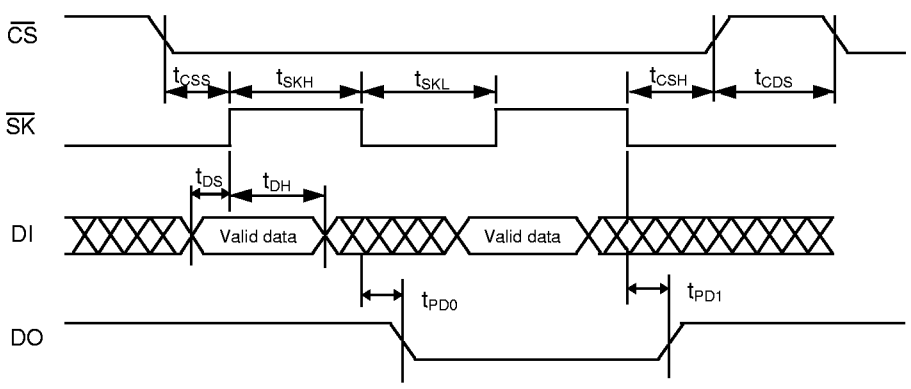
■ AC Electrical Characteristics

Table 8 Measuring conditions

Input pulse voltage	$0.1\times V_{CC}$ to $0.9\times V_{CC}$
Output reference voltage	$0.5\times V_{CC}$
Output load	100pF

Table 9

Parameter	Symbol	Read/Write operations						Read operation			Unit
		V_{CC}=5.0 V±10 %			V_{CC}=2.5 to 4.5 V			V_{CC}=1.8 to 2.5 V			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
$\overline{CS}$ setup time	t_{CSS}	0.2	—	—	0.4	—	—	1.0	—	—	µs
$\overline{CS}$ hold time	t_{CSH}	0.2	—	—	0.4	—	—	1.0	—	—	µs
$\overline{CS}$ setup time (CPU)	$t_{CSS\ (CPU)}$	0.2	—	—	0.4	—	—	1.0	—	—	µs
$\overline{CS}$ hold time (CPU)	$t_{CSH\ (CPU)}$	0.2	—	—	0.4	—	—	1.0	—	—	µs
$\overline{CS}$ deselect time	t_{CDS}	0.2	—	—	0.2	—	—	0.4	—	—	µs
Data setup time	t_{DS}	0.2	—	—	0.4	—	—	0.8	—	—	µs
Data hold time	t_{DH}	0.2	—	—	0.4	—	—	0.8	—	—	µs
1 data output delay time	t_{PD1}	—	—	0.4	—	—	0.8	--	—	2.0	µs
0 data output delay time	t_{PD0}	—	—	0.4	—	—	0.8	--	—	2.0	µs
Clock frequency	f_{SK}	0.0	—	2.0	0.0	—	0.5	0.0	—	0.2	MHz
Clock pulse width	t_{SKH}, t_{SKL}	0.25	—	—	1.0	—	—	2.5	—	—	µs
Output disable time	t_{HZ1}, t_{HZ2}	0	50	150	0	500	1000	—	—	—	ns
Output enable time	t_{SV}	0	50	150	0	500	1000	—	—	—	ns
Programming time	t_{PR}	—	4.0	10	—	4.0	10	—	—	—	ms



Input data is retrieved on the rising edge of $\overline{SK}$.
Output data is triggered on the falling edge of $\overline{SK}$.

Figure 3 Timing Chart

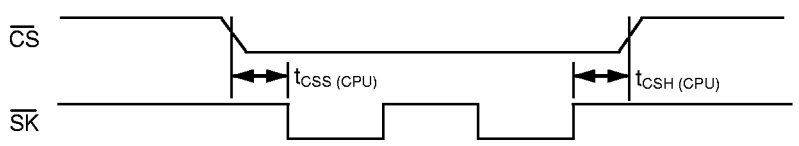


Figure 4 Timing Chart for $t_{CSS\ (CPU)}$ and $t_{CSH\ (CPU)}$ when CPU is connected

■ Operation

Instructions (in the order of operation code, address, and data) are latched to DI in synchronization with the rising edge of $\overline{SK}$ after $\overline{CS}$ goes low. A start-bit can only be recognized when the high of DI is latched at the rising edge of $\overline{SK}$ after changing $\overline{CS}$ to low, it is impossible for it to be recognized as long as DI is low, even if there are $\overline{SK}$ pulses after $\overline{CS}$ goes low. Instruction finishes when $\overline{CS}$ goes high, where it must be high between commands during t_{CDS}.

All input, including DI and $\overline{SK}$ signals, is ignored while $\overline{CS}$ is high. The operation code plus address is a multiple of 8-bits. This makes it easy to prepare your own software using a serial interface incorporated into the CPU.

1. READ

The READ instruction reads data from a specified address. The READ operation code and address are continuously latched in synchronization with the rising edge of $\overline{SK}$. The DO pin begins to output at the 16-th clock from a start-bit. Data is continuously output in synchronization with the falling edge of $\overline{SK}$.

When all of the data (D_{15} to D_0) in the specified address has been read, data in the next address can be read with the input of another $\overline{SK}$ clock. Thus, the data over whole area of the memory can be read by continuously inputting $\overline{SK}$ clocks as long as $\overline{CS}$ is low.

The last address (An ··· A1 A0 = 1 ··· 11) rolls over to the top address (An ··· A1 A0 = 0 ··· 00).

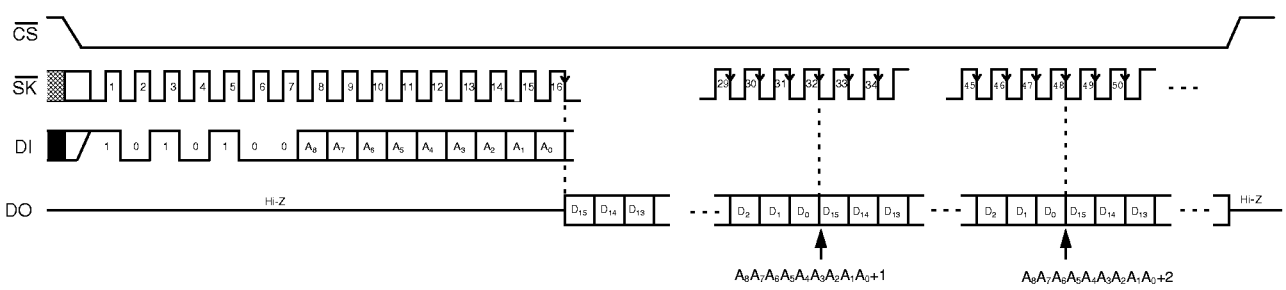


Figure 5 Read Timing

2. PROGRAM

The PROGRAM instruction writes 16-bit data to a specified address.

After changing $\overline{CS}$ to low, input PROGRAM operation code, address, and 16-bit data. If there is a data overflow of more than 16 bits, only the last 16-bits of the data is considered valid. Changing $\overline{CS}$ to high will start the PROGRAM operation. It is not necessary to make the data "1" before initiating the PROGRAM operation.

The write operation is completed in 10 ms (t_{PR} Max.), and the typical write period is less than 5 ms. In the S-29453A, it is easy to VERIFY the completion of the write operation in order to minimize the write cycle by setting $\overline{CS}$ to "L" and checking the DO pin after the write operation begins by setting $\overline{CS}$ to "H" VERIFY operations to detect changes in the DO output can be executed in succession. One is a change from "L" to "H" with $\overline{CS}$="L" The other is a change from "L" to "H" after setting $\overline{CS}$ to "L" and returning $\overline{CS}$ to "H" repeatedly.

Because all $\overline{SK}$ and DI inputs are ignored during the write operation, any input of instruction will also be disregarded. When DO outputs high after completion of the write operation or if it is in the high-impedence state (Hi-Z), the input of instructions is available. Even if the DO pin remains high, it will enter the high-impedence state upon the recognition of a high of DI attached to the rising edge of an $\overline{SK}$ pulse.

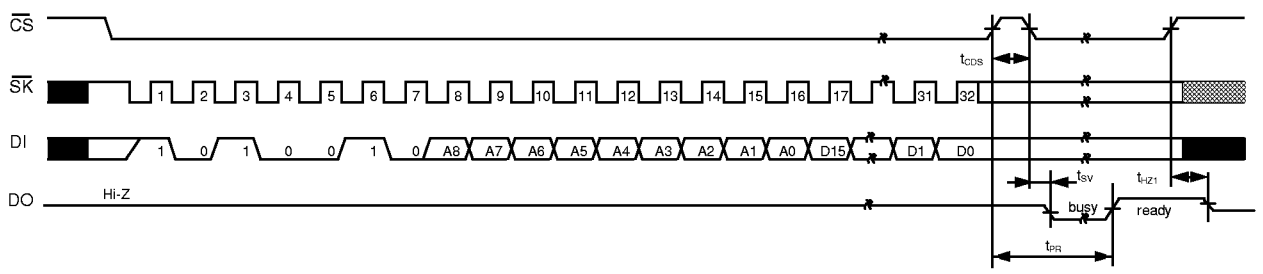


Figure 6 PROGRAM Timing

3. Write enable (EWEN) and Write disable (EWDS)

The EWEN instruction puts the S-29453A into write enable mode, which accepts PROGRAM instruction. The EWDS instruction puts the S-29453A into write disable mode, which refuses PROGRAM instruction.
The S-29453A powers on in write disable mode, which protects data against unexpected, erroneous write operations caused by noise and/or CPU malfunctions. It should be kept in write disable mode except when performing write operations.

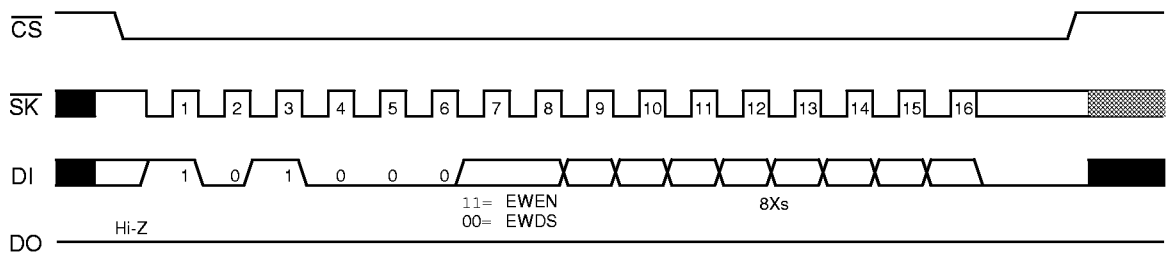


Figure 7 EWEN/EWDS Timing

■ Receiving a Start-Bit

A start-bit can be recognized by latching the high level of DI at the rising edge of $\overline{SK}$ after changing $\overline{CS}$ to low. The write operation begins by inputting the write instruction and setting $\overline{CS}$ to high. The DO pin then outputs low during the write operation and high at its completion by setting $\overline{CS}$ to low (Verify Operation). Therefore, only after a write operation, in order to accept the next command by having $\overline{CS}$ go low, the DO pin is switched from a state of high-impedence to a state of data output; but if it recognizes a start-bit, the DO pin returns to a state of high-impedence (see Figure 8).

Make sure that data output from the CPU does not interfere with the data output from the serial memory IC when you configure a 3-wire interface by connecting DI input pin and DO output pin. Such interference may cause a start-bit fetch problem.

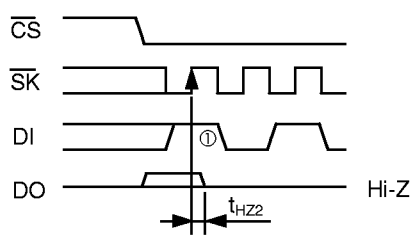


Figure 8 Start-Bit latching timing

■ Three-Wire Interface (DI-DO direct connection)

Although the normal configuration of a serial interface is a 4-wire interface to $\overline{CS}$, $\overline{SK}$, DI, and DO, a 3-wire interface is also a possibility by connecting DI and DO. However, since there is a possibility that the DO output from the serial memory IC will interfere with the data output from the CPU with a 3-wire interface, install a resistor between DI and DO in order to give preference to data output from the CPU to DI(See Figure 9).

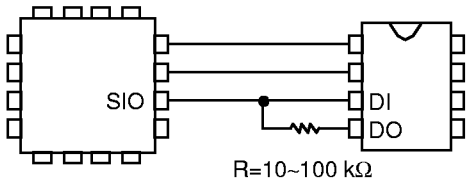


Figure 9 3-wire interface

■ Dimensions (Unit : mm)

1. 8-pin DIP

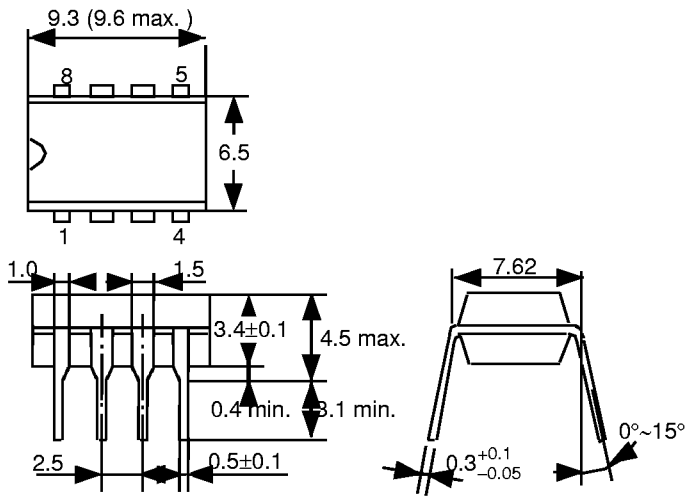


Figure 10

2. 8-pin SOP

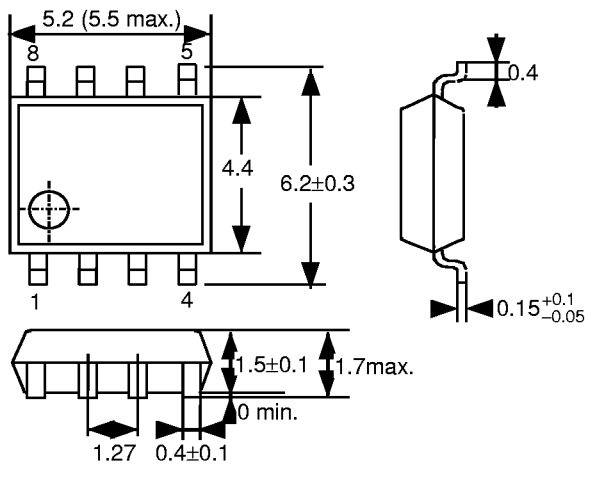


Figure 11

■ Ordering Information

S-29453A XX

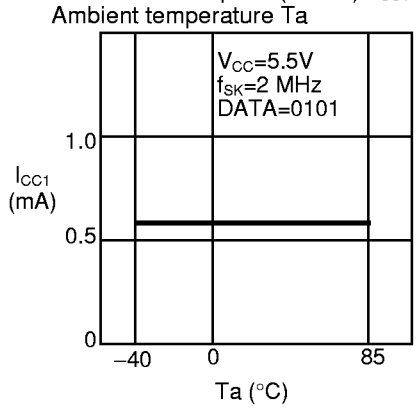
Package

DP : DIP
FE : SOP

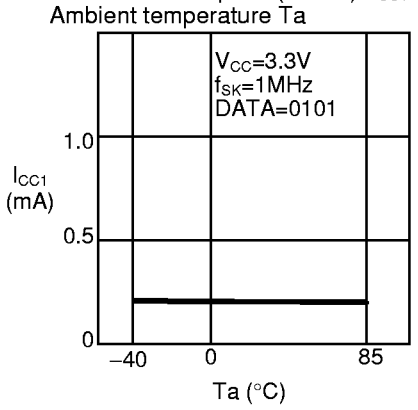
■ Characteristics

1. DC Characteristics

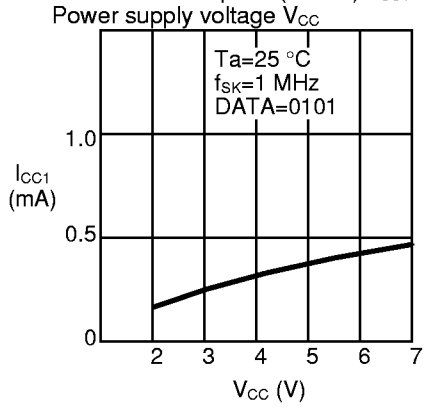
1.1 Current consumption (READ) I_{CC1} - Ambient temperature Ta



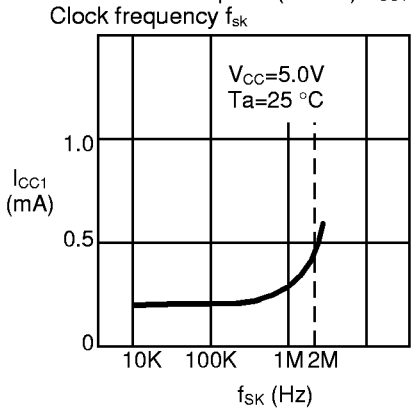
1.2 Current consumption (READ) I_{CC1} - Ambient temperature Ta



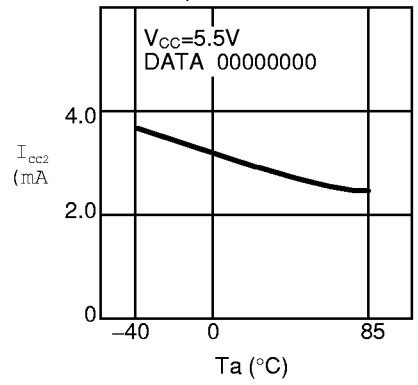
1.3 Current consumption (READ) I_{CC1} - Power supply voltage V_{CC}



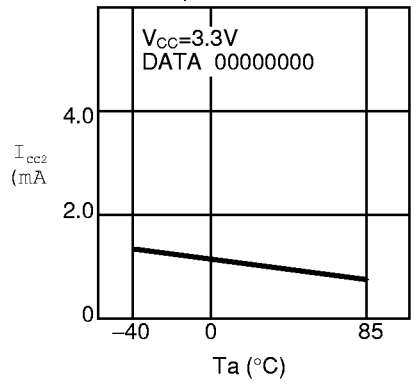
1.4 Current consumption (READ) I_{CC1} - Clock frequency f_{sk}



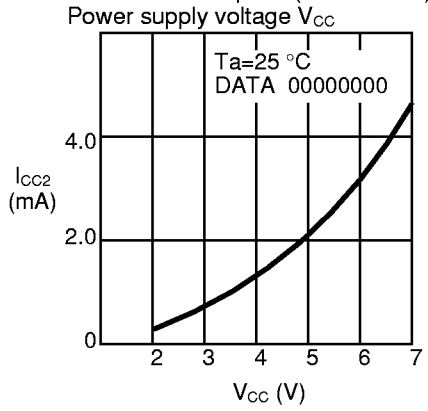
1.5 Current consumption (PROGRAM) I_{CC2} - Ambient temperature Ta



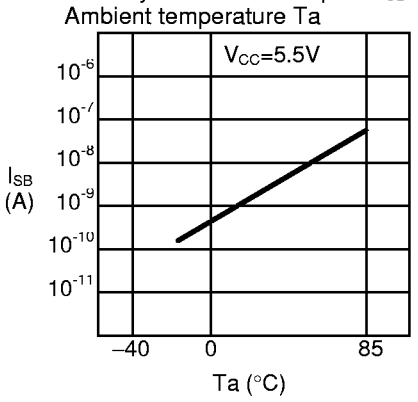
1.6 Current consumption (PROGRAM) I_{CC2} - Ambient temperature Ta



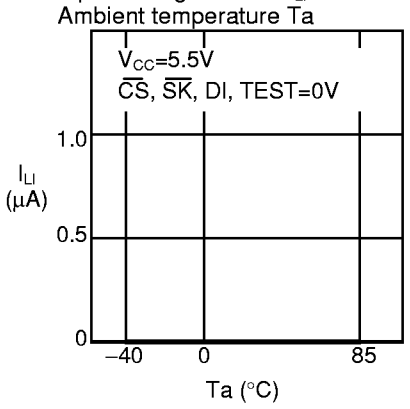
1.7 Current consumption (PROGRAM) I_{CC2} - Power supply voltage V_{CC}



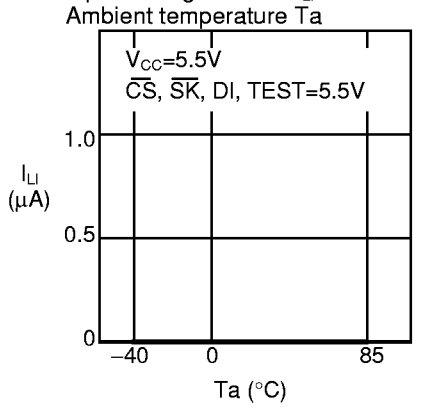
1.8 Standby current consumption I_{SB} -- Ambient temperature Ta



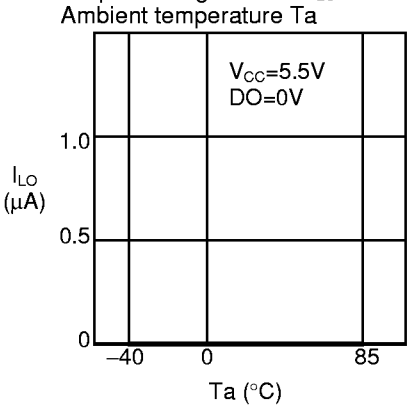
1.9 Input leakage current I_{LI} - Ambient temperature Ta



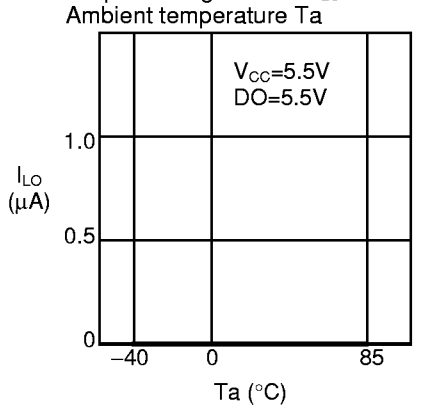
1.10 Input leakage current I_{LI} - Ambient temperature Ta



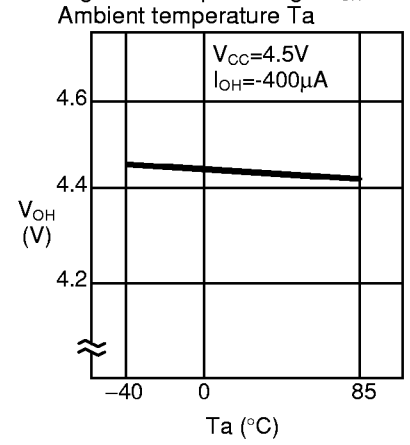
1.11 Output leakage current I_{LO} - Ambient temperature Ta



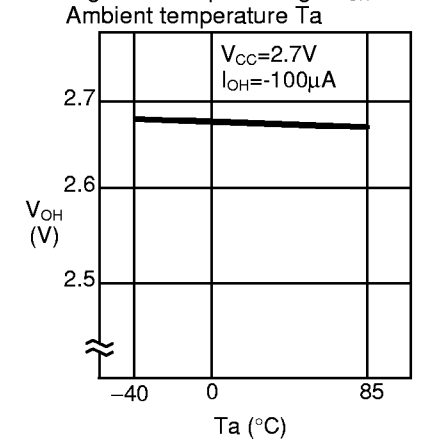
1.12 Output leakage current I_{LO} - Ambient temperature Ta



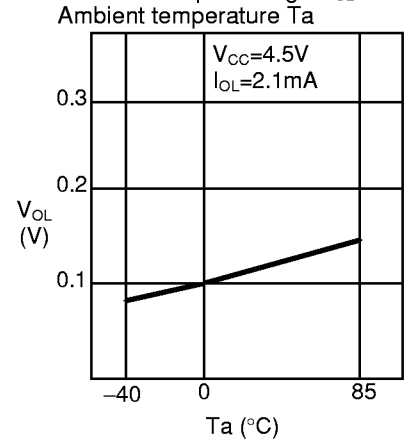
1.13 High level output voltage V_{OH} - Ambient temperature Ta



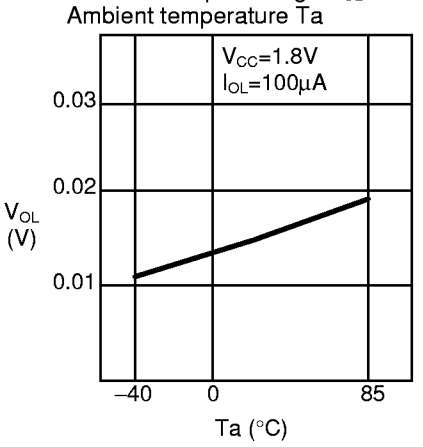
1.14 High level output voltage V_{OH} - Ambient temperature Ta



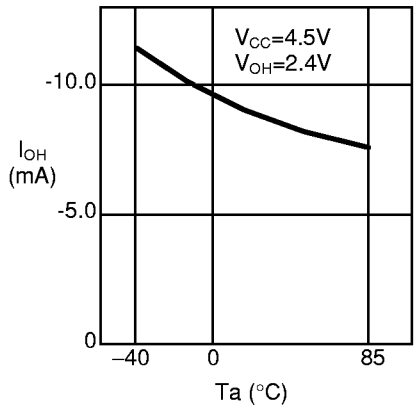
1.15 Low level output voltage V_{OL} - Ambient temperature Ta



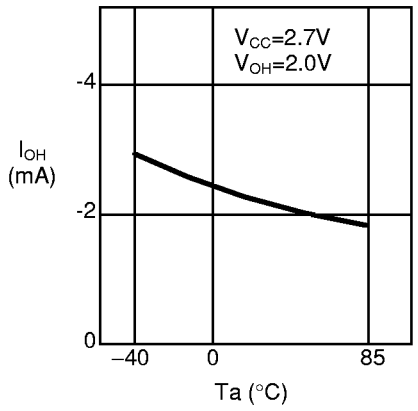
1.16 Low level output voltage V_{OL} - Ambient temperature Ta



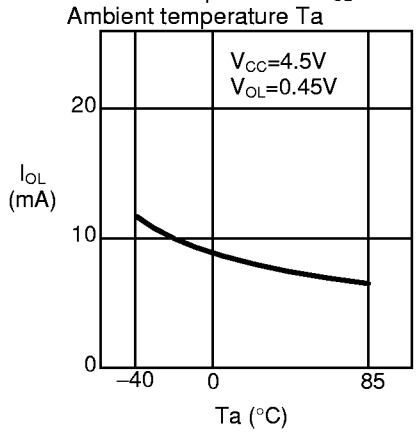
1.17 High level output current I_{OH} - Ambient temperature Ta



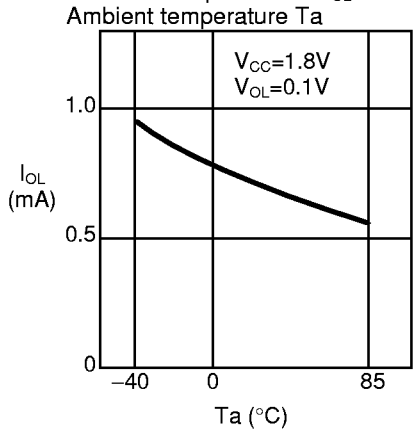
1.18 High level output current I_{OH} - Ambient temperature Ta



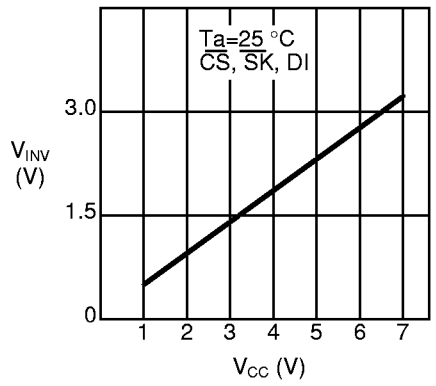
1.19 Low level output current I_{OL} - Ambient temperature Ta



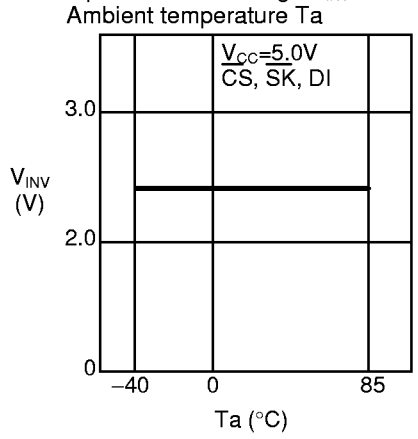
1.20 Low level output current I_{OL} - Ambient temperature Ta



1.21 Input inversion voltage V_{INV} - Power supply voltage V_{CC}

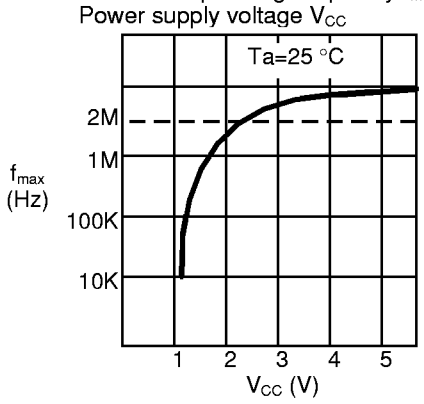


1.22 Input inversion voltage V_{INV} - Ambient temperature Ta

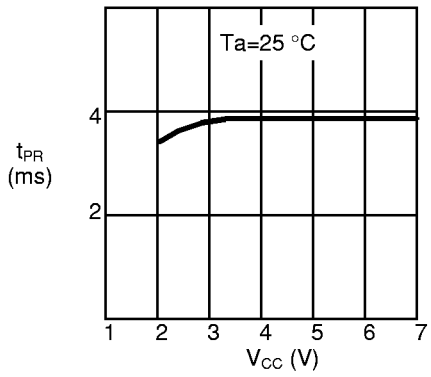


2. AC Characteristics

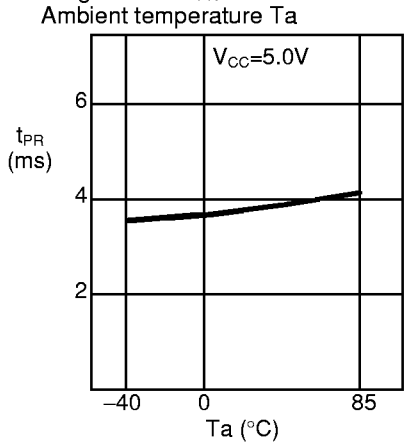
2.1 Maximum operating frequency f_{max} - Power supply voltage V_{CC}



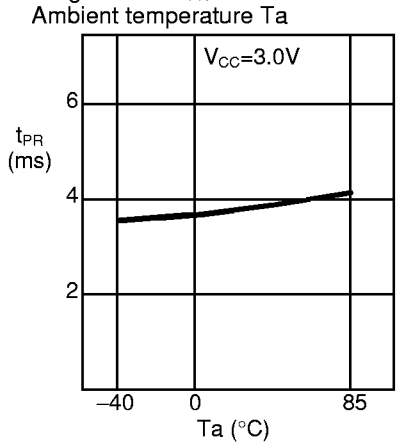
2.2 Program time t_{PR} - Power supply voltage V_{CC}



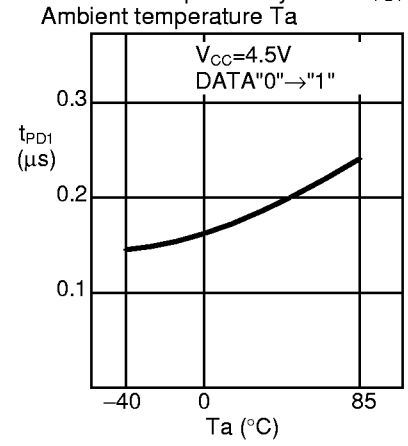
2.3 Program time t_{PR} - Ambient temperature Ta



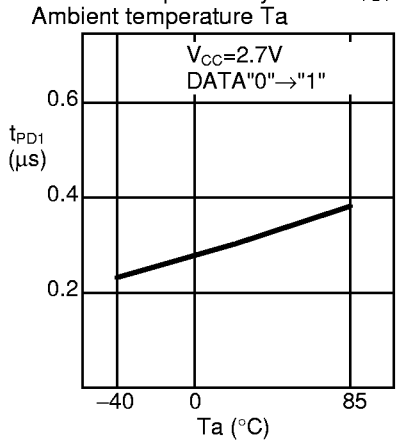
2.4 Program time t_{PR} - Ambient temperature Ta



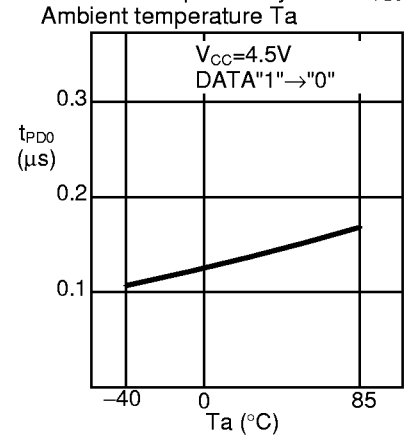
2.5 "1" Data output delay time t_{PD1} - Ambient temperature Ta



2.6 "1"Data output delay time t_{PD1} - Ambient temperature Ta



2.7 “0” Data output delay time t_{PD0} - Ambient temperature Ta



2.8 "0" Data output delay time t_{PD0} - Ambient temperature Ta