1Mx32 SRAM MODULE

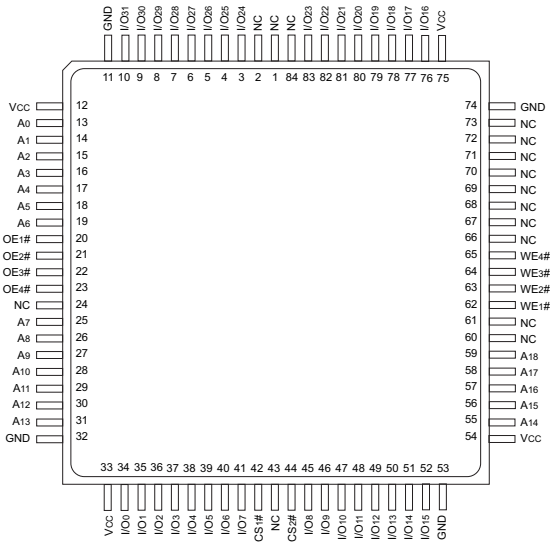
FEATURES

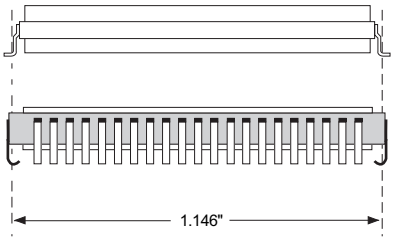
- Access Time of 70, 85, 100, 120ns
- 84 lead, 28mm CQFP, (Package 511)
- Organized as two banks of 512Kx32, User Configurable as 1Mx16 or 2Mx8
- Commercial, Industrial and Military Temperature Ranges
- TTL Compatible Inputs and Outputs
- 5V Power Supply
- Low Power CMOS
- Weight - WS1M32-XG3X - 20 grams typical

*This product is under development, is not qualified or characterized and is subject to change without notice.

PIN CONFIGURATION FOR WS1M32-XG3X

TOP VIEW

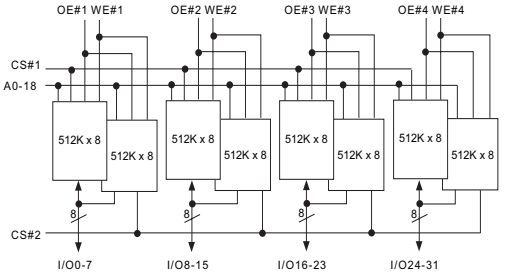




PIN DESCRIPTION

I/O0-31	Data Inputs/Outputs
A0-18	Address Inputs
WE1-4#	Write Enables
CS1-2#	Chip Selects
OE1-4#	Output Enables
V_{CC}	Power Supply
GND	Ground
NC	Not Connected

BLOCK DIAGRAM



Note: CS#1& CS#2 are used as bank select

The WEDC 84 lead G3 CQFP fills the same fit and function as the JEDEC 84 lead CQFJ or 84 PLCC. But the G3 has the TCE and lead inspection advantage of the CQFP form.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T_A	-40	+85	°C
Storage Temperature	T_{STG}	-65	+150	°C
Signal Voltage Relative to GND	V_G	-0.5	V_{CC} +0.5	V
Junction Temperature	T_J		150	°C
Supply Voltage	V_{CC}	-0.5	4.6	V

CAPACITANCE

T_A = +25°C

Parameter	Symbol	Conditions	Max	Unit
OE#1-4 capacitance	C_{OE}	V_{IN} = 0V, f = 1.0MHz	30	pF
WE#1-4 capacitance	C_{WE}	V_{IN} = 0V, f = 1.0MHz	30	pF
CS#1-2 capacitance	C_{CS}	V_{IN} = 0V, f = 1.0MHz	30	pF
Data I/O capacitance	$C_{I/O}$	$V_{I/O}$ = 0V, f = 1.0MHz	30	pF
Address input capacitance	C_{AD}	V_{IN} = 0V, f = 1.0MHz	100	pF

This parameter is guaranteed by design, but not tested.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	3.0	3.6	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	-0.3	+0.8	V
Operating Temperature (Ind.)	T_A	-40	+85	°C

TRUTH TABLE

CS1#	CS2#	OE#	WE#	Mode	Data I/O	Power
H	H	X	X	Standby	High Z	Standby
L	H	L	H	Read	Data Out	Active
L	H	H	H	Out Disable	High Z	Active
L	H	X	L	Write	Data In	Active
H	L	L	H	Read	Data Out	Active
H	L	H	H	Out Disable	High Z	Active
H	L	X	L	Write	Data In	Active
L	L	X	X	Invalid State	Invalid State	Invalid State

DC CHARACTERISTICS

V_{CC} = 3.3V ± 0.3V, -55°C ≤ T_A ≤ +125°C

Parameter	Symbol	Conditions	Min	Max	Units
Input Leakage Current	I_{LI}	V_{CC} = 5.5, V_{IN} = GND to V_{CC}		10	µA
Output Leakage Current	I_{LO}	CS# = V_{IH}, OE# = V_{IH}, V_{OUT} = GND to V_{CC}		10	µA
Operating Supply Current x 32 Mode	$I_{CC \times 32}$	CS# = V_{IL}, OE# = V_{IH}, f = 5MHz, V_{CC} = 5.5		220	mA
Standby Current	I_{SB}	CS# = V_{IH}, OE# = V_{IH}, f = 5MHz, V_{CC} = 5.5		10	mA
Standby Current (Low Power)	I_{SB2}	CS# = V_{IH}, OE# = V_{IH}, f = 5MHz, V_{CC} = 5.5		900	µA
Output Low Voltage	V_{OL}	I_{OL} = 8mA, V_{CC} = 4.5		0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4.0mA, V_{CC} = 4.5	2.4		V

NOTE: DC test conditions: V_{IH} = V_{CC} -0.3V, V_{IL} = 0.3V

AC CHARACTERISTICS

V_{CC} = 5.0V, GND = 0V, -55°C ≤ T_A ≤ +125°C

Parameter Read Cycle	Symbol	-70		-85		-100		-120		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	70		85		100		120		ns
Address Access Time	t_{AA}		70		85		100		120	ns
Output Hold from Address Change	t_{OH}	5		5		5		5		ns
Chip Select Access Time	t_{ACS}		70		85		100		120	ns
Output Enable to Output Valid	t_{OE}		35		40		50		60	ns
Chip Select to Output in Low Z	t_{CLZ}[1]	10		10		10		10		ns
Output Enable to Output in Low Z	t_{OLZ}[1]	5		5		5		5		ns
Chip Disable to Output in High Z	t_{CHZ}[1]		25		25		35		35	ns
Output Disable to Output in High Z	t_{OHZ}[1]		25		25		35		35	ns

1. This parameter is guaranteed by design but not tested.

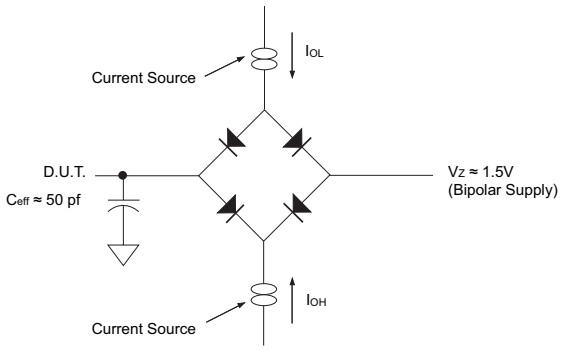
AC CHARACTERISTICS

V_{CC} = 5.0V, GND = 0V, -55°C ≤ T_A ≤ +125°C

Parameter Write Cycle	Symbol	-70		-85		-100		-120		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	70		85		100		120		ns
Chip Select to End of Write	t_{CW}	60		75		80		100		ns
Address Valid to End of Write	t_{AW}	60		75		80		100		ns
Data Valid to End of Write	t_{DW}	30		30		40		40		ns
Write Pulse Width	t_{WP}	50		50		60		60		ns
Address Setup Time	t_{AS}	0		0		0		0		ns
Address Hold Time	t_{AH}	5		5		5		5		ns
Output Active from End of Write	t_{OW}[1]	5		5		5		5		ns
Write Enable to Output in High Z	t_{WHZ}[1]		25		25		35		35	ns
Data Hold Time	t_{DH}	0		0		0		0		ns

1. This parameter is guaranteed by design but not tested.

AC TEST CIRCUIT

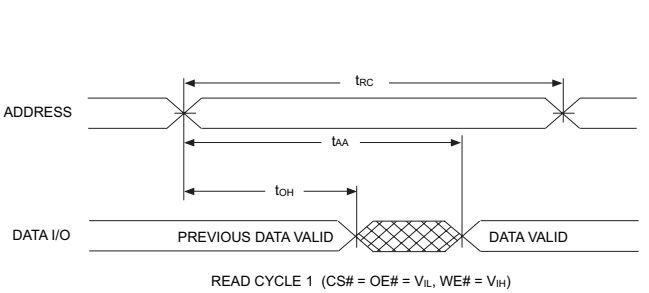


AC TEST CONDITIONS

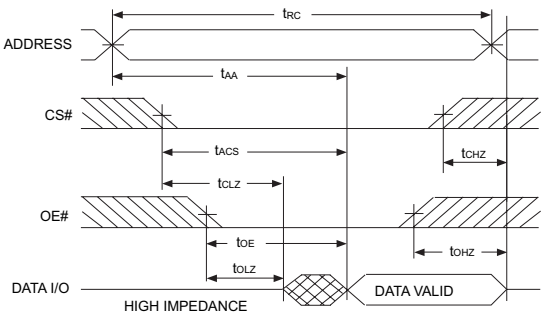
Parameter	Typ	Unit
Input Pulse Levels	V_{IL} = 0, V_{IH} = 3.0	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:
V_Z is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance Z0 = 75Ω.
V_Z is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.

TIMING WAVEFORM - READ CYCLE

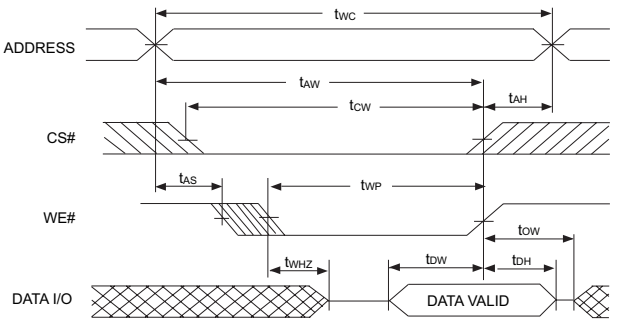


READ CYCLE 1 (CS# = OE# = V_{IL}, WE# = V_{IH})



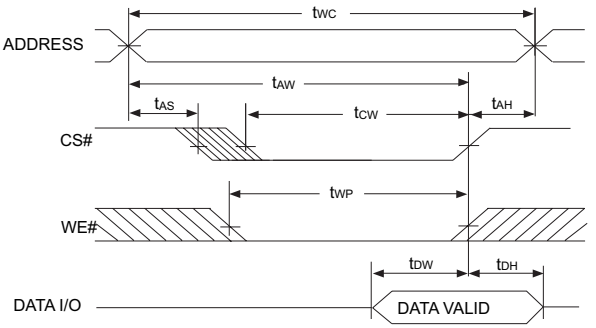
READ CYCLE 2 (WE# = V_{IH})

WRITE CYCLE - WE# CONTROLLED



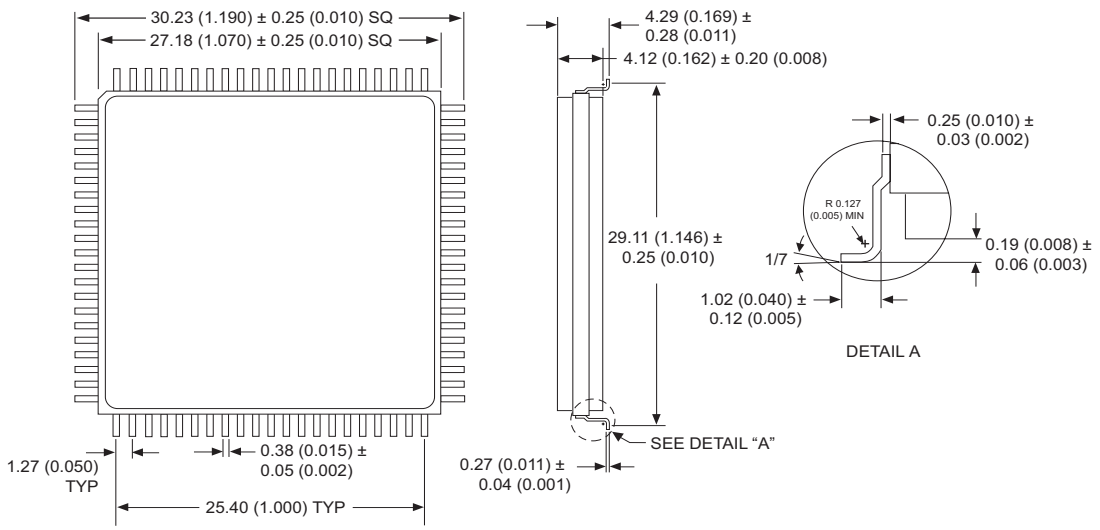
WRITE CYCLE 1, WE# CONTROLLED

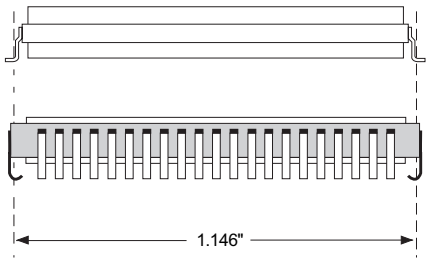
WRITE CYCLE - CS# CONTROLLED



WRITE CYCLE 2, CS# CONTROLLED

PACKAGE 511: 84 LEAD, CERAMIC QUAD FLAT PACK (G3)





The WEDC 84 lead G3 CQFP fills the same fit and function as the JEDEC 84 lead CQFJ or 84 PLCC. But the G3 has the TCE and lead inspection advantage of the CQFP form.

ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION