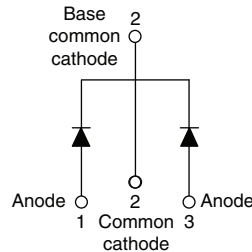


High Performance Schottky Generation 5.0, 2 x 15 A


TO-220AB

FEATURES

- 175 °C high performance Schottky diode
- Very low forward voltage drop
- Extremely low reverse leakage
- Optimized V_F vs. I_F trade off for high efficiency
- Increased ruggedness for reverse avalanche capability
- RBSOA available
- Negligible switching losses
- Submicron trench technology
- Full lead (Pb)-free and RoHS compliant devices
- Designed and qualified for industrial level


**RoHS
COMPLIANT**
PRODUCT SUMMARY

$I_{F(AV)}$	2 x 15 A
V_R	45 V
V_F at 15 A at 125 °C	0.54 A

APPLICATIONS

- High efficiency SMPS
- Automotive
- High frequency switching
- Output rectification
- Reverse battery protection
- Freewheeling
- Dc-to-dc systems
- Increased power density systems

MAJOR RATINGS AND CHARACTERISTICS

SYMBOL	CHARACTERISTICS	VALUES	UNITS
V_{RRM}		45	V
V_F	15 Apk, $T_J = 125$ °C (typical, per leg)	0.50	
T_J	Range	- 55 to 175	°C

VOLTAGE RATINGS

PARAMETER	SYMBOL	TEST CONDITIONS	30CTT045	UNITS
Maximum DC reverse voltage	V_R	$T_J = 25$ °C	45	V

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum average forward current <small>per leg</small> <small>per device</small>	$I_{F(AV)}$	50 % duty cycle at $T_C = 146$ °C, rectangular waveform	15	A
			30	
Maximum peak one cycle non-repetitive surge current per leg	I_{FSM}	5 μ s sine or 3 μ s rect. pulse	880	
		10 ms sine or 6 ms rect. pulse	220	
Non-repetitive avalanche energy per leg	E_{AS}	$T_J = 25$ °C, $I_{AS} = 5$ A, $L = 4.4$ mH	55	mJ
Repetitive avalanche current per leg	I_{AR}	Limited by frequency of operation and time pulse duration so that $T_J < T_J$ max. I_{AS} at T_J max. as a function of time pulse See fig. 8	I_{AS} at T_J max.	A

ELECTRICAL SPECIFICATIONS						
PARAMETER	SYMBOL	TEST CONDITIONS		TYP.	MAX.	UNITS
Forward voltage drop per leg	$V_{FM}^{(1)}$	15 A	$T_J = 25\text{ }^\circ\text{C}$	-	0.60	V
		30 A		-	0.72	
		15 A	$T_J = 125\text{ }^\circ\text{C}$	-	0.54	
		30 A		-	0.69	
Reverse leakage current per leg	$I_{RM}^{(1)}$	$T_J = 25\text{ }^\circ\text{C}$	$V_R = \text{Rated } V_R$	-	100	μA
		$T_J = 125\text{ }^\circ\text{C}$		-	8	mA
Junction capacitance per leg	C_T	$V_R = 5\text{ }V_{DC}$ (test signal range 100 kHz to 1 MHz) $25\text{ }^\circ\text{C}$		1020	-	pF
Series inductance per leg	L_S	Measured lead to lead 5 mm from package body		8.0	-	nH
Maximum voltage rate of change	dV/dt	Rated V_R		-	10 000	V/ μs

Note(1) Pulse width < 300 μs , duty cycle < 2 %

THERMAL - MECHANICAL SPECIFICATIONS				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum junction and storage temperature range	T_J, T_{Stg}		- 55 to 175	$^\circ\text{C}$
Maximum thermal resistance, junction to case per leg	R_{thJC}	DC operation	2.5	$^\circ\text{C/W}$
Maximum thermal resistance, junction to case per device			1.25	
Typical thermal resistance, case to heatsink	R_{thCS}	Mounting surface, smooth and greased	0.5	
Approximate weight			2	g
			0.07	oz.
Mounting torque	minimum		6 (5)	kgf · cm (lbf · in)
	maximum		12 (10)	
Marking device		Case style TO-220AB	30CTT045	

High Performance
Schottky Generation 5.0,
2 x 15 A

Vishay High Power Products

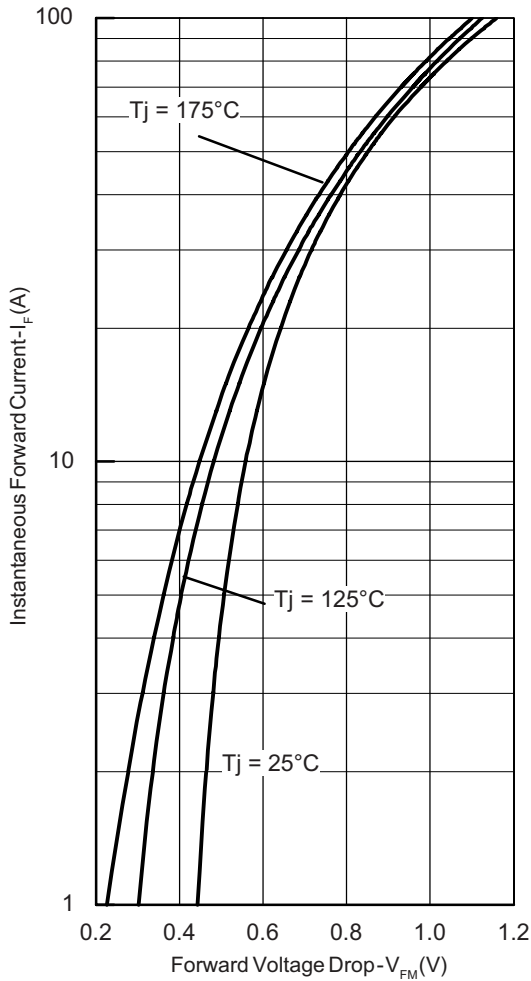


Fig. 1 - Maximum Forward Voltage Drop Characteristics

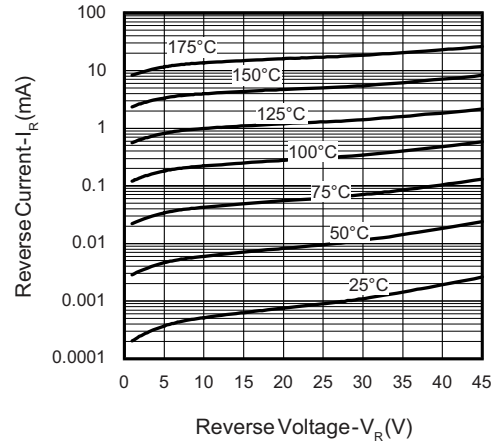


Fig. 2 - Typical Values of Reverse Current vs. Reverse Voltage

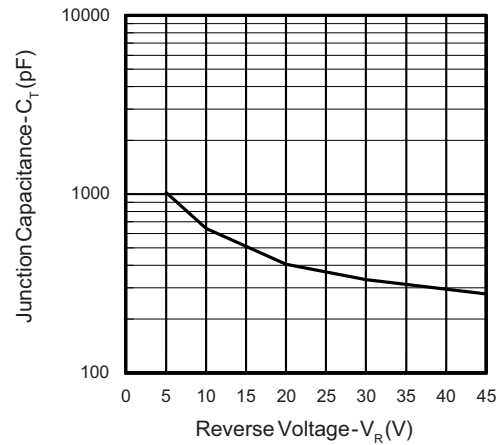


Fig. 3 - Typical Junction Capacitance vs. Reverse Voltage

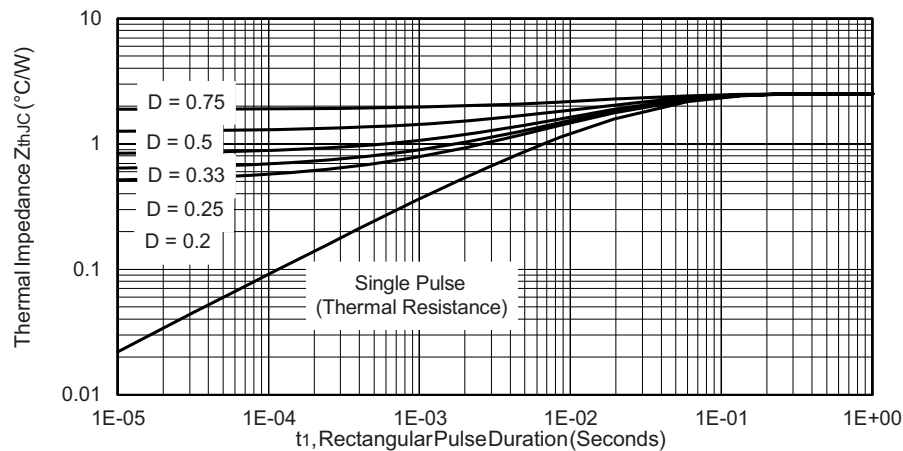


Fig. 4 - Maximum Thermal Impedance Z_{thJC} Characteristics

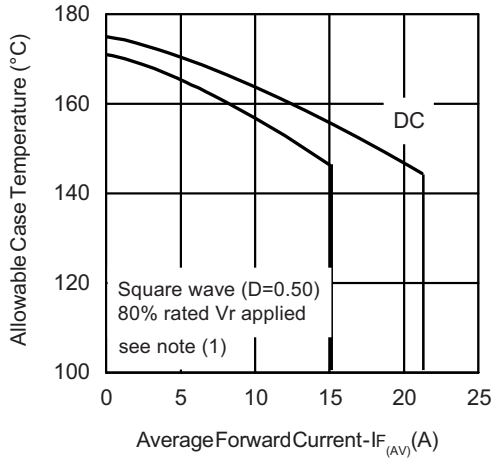


Fig. 5 - Maximum Allowable Case Temperature vs. Average Forward Current

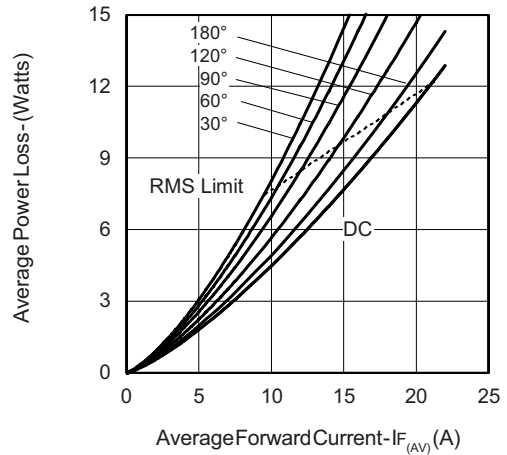


Fig. 6 - Forward Power Loss Characteristics

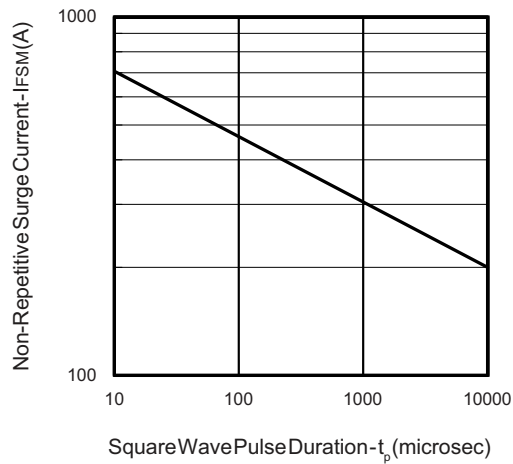


Fig. 7 - Maximum Non-Repetitive Surge Current

Note

- (1) Formula used: $T_C = T_J - (P_d + P_{d_{REV}}) \times R_{thJC}$;
 $P_d = \text{Forward power loss} = I_{F(AV)} \times V_{FM} \text{ at } (I_{F(AV)}/D)$ (see fig. 6);
 $P_{d_{REV}} = \text{Inverse power loss} = V_{R1} \times I_R (1 - D)$; I_R at $V_{R1} = 80\%$ rated V_R



High Performance Schottky Generation 5.0,
2 x 15 A Vishay High Power Products

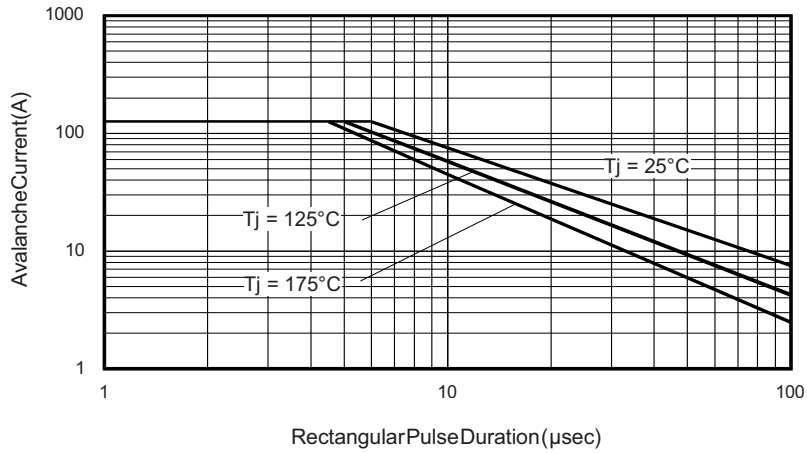


Fig. 8 - Reverse Bias Safe Operating Area (Avalanche Current vs. Rectangular Pulse Duration)

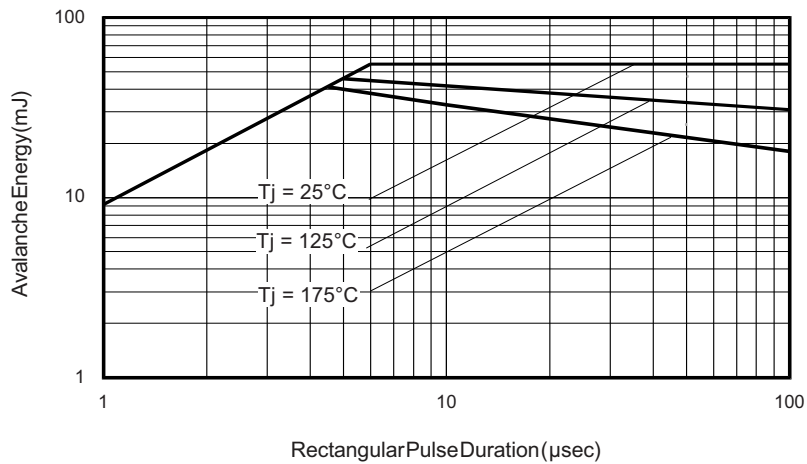
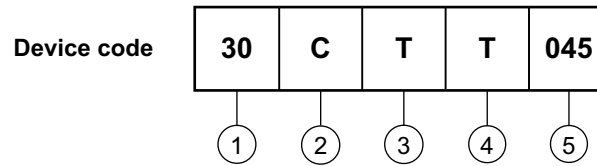


Fig. 9 - Reverse Bias Safe Operating Area (Avalanche Energy vs. Rectangular Pulse Duration)



ORDERING INFORMATION TABLE



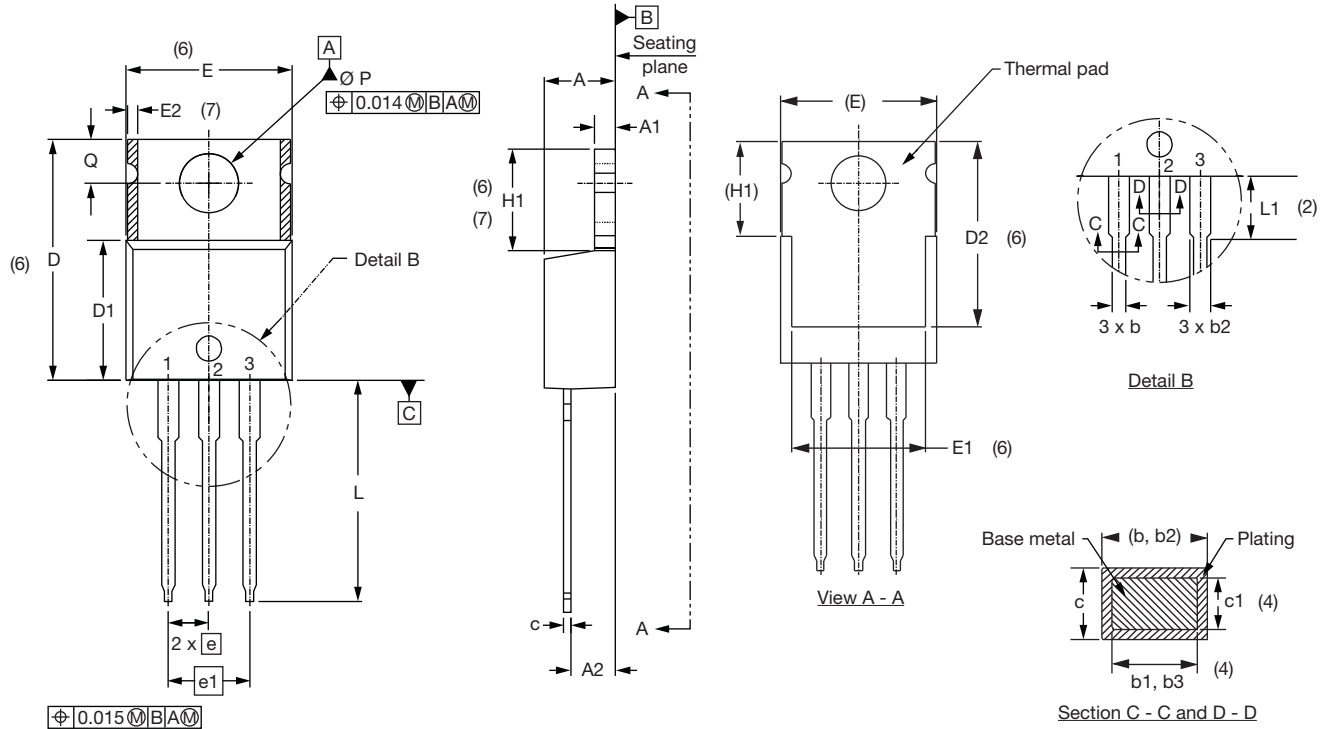
- 1** - Current rating (30 A)
- 2** - Circuit configuration:
C = Common cathode
- 3** - Package:
T = TO-220
- 4** - T = Trench
- 5** - Voltage code (45 V)

Tube standard pack quantity: 50 pieces

LINKS TO RELATED DOCUMENTS	
Dimensions	http://www.vishay.com/doc?95222
Part marking information	http://www.vishay.com/doc?95225

TO-220AB

DIMENSIONS in millimeters and inches



Lead assignments

Diodes

- 1. - Anode/open
- 2. - Cathode
- 3. - Anode

Conforms to JEDEC outline TO-220AB

SYMBOL	MILLIMETERS		INCHES		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	4.25	4.65	0.167	0.183	
A1	1.14	1.40	0.045	0.055	
A2	2.56	2.92	0.101	0.115	
b	0.69	1.01	0.027	0.040	
b1	0.38	0.97	0.015	0.038	4
b2	1.20	1.73	0.047	0.068	
b3	1.14	1.73	0.045	0.068	4
c	0.36	0.61	0.014	0.024	
c1	0.36	0.56	0.014	0.022	4
D	14.85	15.25	0.585	0.600	3
D1	8.38	9.02	0.330	0.355	
D2	11.68	12.88	0.460	0.507	6
E	10.11	10.51	0.398	0.414	3, 6
E1	6.86	8.89	0.270	0.350	6
E2	-	0.76	-	0.030	7
e	2.41	2.67	0.095	0.105	
e1	4.88	5.28	0.192	0.208	
H1	6.09	6.48	0.240	0.255	6, 7
L	13.52	14.02	0.532	0.552	
L1	3.32	3.82	0.131	0.150	2
Ø P	3.54	3.73	0.139	0.147	
Q	2.60	3.00	0.102	0.118	
θ	90° to 93°		90° to 93°		

Notes

- (1) Dimensioning and tolerancing as per ASME Y14.5M-1994
- (2) Lead dimension and finish uncontrolled in L1
- (3) Dimension D, D1 and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body
- (4) Dimension b1, b3 and c1 apply to base metal only
- (5) Controlling dimensions: inches
- (6) Thermal pad contour optional within dimensions E, H1, D2 and E1
- (7) Dimensions E2 x H1 define a zone where stamping and singulation irregularities are allowed
- (8) Outline conforms to JEDEC TO-220, except A2 (maximum) and D2 (minimum) where dimensions are derived from the actual package outline



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