*Advance information*

Features

- Organization: 1M×8
- Sector architecture
  - One 16K; two 8K; one 32K; and fifteen 64K byte sectors
  - Boot code sector architecture—T (top) or B (bottom)
  - Erase any combination of sectors or full chip
- Single 2.2-2.7V power supply for read/write operations
- Sector protection
- High speed 120/150/200 ns address access time
- Automated on-chip programming algorithm
  - Automatically programs/verifies data at specified address
- Automated on-chip erase algorithm
  - Automatically preprograms/erases chip or specified sectors
- 10,000 write/erase cycle endurance
- Hardware $\overline{RESET}$ pin
  - Resets internal state machine to read mode

- Low power consumption
  - 8 mA typical read current
  - 16 mA typical program current
  - <1 µA typical standby current
  - 1 µA typical automatic sleep mode current
- JEDEC standard software, packages and pinouts
  - 40-pin TSOP
- Detection of program/erase cycle completion
  - DQ7 $\overline{DATA}$ polling
  - DQ6 toggle bit
  - DQ2 toggle bit
  - RY/$\overline{BY}$ output
- Erase suspend/resume
  - Supports reading data from or programming data to a sector not being erased
- Low V_{CC} write lock-out

Logic block diagram
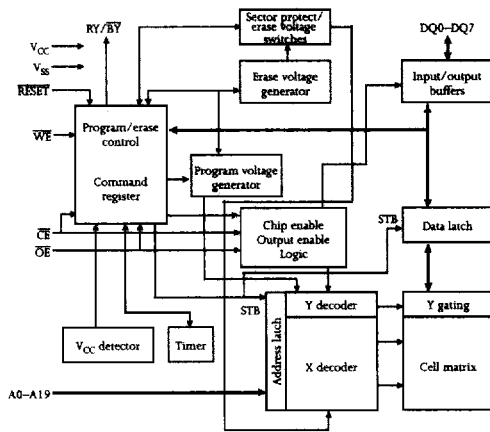
Pin arrangement

40-pin TSOP
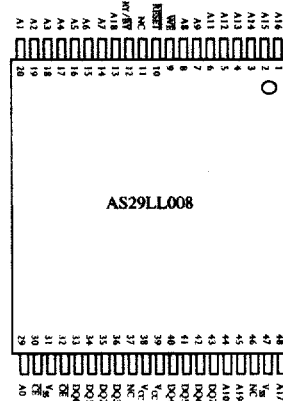
AS29LL008

Selection guide

		29LL008-120	29LL008-150	29LL008-200	Unit
Maximum access time	t_{AA}	120	150	200	ns
Maximum chip enable access time	t_{CE}	120	150	200	ns
Maximum output enable access time	t_{OE}	50	50	55	ns

Functional description

The AS29LL008 is an 8 megabit, 2.2-volt only Flash memory organized as 1 Megabyte of 8 bits each. For flexible erase and program capability, the 8 megabits of data is divided into nineteen sectors: one 16K, two 8K, one 32K, and fifteen 64k byte sectors. The ×8 data appears on DQ0–DQ7. The AS29LL008 is offered in a JEDEC standard 40-pin TSOP package. This device is designed to be programmed and erased in-system with a single 2.2V V_{CC} supply. The device can also be reprogrammed in standard EPROM programmers.

The AS29LL008 offers access times of 120/150/200 ns, allowing 0-wait state operation of high speed microprocessors. To eliminate bus contention the device has separate chip enable ($\overline{CE}$), write enable ($\overline{WE}$), and output enable ($\overline{OE}$) controls.

The AS29LL008 is fully compatible with the JEDEC single power supply Flash standard. Write commands to the command register using standard microprocessor write timings. An internal state-machine uses register contents to control the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Read data from the device in the same manner as other Flash or EPROM devices. Use the program command sequence to invoke the automated on-chip programming algorithm that automatically times the program pulse widths and verifies proper cell margin. Use the erase command sequence to invoke the automated on-chip erase algorithm that preprograms the sector if it is not already programmed before executing the erase operation, times the erase pulse widths, and verifies proper cell margin.

Boot sector architecture enables the system to boot from either the top (AS29LL008T) or the bottom (AS29LL008B) sector. Sector erase architecture allows specified sectors of memory to be erased and reprogrammed without altering data in other sectors. A sector typically erases and verifies within 1.5 seconds. Hardware sector protection disables both program and erase operations in all or any combination of the nineteen sectors. The device provides true background erase with Erase Suspend, which puts erase operations on hold to either read data from or program data to a sector that is not being erased. The chip erase command will automatically erase all unprotected sectors.

A factory shipped AS29LL008 is fully erased (all bits = 1). The programming operation sets bits to 0. Data is programmed into the array one byte at a time in any sequence and across sector boundaries. A sector must be erased to change bits from 0 to 1. Erase returns all bytes in a sector to the erased state (all bits = 1). Each sector is erased individually with no effect on other sectors.

The device features single 2.2V power supply operation for read, write, and erase functions. Internally generated and regulated voltages are provided for the program and erase operations. A low V_{CC} detector automatically inhibits write operations during power transitions. The RY/$\overline{BY}$ pin, $\overline{DATA}$ polling of DQ7, or toggle bit (DQ6) may be used to detect end of program or erase operations. The device automatically resets to the read mode after program/erase operations are completed. DQ2 indicates which sectors are being erased.

The AS29LL008 resists accidental erasure or spurious programming signals resulting from power transitions. Control register architecture permits alteration of memory contents only after successful completion of specific command sequences. During power up, the device is set to read mode with all program/erase commands disabled when V_{CC} is less than V_{LKO} (lockout voltage). The command registers are not affected by noise pulses of less than 5 ns on $\overline{OE}$, $\overline{CE}$, or $\overline{WE}$. To initiate write commands, $\overline{CE}$ and $\overline{WE}$ must be logical zero and $\overline{OE}$ a logical one.

When the device's hardware $\overline{RESET}$ pin is driven low, any program/erase operation in progress will be terminated and the internal state machine will be reset to read mode. If the $\overline{RESET}$ pin is tied to the system reset circuitry and a system reset occurs during an automated on-chip program/erase algorithm, data in address locations being operated on will become corrupted and require rewriting. Resetting the device enables the system's microprocessor to read boot-up firmware from the Flash memory.

The AS29LL008 uses Fowler-Nordheim tunnelling to electrically erase all bits within a sector simultaneously. Bytes/words are programmed one at a time using EPROM programming mechanism of hot electron injection.