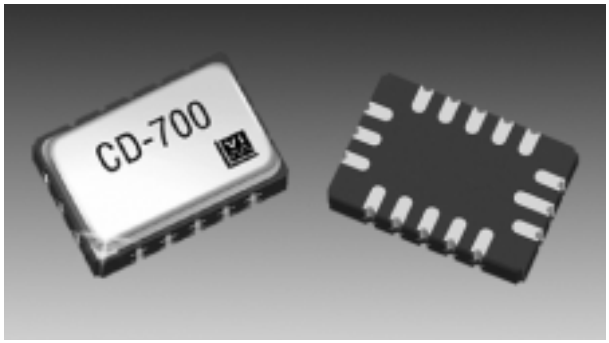
CD-700



Description:

Vectron's CD-700 is a user-configurable crystal based PLL integrated circuit. It includes a digital phase detector, op-amp, VCXO and additional integrated functions for use in digital synchronization applications

Features:

- **5 x 7.5mm, smallest VCXO PLL available**
- **Output Frequencies to 65.536 MHz**
- **5 or 3.3 Vdc operation**
- **Tri-state Output**
- **Loss of Signal Alarm**
- **VCXO with CMOS outputs**
- **0/70 or -40/85°C temperature range**
- **Hermetically sealed ceramic SMD package**

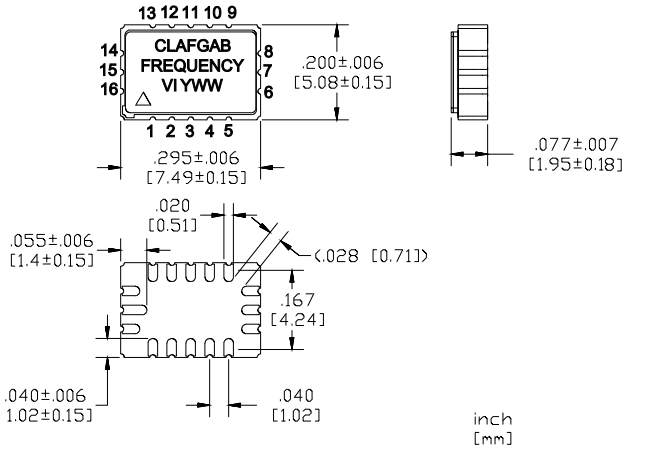
Performance Characteristics

Parameter	Symbol	Min.	Typical	Max	Unit
Output Frequency: (ordering option) Out 1, 5V option Out 1, 3.3V option		 12.000 12.000		 65.536 51.840	 MHz MHz
Supply Voltage[1]: +5.0 +3.3	V_{DD}	 4.5 3.0	 5.0 3.3	 5.5 3.3	 V V
Supply Current:	I_{DD}			63	mA
Output Logic Levels: Output Logic High Output Logic Low	 V_{OH} V_{OL}	 2.5		 0.5	 V V
Output Transition Times: Rise Time[2] Fall Time[2]	 t_R t_F			 5 5	 ns ns
Input Logic Levels: Input Logic High[2] Input Logic Low[2]	 V_{IH} V_{OL}	 2.0		 0.5	 V V
Nominal Frequency on Loss of Signal Output 1 Output 2				 ±75 ±75	 ppm ppm
Symmetry or Duty Cycle[2] Out 1 Out 2 RCLK	 SYM1 SYM2 RCLK	 40 45 40		 60 55 60	 % % %
Absolute Pull Range (ordering option) over operating temp, aging, p.s. variations	APR	±50, ±80, ±100			ppm
Test Conditions for APR (+5V option)	V_C	0.5		4.5	V
Test Conditions for APR (+3.3V option)	V_C	0.3		3.0	V
Transfer Function		Positive			
Phase Detector Gain +5.0V option +3.3V option		 0.53 0.35			 rad/V rad/V
Operating temperature (ordering option)			0/70 or -40/85		°C
Control Voltage Leakage Current	I_{VCXO}			±1	uA

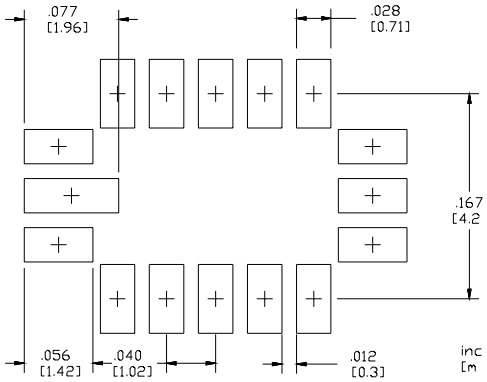
1. A 0.01 uF capacitor should be located as close to the supply as possible (to ground) and a 0.1 uF is also recommended.
2. Symmetry is defined as (ON TIME/PERIOD) with V_S = 1.4V for both 5V and 3.3V operation.

CD-700

Outline Drawing



Pad Layout



Pin Out Information

Pin	Symbol	Function
1	OPOUT	Op-Amp Output
2	OPN	Op-Amp Negative Input
3	PHO	Phase detector output
4	LOSIN	Loss of signal input
5	DATAIN	Phase detector Input signal
6	CLKIN	Phase detector Clock signal
7	GND	Cover and Electrical Ground
8	LOS	Loss of signal indicator
9	RCLK	Recovered Clock
10	RDATA	Recovered Data
11	Output 2	Divided-down VCXO Output, or No Output
12	HIZ	INPUT (This Tri-states the outputs)
13	Output 1	VCXO Output
14	V_{DD}	Power Supply Voltage (3.3V ±10% or 5.0V ±10%)
15	OPP	Op-Amp Positive Input
16	V_C	VCXO Control Voltage

Standard Frequencies (MHz)

12.000	12.288	12.352	16.000	16.384
19.440	24.576	24.704	24.960	25.000
27.000	30.000	30.720	32.768	34.368
35.328	38.880	39.3216	40.000	40.960
44.736	51.840	54.000	60.000	62.208
62.500	65.536			

Consult datasheet on website.

CDR

Ordering Information

CD – 700 – L A F – G A B – 44.736 MHz

Product Family
CD = Clock and Data

Package
700 = 16 pin SMD

Input
K = 5.0 Vdc ±10%
L = 3.3 Vdc ±10%

Output
A = CMOS

Temperature Range
C = 0ºC to +70ºC
F = -40ºC to +85ºC

Absolute Pull Range
G = ±50 ppm
N = ±80 ppm
H = ±100 ppm

Divide By
A = 2 **F** = 64
B = 4 **G** = 128
C = 8 **H** = 256
D = 16 **K** = Disable
E = 32

Duty Cycle
B = 50/50 ±10% (Out 1)

Frequency
12.000 MHz to 65.536 MHz