CYPRESS

PRELIMINARY

CY7C178
CY7C179

32K x 18 Synchronous Cache RAM

Features

- **Supports 66-MHz Pentium™ microprocessor cache systems with zero wait states**
- **32K by 18 common I/O**
- **Fast clock-to-output times**
  - **— 8.5 ns**
- **Two-bit wraparound counter supporting Pentium and 486 burst sequence (CY7C178)**
- **Two-bit wraparound counter supporting linear burst sequence (CY7C179)**
- **Separate processor and controller address strobes**
- **Synchronous self-timed write**
- **Direct interface with the processor and external cache controller**
- **Asynchronous output enable**
- **I/Os capable of 3.3V operation**
- **Industry-standard pinout**
- **52-pin PLCC and PQFP**

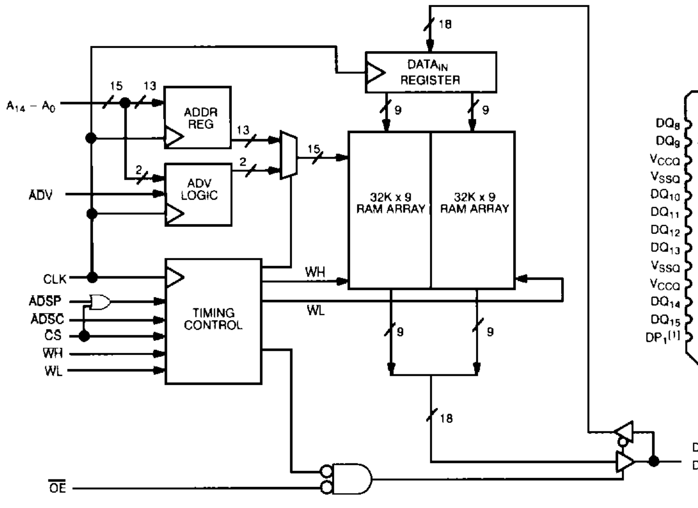
Functional Description

The CY7C178 and CY7C179 are 32K by 18 synchronous cache RAMs designed to interface with high-speed microprocessors with minimum glue logic. Maximum access delay from clock rise is 8.5 ns. A 2-bit on-chip counter captures the first address in a burst and increments the address automatically for the rest of the burst access.

The CY7C178 is designed for Intel Pentium and i486 CPU-based systems; its counter follows the burst sequence of the Pentium and the i486 processors. The CY7C179 is architected for processors with linear burst sequences. Burst accesses can be initiated with the processor address strobe ($\overline{ADSP}$) or the cache controller address strobe ($\overline{ADSC}$) inputs. Address advancement is controlled by the address advancement ($\overline{ADV}$) input.

A synchronous self-timed write mechanism is provided to simplify the write interface. A synchronous chip select input and an asynchronous output enable input provide easy control for bank selection and output three-state control.

Logic Block Diagram



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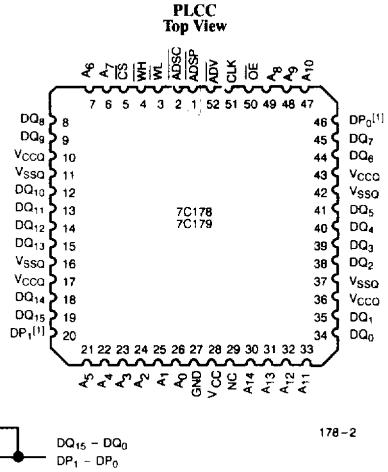
Pin Configuration



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Selector Guide

		7C178–8 7C179–8	7C178–10 7C179–10	7C178–12 7C179–12
Maximum Access Time (ns)		8.5	10.5	12.5
Maximum Operating Current (mA)	Commercial	225	210	180
	Military			270

Shaded area contains advanced information.

Note:

1. DP_0 and DP_1 are functionally equivalent to DQ_x.

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Functional Description (continued)

Single Write Accesses Initiated by $\overline{\text{ADSP}}$

This access is initiated when the following conditions are satisfied at clock rise: (1) $\overline{\text{CS}}$ is LOW and (2) $\overline{\text{ADSP}}$ is LOW. $\overline{\text{ADSP}}$-triggered write cycles are completed in two clock periods. The address at A_0 through A_{14} is loaded into the address register and address advancement logic and delivered to the RAM core. The write signal is ignored in this cycle because the cache tag or other external logic uses this clock period to perform address comparisons or protection checks. If the write is allowed to proceed, the write input to the CY7C178 and CY7C179 will be pulled LOW before the next clock rise. $\overline{\text{ADSP}}$ is ignored if $\overline{\text{CS}}$ is HIGH.

If $\overline{\text{WH}}$, $\overline{\text{WL}}$, or both are LOW at the next clock rise, information presented at $DQ_0 - DQ_{15}$ and $DP_0 - DP_1$ will be written into the location specified by the address advancement logic. $\overline{\text{WL}}$ controls the writing of $DQ_0 - DQ_7$ and DP_0 while $\overline{\text{WH}}$ controls the writing of $DQ_8 - DQ_{15}$ and DP_1. Because the CY7C178 and CY7C179 are common-I/O devices, the output enable signal ($\overline{\text{OE}}$) must be deasserted before data from the CPU is delivered to $DQ_0 - DQ_{15}$ and $DP_0 - DP_1$. As a safety precaution, the appropriate data lines are three-stated in the cycle where $\overline{\text{WH}}$, $\overline{\text{WL}}$, or both are sampled LOW, regardless of the state of the $\overline{\text{OE}}$ input.

Single Write Accesses Initiated by $\overline{\text{ADSC}}$

This write access is initiated when the following conditions are satisfied at rising edge of the clock: (1) $\overline{\text{CS}}$ is LOW, (2) $\overline{\text{ADSC}}$ is LOW, and (3) $\overline{\text{WH}}$ or $\overline{\text{WL}}$ are LOW. $\overline{\text{ADSC}}$ triggered accesses are completed in a single clock cycle.

The address at A_0 through A_{14} is loaded into the address register and address advancement logic and delivered to the RAM core. Information presented at $DQ_0 - DQ_{15}$ and $DP_0 - DP_1$ will be written into the location specified by the address advancement logic. Since the CY7C178 and the CY7C179 are common-I/O devices, the output enable signal ($\overline{\text{OE}}$) must be deasserted before data from the cache controller is delivered to the data and parity lines. As a safety precaution, the appropriate data and parity lines are three-stated in the cycle where $\overline{\text{WH}}$ and $\overline{\text{WL}}$ are sampled LOW regardless of the state of the $\overline{\text{OE}}$ input.

Single Read Accesses

A single read access is initiated when the following conditions are satisfied at clock rise: (1) $\overline{\text{CS}}$ is LOW, (2) $\overline{\text{ADSP}}$ or $\overline{\text{ADSC}}$ is LOW, and (3) $\overline{\text{WH}}$ and $\overline{\text{WL}}$ are HIGH. The address at A_0 through A_{14} is stored into the address advancement logic and delivered to the RAM core. If the output enable ($\overline{\text{OE}}$) signal is asserted (LOW), data will be available at the data outputs a maximum of 8.5 ns after clock rise. $\overline{\text{ADSP}}$ is ignored if $\overline{\text{CS}}$ is HIGH.

Burst Sequences

The CY7C178 provides a 2-bit wraparound counter, fed by pins $A_0 - A_1$, that implements the 486 and Pentium processor's address burst sequence (see *Table 1*). Note that the burst sequence depends on the first burst address.

Table 1. Counter Implementation for the Intel Pentium/486 Processor's Sequence

First Address	Second Address	Third Address	Fourth Address
A_{X+1}, A_X	A_{X+1}, A_X	A_{X+1}, A_X	A_{X+1}, A_X
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

The CY7C179 provides a two-bit wraparound counter, fed by pins $A_0 - A_1$, that implements a linear address burst sequence (see *Table 2*).

Table 2. Counter Implementation for a Linear Sequence

First Address	Second Address	Third Address	Fourth Address
A_{X+1}, A_X	A_{X+1}, A_X	A_{X+1}, A_X	A_{X+1}, A_X
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

Application Example

Figure 1 shows a 256-Kbyte secondary cache for the Pentium microprocessor using four CY7C178 cache RAMs.

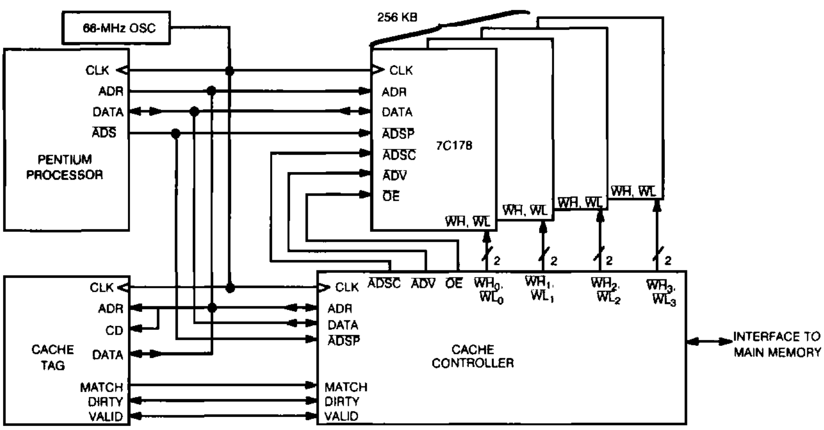

Figure 1. Cache Using Four CY7C178s

Pin Definitions

Signal Name	Type	# of Pins	Description
V_{CC}	Input	1	+5V Power
V_{CCQ}	Input	4	+5V or 3.3V (Outputs)
GND	Input	1	Ground
V_{SSQ}	Input	4	Ground (Outputs)
CLK	Input	1	Clock
$A_{14} - A_0$	Input	15	Address
$\overline{ADSP}$	Input	1	Address Strobe from Processor
$\overline{ADSC}$	Input	1	Address Strobe from Cache Controller
$\overline{WH}$	Input	1	Write Enable – High Byte
$\overline{WL}$	Input	1	Write Enable – Low Byte
$\overline{ADV}$	Input	1	Advance
$\overline{OE}$	Input	1	Output Enable
$\overline{CS}$	Input	1	Chip Select
$DQ_{15}-DQ_0$	Input/Output	16	Regular Data
DP_1-DP_0	Input/Output	2	Parity Data

Pin Descriptions

Signal Name	I/O	Description
Input Signals		
CLK	I	Clock signal. It is used to capture the address, the data to be written, and the following control signals: $\overline{ADSP}$, $\overline{ADSC}$, $\overline{CS}$, $\overline{WH}$, $\overline{WL}$, and $\overline{ADV}$. It is also used to advance the on-chip auto-address-increment logic (when the appropriate control signals have been set).
A_{14}–A_0	I	Fifteen address lines used to select one of 32K locations. They are captured in an on-chip register on the rising edge of CLK if $\overline{ADSP}$ or $\overline{ADSC}$ is LOW. The rising edge of the clock also loads the lower two address lines, $A_1 - A_0$, into the on-chip auto-address-increment logic if $\overline{ADSP}$ or $\overline{ADSC}$ is LOW.
$\overline{ADSP}$	I	Address strobe from processor. This signal is sampled at the rising edge of CLK. When this input and/or $\overline{ADSC}$ is asserted, $A_0 - A_{14}$ will be captured in the on-chip address register. It also allows the lower two address bits to be loaded into the on-chip auto-address-increment logic. If both $\overline{ADSP}$ and $\overline{ADSC}$ are asserted at the rising edge of CLK, only $\overline{ADSP}$ will be recognized. The $\overline{ADSP}$ input should be connected to the $\overline{ADS}$ output of the processor. $\overline{ADSP}$ is ignored when $\overline{CS}$ is HIGH.
$\overline{ADSC}$	I	Address strobe from cache controller. This signal is sampled at the rising edge of CLK. When this input and/or $\overline{ADSP}$ is asserted, $A_0 - A_{14}$ will be captured in the on-chip address register. It also allows the lower two address bits to be loaded into the on-chip auto-address-increment logic. The $\overline{ADSC}$ input should *not* be connected to the $\overline{ADS}$ output of the processor.
$\overline{WH}$	I	Write signal for the high-order half of the RAM array. This signal is sampled by the rising edge of CLK. If $\overline{WH}$ is sampled as LOW, i.e., asserted, the control logic will perform a self-timed write of $DQ_{15} - DQ_8$ and DP_1 from the on-chip data register into the selected RAM location. There is one exception to this. If $\overline{ADSP}$, $\overline{WH}$, and $\overline{CS}$ are asserted (LOW) at the rising edge of CLK, the write signal, $\overline{WH}$, is ignored. Note that $\overline{ADSP}$ has no effect on $\overline{WH}$ if $\overline{CS}$ is HIGH.
$\overline{WL}$	I	Write signal for the low-order half of the RAM array. This signal is sampled by the rising edge of CLK. If $\overline{WL}$ is sampled as LOW, i.e., asserted, the control logic will perform a self-timed write of $DQ_7 - DQ_0$ and DP_0 from the on-chip data register into the selected RAM location. There is one exception to this. If $\overline{ADSP}$, $\overline{WL}$, and $\overline{CS}$ are asserted (LOW) at the rising edge of CLK, the write signal, $\overline{WL}$, is ignored. Note that $\overline{ADSP}$ has no effect of $\overline{WL}$ if $\overline{CS}$ is HIGH.
$\overline{ADV}$	I	Advance. This signal is sampled by the rising edge of CLK. When it is asserted, it automatically increments the 2-bit on-chip auto-address-increment counter. In the CY7C179, the address will be incremented linearly. In the CY7C178, the address will be incremented according to the Pentium/486 burst sequence. This signal is ignored if $\overline{ADSP}$ or $\overline{ADSC}$ is asserted concurrently with $\overline{CS}$.. Note that $\overline{ADSP}$ has no effect on $\overline{ADV}$ if $\overline{CS}$ is HIGH.
$\overline{CS}$	I	Chip select. This signal is sampled by the rising edge of CLK. If $\overline{CS}$ is HIGH and $\overline{ADSC}$ is LOW, the SRAM is deselected. If $\overline{CS}$ is LOW and $\overline{ADSC}$ or $\overline{ADSP}$ is LOW, a new address is captured by the address register. If $\overline{CS}$ is HIGH, $\overline{ADSP}$ is ignored.

Pin Descriptions (continued)

Signal Name	I/O	Description
$\overline{OE}$	I	Output enable. This signal is an asynchronous input that controls the direction of the data I/O pins. If $\overline{OE}$ is asserted (LOW), the data pins are outputs, and the SRAM can be read (as long as $\overline{CS}$ was asserted when it was sampled at the beginning of the cycle). If $\overline{OE}$ is deasserted (HIGH), the data I/O pins will be three-stated, functioning as inputs, and the SRAM can be written.

Bidirectional Signals

Signal Name	I/O	Description
DQ_{15}–DQ_0	I/O	Sixteen bidirectional data I/O lines. DQ_{15} – DQ_8 are inputs to and outputs from the high-order half of the RAM array, while DQ_7 – DQ_0 are inputs to and outputs from the low-order half of the RAM array. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they carry the data read from the selected location in the RAM array. The direction of the data pins is controlled by $\overline{OE}$: when $\overline{OE}$ is high, the data pins are three-stated and can be used as inputs; when $\overline{OE}$ is low, the data pins are driven by the output buffers and are outputs. DQ_{15} – DQ_8 and DQ_7 – DQ_0 are also three-stated when $\overline{WH}$ and $\overline{WL}$, respectively, is sampled LOW at clock rise.
DP_1–DP_0	I/O	Two bidirectional data I/O lines. These operate in exactly the same manner as DQ_{15} – DQ_0, but are named differently because their primary purpose is to store parity bits, while the DQs' primary purpose is to store ordinary data bits. DP_1 is an input to and an output from the high-order half of the RAM array, while DP_0 is an input to and an output from the lower-order half of the RAM array.

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Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with Power Applied .... −55°C to +125°C

Supply Voltage on V_{CC} Relative to GND .... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State[2] .... −0.5V to V_{CC} + 0.5V

DC Input Voltage[2] .... −0.5V to V_{CC} + 0.5V

Current into Outputs (LOW) .... 20 mA

Static Discharge Voltage .... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current .... >200 mA

Operating Range

Range	Ambient Temperature[3]	V_{CC}	V_{CCQ}
Com'l	0°C to +70°C	5V ± 5%	3.0V to V_{CC}
Mil	−55°C to +125°C	5V ± 5%	5V ± 5%

Electrical Characteristics Over the Operating Range[4]

Parameter	Description	Test Conditions	7C178−8 7C179−8 Min.	Max.	7C178−10 7C179−10 Min.	Max.	7C178−12 7C179−12 Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA	2.4	V_{CCQ}	2.4	V_{CCQ}	2.4	V_{CCQ}	V
V_{OL}	Output LOW Voltage	V_{CC} = Min, I_{OL}=8.0 mA		0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC} +0.3V	2.2	V_{CC} +0.3V	2.2	V_{CC} +0.3V	V
V_{IL}	Input LOW Voltage[2]		−0.3	0.8	−0.3	0.8	−0.3	0.8	V
I_X	Input Load Current	GND ≤ V_I ≤ V_{CC}	−1	1	−1	1	−1	1	μA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled	−5	5	−5	5	−5	5	μA

Notes:

2. Minimum voltage equals −2.0V for pulse durations of less than 20 ns.
3. T_A is the "instant on" case temperature.
4. See the last page for Group A subgroup testing information.

Electrical Characteristics Over the Operating Range (continued)[4]

Parameter	Description	Test Conditions		7C178-8 7C179-8 Min.	Max.	7C178-10 7C179-10 Min.	Max.	7C178-12 7C179-12 Min.	Max.	Unit
I_{OS}	Output Short Circuit Current[5]	V_{CC}=Max., V_{OUT}=GND			−300		−300		−300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC}=Max., Iout=0mA, f=f_{MAX} =1/t_{RC}	Com'l		225		210		190	mA
			Mil						270	
I_{SB1}	Automatic CE Power-Down Current−TTL Inputs	Max. V_{CC}, $\overline{CS} \geq V_{IH}$, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, f=f_{MAX}	Com'l		50		40		30	mA
			Mil						50	
I_{SB2}	Automatic CE Power-Down Current−CMOS Inputs	Max. V_{CC}, $\overline{CS} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$, f=0[6]	Com'l		20		20		20	mA
			Mil						20	

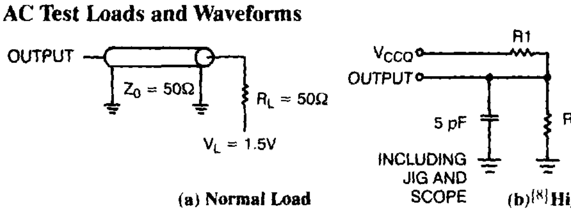
Shaded areas contain advanced information

Capacitance[7]

Parameter	Description	Test Conditions		Max.	Unit
C_{IN}: Addresses	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	Com'l	4.5	pF
			Mil	6	
C_{IN}: Other Inputs			Com'l	5	pF
			Mil	8	
C_{OUT}	Output Capacitance		Com'l	8	pF
			Mil	10	

Shaded areas contain advanced information

AC Test Loads and Waveforms



(a) Normal Load (b)[8] High-Z Load

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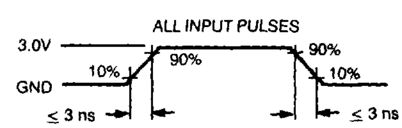

178-4

Notes:

5. Not more than one output should be shortened at one time. Duration of the short circuit should not exceed 30 seconds.
6. Inputs are disabled, clock signal allowed to run at speed.
7. Tested initially and after any design or process changes that may affect these parameters.
8. Resistor values for V_{CCO}=5V are: R1=481Ω and R2=255Ω. Resistor values for V_{CCO}=3.3V are R1=1179Ω and R2=868Ω

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Switching Characteristics Over the Operating Range[9]

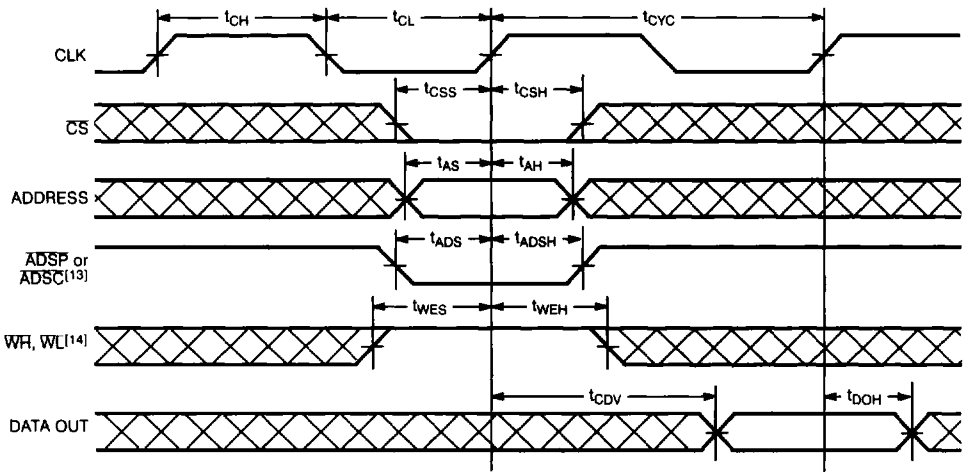
Parameter	Description	7C178−8 7C179−8 Min.	7C178−8 7C179−8 Max.	7C178−10 7C179−10 Min.	7C178−10 7C179−10 Max.	7C178−12 7C179−12 Min.	7C178−12 7C179−12 Max.	Unit
t_{CYC}	Clock Cycle Time	12.5		15		20		ns
t_{CH}	Clock HIGH	5		6		8		ns
t_{CL}	Clock LOW	5		6		8		ns
t_{AS}	Address Set-Up Before CLK Rise	2.5		2.5		2.5		ns
t_{AH}	Address Hold After CLK Rise	0.5		0.5		0.5		ns
t_{CDV}	Data Output Valid After CLK Rise		8.5		10		12	ns
t_{DOH}	Data Output Hold After CLK Rise	3		3		3		ns
t_{ADS}	$\overline{ADSP}$, $\overline{ADSC}$ Set-Up Before CLK Rise	2.5		2.5		2.5		ns
t_{ADSH}	$\overline{ADSP}$, $\overline{ADSC}$ Hold After CLK Rise	0.5		0.5		0.5		ns
t_{WES}	$\overline{WH}$, $\overline{WL}$ Set-Up Before CLK Rise	2.5		2.5		2.5		ns
t_{WEH}	$\overline{WH}$, $\overline{WL}$ Hold After CLK Rise	0.5		0.5		0.5		ns
t_{ADVS}	$\overline{ADV}$ Set-Up Before CLK Rise	2.5		2.5		2.5		ns
t_{ADVH}	$\overline{ADV}$ Hold After CLK Rise	0.5		0.5		0.5		ns
t_{DS}	Data Input Set-Up Before CLK Rise	2.5		2.5		2.5		ns
t_{DH}	Data Input Hold After CLK Rise	0.5		0.5		0.5		ns
t_{CSS}	Chip Select Set-Up	2.5		2.5		2.5		ns
t_{CSH}	Chip Select Hold After CLK Rise	0.5		0.5		0.5		ns
t_{CSOZ}	Chip Select Sampled to Output High Z[10]	2	6	2	6	2	7	ns
t_{EOZ}	$\overline{OE}$ HIGH to Output High Z[10]	2	6	2	6	2	7	ns
t_{EOV}	$\overline{OE}$ LOW to Output Valid		5		5		6	ns
t_{WEOZ}	$\overline{WH}$ or $\overline{WL}$ Sampled LOW to Output High Z[10, 11]		5		6		7	ns
t_{WEOV}	$\overline{WH}$ or $\overline{WL}$ Sampled HIGH to Output Valid[11]		8.5		10		12	ns

Notes:

9. Unless otherwise noted, test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and load capacitance. Shown in Figure (a) and (b) of AC Test Loads.
10. t_{CSOZ}, t_{EOZ}, and t_{WEOZ} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady state voltage.
11. At any given voltage and temperature, t_{WEOZ} min. is less than t_{WEOV} min.

Switching Waveforms

Single Read[12]



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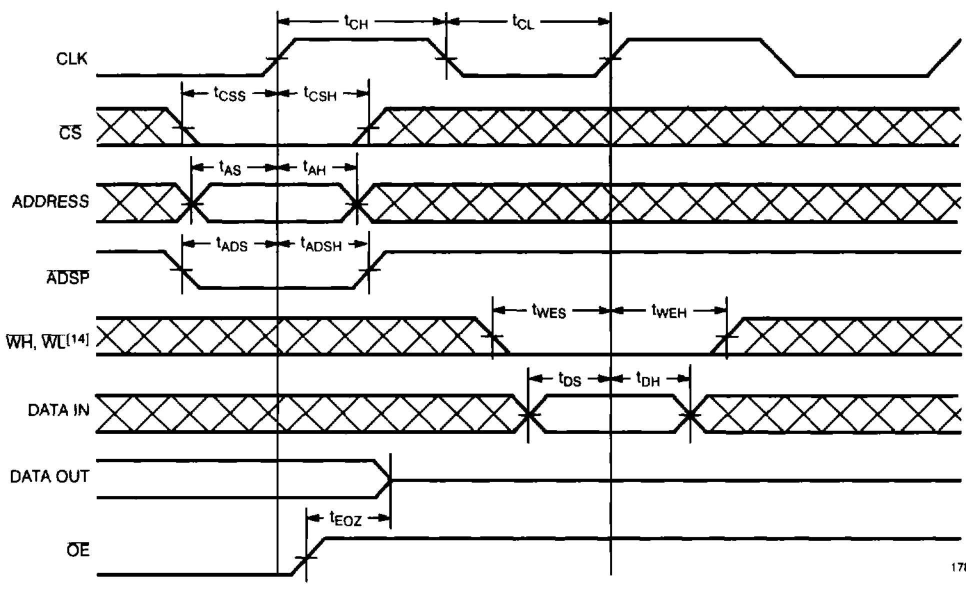
Single Write Timing: Write Initiated by ADSP



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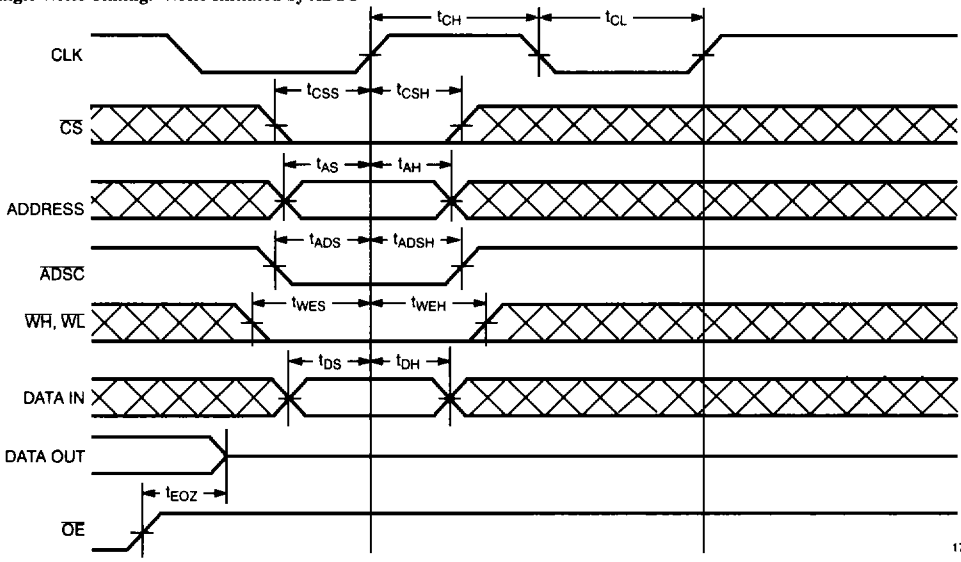
Notes:

12. OE is LOW throughout this operation.
13. If ADSP is asserted while CS is HIGH, ADSP will be ignored.
14. ADSP has no effect on ADV, WH, and WL if CS is HIGH.

Switching Waveforms (continued)

Single Write Timing: Write Initiated by $\overline{ADSC}$



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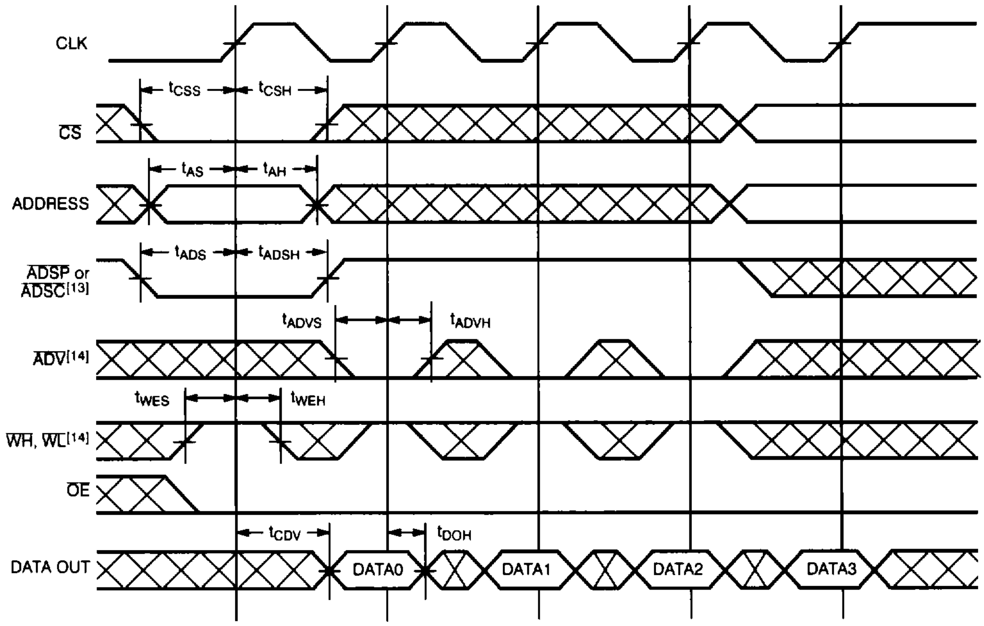
Burst Read Sequence with Four Accesses



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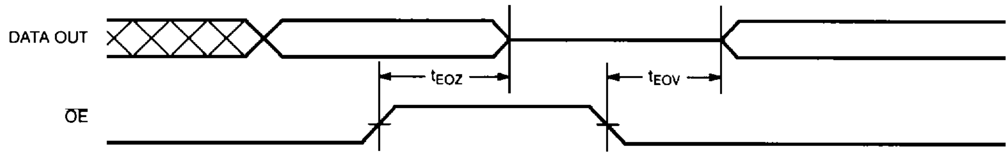
Switching Waveforms (continued)

Output (Controlled by $\overline{OE}$)



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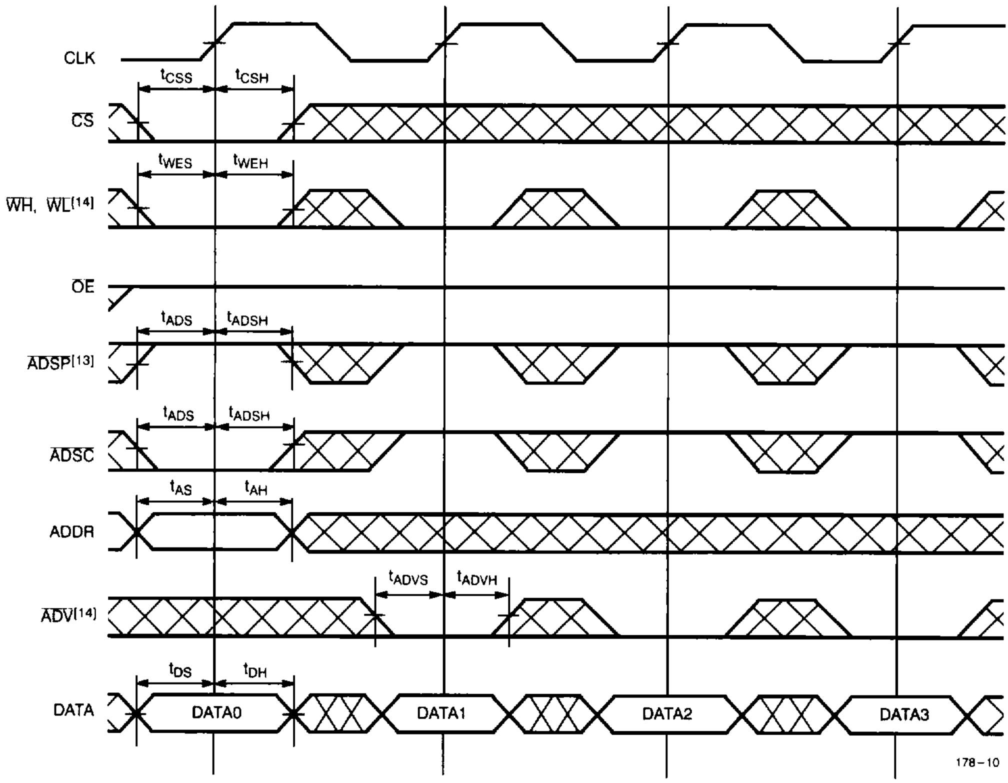
Write Burst Timing: Write Initiated by $\overline{ADSC}$



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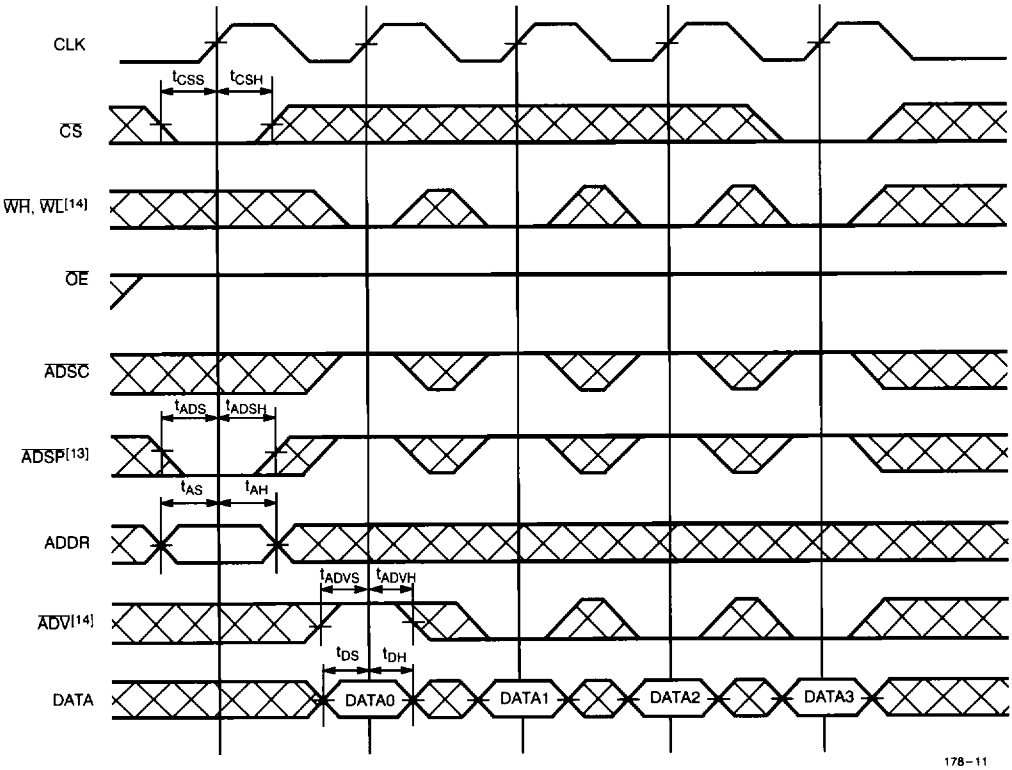
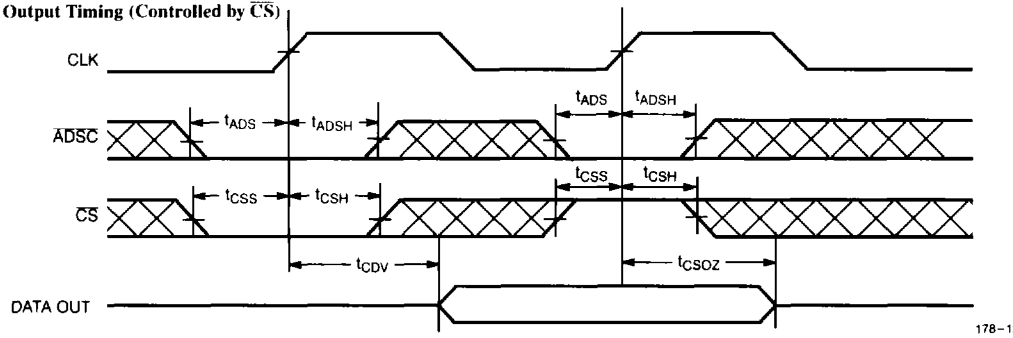
Switching Waveforms (continued)

Write Burst Timing: Write Initiated by $\overline{ADSP}$

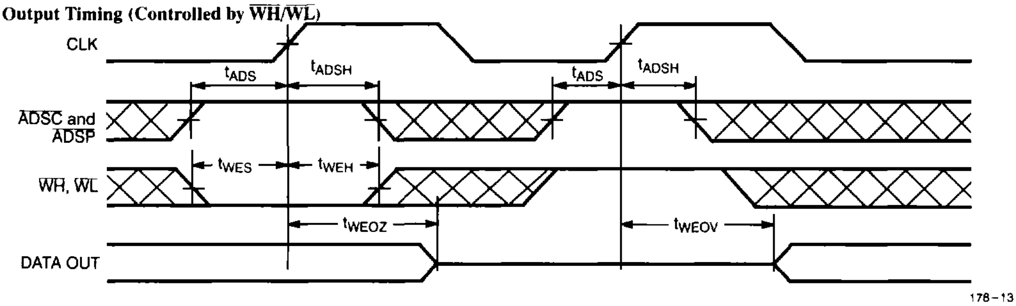


Switching Waveforms (continued)

Output Timing (Controlled by $\overline{CS}$)



Output Timing (Controlled by $\overline{WH}$/$\overline{WL}$)



Truth Table

Input						Address	Operation
$\overline{CS}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WH}$ or $\overline{WL}$	CLK		
H	L	H	H	H	L→H	Same address as previous cycle	$\overline{ADSP}$ ignored, read cycle
H	L	H	L	H	L→H	Incremented burst address	$\overline{ADSP}$ ignored, read cycle in burst sequence
H	L	H	H	L	L→H	Same address as previous cycle	$\overline{ADSP}$ ignored, write cycle
H	L	H	L	L	L→H	Incremented burst address	$\overline{ADSP}$ ignored, write cycle in burst sequence
H	X	L	X	X	L→H	N/A	Chip deselected
L	L	X	X	X	L→H	External	Read cycle, begin burst
L	H	L	X	H	L→H	External	Read cycle, begin burst
L	H	L	X	L	L→H	External	Write cycle, begin burst
X	H	H	L	L	L→H	Incremented burst address	Write cycle, in burst sequence
X	H	H	L	H	L→H	Incremented burst address	Read cycle, in burst sequence
X	H	H	H	L	L→H	Same address as previous cycle	Write cycle
X	H	H	H	H	L→H	Same address as previous cycle	Read cycle

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
8	CY7C178-8JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C178-8NC	TBD	52-Lead Plastic Quad Flatpack	
10	CY7C178-10JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C178-10NC	TBD	52-Lead Plastic Quad Flatpack	
12	CY7C178-12JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C178-10NC	TBD	52-Lead Plastic Quad Flatpack	
	CY7C178-12YMB	Y59	52-Pin Ceramic Leaded Chip Carrier	Military

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
8	CY7C179-8JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C179-8NC	TBD	52-Lead Plastic Quad Flatpack	
10	CY7C179-10JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C179-10NC	TBD	52-Lead Plastic Quad Flatpack	
12	CY7C179-12JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C179-12NC	TBD	52-Lead Plastic Quad Flatpack	
	CY7C179-12YMB	Y59	52-Pin Ceramic Leaded Chip Carrier	Military

Shaded areas contain advanced information.

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