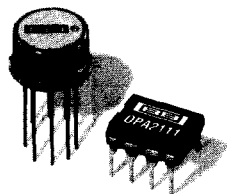


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OPA2111

www.burr-brown.com/databook/OPA2111.html

OPA2111

2

OPERATIONAL AMPLIFIERS

Dual Low Noise Precision *Difet*® OPERATIONAL AMPLIFIER

FEATURES

- **LOW NOISE:** 100% Tested, $8\text{nV}/\sqrt{\text{Hz}}$ max at 10kHz
- **LOW BIAS CURRENT:** 4pA max
- **LOW OFFSET:** 500 μV max
- **LOW DRIFT:** 2.8 $\mu\text{V}/^\circ\text{C}$
- **HIGH OPEN-LOOP GAIN:** 114dB min
- **HIGH COMMON-MODE REJECTION:** 96dB min

APPLICATIONS

- **PRECISION INSTRUMENTATION**
- **DATA ACQUISITION**
- **TEST EQUIPMENT**
- **PROFESSIONAL AUDIO EQUIPMENT**
- **MEDICAL EQUIPMENT**
- **DETECTOR ARRAYS**

DESCRIPTION

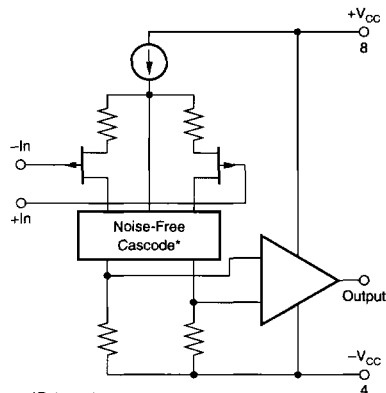
The OPA2111 is a high precision monolithic dielectrically isolated FET (*Difet*) operational amplifier. Outstanding performance characteristics allow its use in the most critical instrumentation applications.

Noise, bias current, voltage offset, drift, open-loop gain, common-mode rejection, and power supply rejection are superior to BIFET® amplifiers.

Very low bias current is obtained by dielectric isolation with on-chip guarding.

Laser trimming of thin-film resistors gives very low offset and drift. Extremely low noise is achieved with patented circuit design techniques. A cascode design allows high precision input specifications and reduced susceptibility to flicker noise.

Standard dual op amp pin configuration allows upgrading of existing designs to higher performance levels.



*Patented

OPA2111 Simplified Circuit
(Each Amplifier)

BIFET® National Semiconductor Corp., *Difet*® Burr-Brown Corp.

International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111
Internet: <http://www.burr-brown.com/> • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132



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SPECIFICATIONS

ELECTRICAL

At $V_{CC} = \pm 15VDC$ and $T_A = +25^\circ C$, unless otherwise noted

PARAMETER	CONDITION	OPA2111AM			OPA2111BM			OPA2111SM			OPA2111KM, KP			UNITS	
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
INPUT NOISE Voltage, $f_o = 10Hz$ $f_o = 100Hz$ $f_o = 1kHz$ $f_o = 10kHz$ $f_B = 10Hz$ to $10kHz$ $f_B = 0.1Hz$ to $10Hz$ Current, $f_B = 0.1Hz$ to $10Hz$ $f_o = 0.1Hz$ to $20kHz$	100% Tested		40	80		30	60		40	80		40		nV/\sqrt{Hz}	
	100% Tested		15	40		11	30		15	40		15		nV/\sqrt{Hz}	
	100% Tested		8	15		7	12		8	15		8		nV/\sqrt{Hz}	
	(1)		6	8		6	8		6	8		6		nV/\sqrt{Hz}	
	(1)		0.7	1.2		0.6	1		0.7	1.2		0.7		μV_{rms}	
	(1)		1.6	3.3		1.2	2.5		1.6	3.3		1.6		μV_{p-p}	
(1)		15	24		12	19		15	24		15		fA_{p-p}		
(1)		0.8	1.3		0.6	1		0.8	1		0.8		fA/\sqrt{Hz}		
OFFSET VOLTAGE (2) Input Offset Voltage Average Drift Match Supply Rejection Channel Separation	$V_{CM} = 0VDC$ $T_A = T_{MIN}$ to T_{MAX}		± 0.1	± 0.75		± 0.05	± 0.5		± 0.1	± 0.75		± 0.3	± 2	mV	
			± 2	± 6		± 0.5	± 2.8		± 2	± 6		± 8	± 15	$\mu V/^\circ C$	
			± 1			± 0.5			± 2			± 2		$\mu V/^\circ C$	
		90	110		96	110		90	110		86	110		dB	
	100Hz, $R_L = 2k\Omega$		± 3	± 31		± 3	± 16		± 3	± 31		± 3	± 50	$\mu V/V$	
			136			136			136			136		dB	
BIAS CURRENT (2) Input Bias Current Match	$V_{CM} = 0VDC$		± 2	± 8		± 1.2	± 4		± 2	± 8		± 3	± 15	pA	
			± 1			± 0.5			± 1			± 2		pA	
OFFSET CURRENT (2) Input Offset Current	$V_{CM} = 0VDC$		± 1.2	± 6		± 0.6	± 3		± 1.2	± 6		± 3	± 12	pA	
IMPEDANCE Differential Common-Mode			$10^{13} \parallel 1$			$10^{13} \parallel 1$			$10^{13} \parallel 1$			$10^{13} \parallel 1$		Ω \parallel pF	
			$10^{14} \parallel 3$			$10^{14} \parallel 3$			$10^{14} \parallel 3$			$10^{14} \parallel 3$		Ω \parallel pF	
VOLTAGE RANGE Common-Mode Input Range Common-Mode Rejection	$V_{IN} = \pm 10VDC$	± 10	± 11		± 10	± 11		± 10	± 11		± 10	± 11		V	
		90	110		96	110		90	110		82	110		dB	
OPEN-LOOP GAIN, DC Open-Loop Voltage Gain Match	$R_L \geq 2k\Omega$	110	125		114	125		110	125		106	125		dB	
				3			2			3			3	dB	
FREQUENCY RESPONSE Unity Gain, Small Signal Full Power Response Slew Rate Settling Time, 0.1% 0.01% Overload Recovery, 50% Overdrive(3)	20Vp-p, $R_L = 2k\Omega$ $V_O = \pm 10V$, $R_L = 2k\Omega$ Gain = -1, $R_L = 2k\Omega$ 10V Step		2			2			2			2		MHz	
		16	32		16	32		16	32			32		kHz	
		1	2		1	2		1	2			2		V/ μs	
			6			6			6			6		μs	
	Gain = -1		10			10			10			10		μs	
RATED OUTPUT Voltage Output Current Output Output Resistance Load Capacitance Stability Short Circuit Current	$R_L = 2k\Omega$ $V_O = \pm 10VDC$ DC, Open-Loop Gain = +1	± 10	± 11		± 10	± 11		± 10	± 11		± 10	± 11		V	
		± 5	± 10		± 5	± 10		± 5	± 10		± 5	± 10		mA	
			100			100			100			100		Ω	
			1000			1000			1000			1000		pF	
		10	40		10	40		10	40		10	40		mA	
POWER SUPPLY Rated Voltage Voltage Range, Derated Performance Current, Quiescent	$I_O = 0mADC$		± 15			± 15			± 15			± 15		VDC	
		± 5		± 18	± 5		± 18	± 5		± 18	± 5		± 18	VDC	
			5	7		5	7		5	7		5	9	mA	
TEMPERATURE RANGE Specification Operating "M" Package "P" Package Storage "M" Package "P" Package θ Junction-Ambient	Ambient Temp.	-25		+85	-25		+85	-55		+125	0		+70	$^\circ C$	
		-55		+125	-55		+125	-55		+125	-55		+125	$^\circ C$	
												-40		+85	$^\circ C$
		-65		+150	-65		+150	-65		+150	-65		+150	$^\circ C$	
												-40		+85	$^\circ C$
		200			200			200			200(4)		$^\circ C/W$		

NOTES: (1) Sample tested—this parameter is guaranteed. (2) Offset voltage, offset current, and bias current are measured with the units fully warmed up. (3) Overload recovery is defined as the time required for the output to return from saturation to linear operation following the removal of a 50% input overdrive. (4) Typical $\theta_{JA} = 150^\circ C/W$ for plastic DIP.



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ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

At $V_{CC} = \pm 15\text{VDC}$ and $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.

PARAMETER	CONDITION	OPA2111AM			OPA2111BM			OPA2111SM			OPA2111KM, KP			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TEMPERATURE RANGE Specification Range	Ambient Temp.	-25		+85	-25		+85	-55		+125	0		+70	°C
INPUT OFFSET VOLTAGE ⁽¹⁾ Input Offset Voltage Average Drift Match Supply Rejection	$V_{CM} = 0\text{VDC}$		±0.22 ±2 1 86	±1.2 ±6 ±50		±0.08 ±0.5 0.5 90	±0.75 ±2.8 ±10		±0.3 ±2 2 86	±1.5 ±6 ±50		±0.9 ±8 2 82	±5 ±15 ±80	mV μV/°C dB μV/V
BIAS CURRENT ⁽¹⁾ Input Bias Current Match	$V_{CM} = 0\text{VDC}$		±125 60	±1nA		±75 30	±500		±2nA 1nA	±16.3nA		±125 ±500	pA pA	
OFFSET CURRENT ⁽¹⁾ Input Offset Current	$V_{CM} = 0\text{VDC}$		±75	±750		±38	±375		±1.3nA	±12nA		±75	±375	pA
VOLTAGE RANGE Common-Mode Input Range Common-Mode Rejection	$V_{IN} = \pm 10\text{VDC}$	±10 86	±11 100		±10 90	±11 100		±10 86	±11 100		±10 80	±11 100		V dB
OPEN-LOOP GAIN, DC Open-Loop Voltage Gain Match	$R_L \geq 2\text{k}\Omega$	106 86	120 5		110 90	120 3		106 86	120 5		100 80	120 5		dB dB
RATED OUTPUT Voltage Output Current Output Short Circuit Current	$R_L = 2\text{k}\Omega$ $V_O = \pm 10\text{VDC}$ $V_O = 0\text{VDC}$	±10.5 ±5 10	±11 ±10 40		±10.5 ±5 10	±11 ±10 40		±10.5 ±5 10	±11 ±10 40		±10.5 ±5 10	±11 ±10 40		V mA mA
POWER SUPPLY Current, Quiescent	$I_O = 0\text{mADC}$		5	8		5	8		5	8		5	10	mA

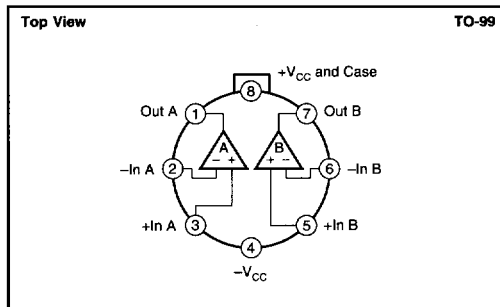
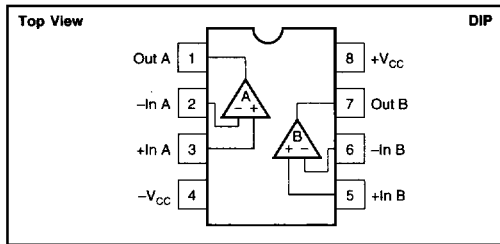
NOTES: (1) Offset voltage, offset current, and bias current are measured with the units fully warmed up.

OPA2111
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OPERATIONAL AMPLIFIERS

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CONNECTION DIAGRAMS



ABSOLUTE MAXIMUM RATINGS

Supply	±18VDC
Internal Power Dissipation ($T_J \leq +175^\circ\text{C}$)	500mW
Differential Input Voltage	Total V_{CC}
Input Voltage Range	$\pm V_{CC}$
Storage Temperature Range: "M" Package	-65°C to +150°C
"P" Package	-40°C to +85°C
Operating Temperature Range: "M" Package	-55°C to +125°C
"P" Package	-40°C to +85°C
Lead Temperature (soldering, 10s)	+300°C
Output Short Circuit to Ground (+25°C)	Continuous
Junction Temperature	+175°C

ORDERING INFORMATION

PRODUCT	PACKAGE	TEMPERATURE RANGE	OFFSET VOLTAGE, max (mV)
OPA2111AM	TO-99	-25°C to +85°C	±0.75
OPA2111BM	TO-99	-25°C to +85°C	±0.5
OPA2111KM	TO-99	0°C to +70°C	±2
OPA2111SM	TO-99	-55°C to +125°C	±0.75
OPA2111KP	8-Pin Plastic DIP	0°C to +70°C	±2

PACKAGE INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER ⁽¹⁾
OPA2111AM	TO-99	001
OPA2111BM	TO-99	001
OPA2111KM	TO-99	001
OPA2111SM	TO-99	001
OPA2111KP	8-Pin Plastic DIP	006

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

