

## Low-Noise Phase-Locked Loop Clock Driver with 9 Clock Outputs

### Features

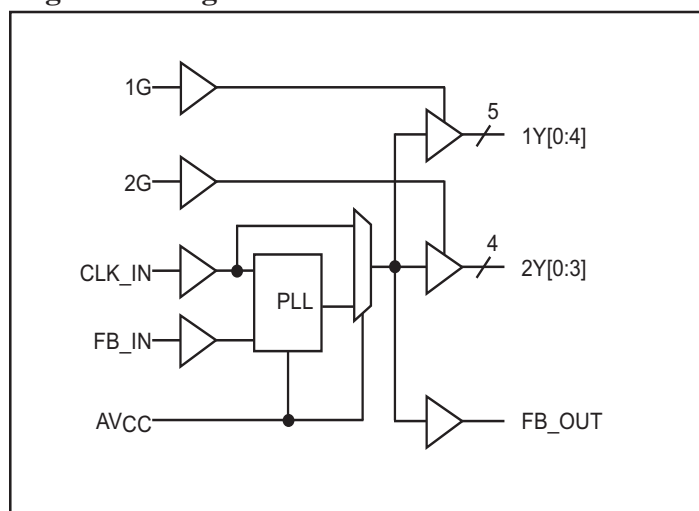
- Operating Frequency up to 150 MHz
- Low-Noise Phase-Locked Loop Clock Distribution to meet 133 MHz Registered DIMM Synchronous DRAM module specifications for server/workstation/PC applications
- Allows Clock Input to have Spread Spectrum modulation for EMI reduction
- Zero input-to-output delay: Distribute One Clock Input to one bank of five and one bank of four outputs, with separate output enables
- Low jitter: cycle-to-cycle jitter  $\pm 75$ ps max.
- 30-ohm on-chip series damping resistor at clock output drivers for low noise and EMI reduction
- Operates at 3.3V V<sub>CC</sub>
- Package (Pb-free and Green available):  
- 24-pin TSSOP (L)

### Description

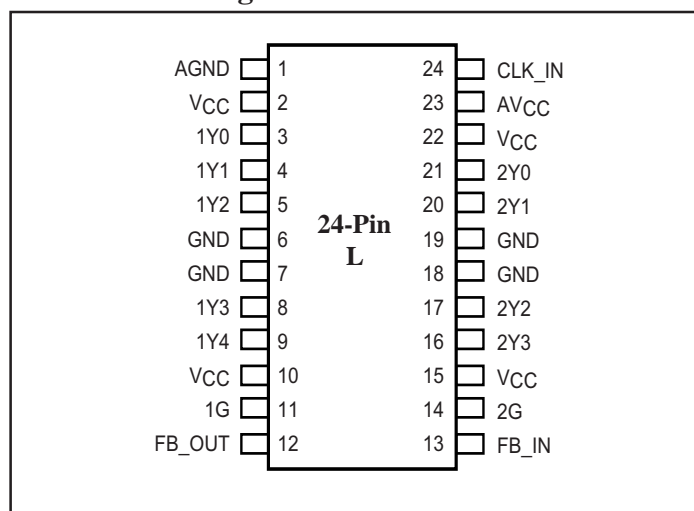
The PI6C2509-133 is a “quiet,” low-skew, low-jitter, phase-locked loop (PLL) clock driver, distributing low-noise clock signals for SDRAM and server applications. By connecting the feedback FB\_OUT output to the feedback FB\_IN input, the propagation delay from the CLK\_IN input to any clock output will be nearly zero. This zero-delay feature allows the CLK\_IN input clock to be distributed, providing 5 clocks for the first bank, and an additional 4 clocks for the second bank.

This clock driver is designed to meet the PC133 SDRAM Registered DIMM specification. For test purposes, the PLL can be bypassed by strapping AV<sub>CC</sub> to ground.

### Logic Block Diagram



### Product Pin Configuration



**Functional Table**

Input Control	Outputs	
X <sup>(1)</sup> G	X <sup>(1)</sup> Y[0:3]	FB_OUT
L	L	CLK_IN
H	CLK_IN	CLK_IN

**Note:**

1. X is either 1 or 2

**Pin Functions**

Pin Name	Pin No.	Type	Description
CLK_IN	24	I	Clock input. CLK_IN allows spread spectrum.
FB_IN	13	I	Feedback input. FB_IN provides the feedback signal to the internal PLL.
1G	11	I	Output bank enable. When 1G is LOW, outputs 1Y[0:4] are disabled to a logic low state. When 1G is HIGH, all outputs 1Y[0:4] are enabled.
2G	14	I	Output bank enable. When 2G is LOW, outputs 2Y[0:3] are disabled to a logic low state. When 2G is HIGH, all outputs 2Y[0:3] are enabled.
FB_OUT	12	O	Feedback output. FB_OUT is dedicated for external feedback. FB_OUT has an embedded series-damping resistor of the same value as the clock outputs 1Y <sub>x</sub> , 2Y <sub>x</sub> .
1Y[0:4]	3,4,5,8,9	O	Clock outputs. These outputs provide low-skew copies of CLK_IN. Each output has an embedded series-damping resistor.
2Y[3:0]	16,17, 20, 21	O	Clock outputs. These outputs provide low-skew copies of CLK_IN. Each output has an embedded series-damping resistor.
AV <sub>CC</sub>	23	Power	Analog power supply. AV <sub>CC</sub> can be also used to bypass the PLL for test purposes. When AV <sub>CC</sub> is strapped to ground, PLL is bypassed and CLK_IN. is buffered directly to the device outputs.
AGND	1	Ground	Analog ground. AGND provides the ground reference for the analog circuitry.
V <sub>CC</sub>	2,10,15,22	Power	Power supply.
GND	6,7,18,19	Ground	Ground.

**DC Specifications** (Absolute maximum ratings over operating free-air temperature range)

Symbol	Parameter	Min.	Max.	Units
$V_I$	Input voltage range	-0.5	$V_{CC} + 0.5$	V
$V_O$	Output voltage range			
$V_{L\_DC}$	DC input voltage		+5.0	
$I_{O\_DC}$	DC output current		100	mA
Power	Maximum power dissipation at $T_A = 55^\circ\text{C}$ in still air		1.0	W
$T_{STG}$	Storage temperature	-65	150	$^\circ\text{C}$

**Note:**

Stress beyond those listed under “absolute maximum ratings” may cause permanent damage to the device.

Parameter	Test Conditions	$V_{CC}$	Min.	Typ.	Max.	Units
$I_{CC}$	$V_I = V_{CC}$ or GND; $I_O = 0^{(1)}$	3.6V			10	$\mu\text{A}$
$C_I$	$V_I = V_{CC}$ or GND	3.3V		4		pF
$C_O$	$V_O = V_{CC}$ or GND			6		

**Note:**

1. Continuous output current

**Recommended Operating Conditions**

Symbol	Parameter	Min.	Max.	Units
$V_{CC}$	Supply voltage (Commercial)	3.0	3.6	V
	Supply voltage (Industrial)	3.135	3.465	
$V_{IH}$	High level input voltage	2.0		
$V_{IL}$	Low level input voltage		0.8	
$V_I$	Input voltage	0.0	$V_{CC}$	
$T_A$	Operating free-air temperature (Commercial)	0	70	
	Operating free-air temperature (Industrial)	-40	85	

**Electrical Characteristics** (Over recommended operating free-air temperature range)

**Pull Up/Down Currents:  $V_{CC} = 3.0\text{V}$  ( $V_{CC} = 3.135\text{V}$ )**

Symbol	Parameter	Condition	Min.	Max.	Units
$I_{OH}$	Pull-up current	$V_{OUT} = 2.4\text{V}$		-13.6	mA
	Pull-up current	$V_{OUT} = 2.0\text{V}$		-22	
$I_{OL}$	Pull-down current	$V_{OUT} = 0.8\text{V}$	19		
	Pull-down current	$V_{OUT} = 0.55\text{V}$	13		

### AC Specifications

(Timing requirements over recommended ranges of supply voltage and operating free-air temperature.)

Symbol	Parameter	Min.	Max.	Units
F <sub>CLK</sub>	Input clock frequency (Commercial)	25	150	MHz
	Input clock frequency (Industrial)	25	125	
	Input clock duty cycle	40	60	%
	Stabilization time after power up		1	ms

### Switching Characteristics

(Over recommended ranges of supply voltage and commercial temperature, V<sub>CC</sub>=3.3V ±0.3V, T<sub>A</sub>=0~70°C, C<sub>L</sub>=15pF)

Parameter	Test Conditions	Min.	Typ.	Max.	Units
t <sub>pe</sub> , Phase error	CLK_IN to FB_IN, f = 133 MHz	-150		150	ps
t <sub>j</sub> , Jitter (cycle-to-cycle)	f = 133 MHz	-75		75	
t <sub>sk</sub> , Output skew	Yn or FB_OUT to Yn or FB_OUT			150	
t <sub>dc</sub> , Duty cycle	f = 133 MHz, V <sub>CC</sub> /2	45	50	55	%
t <sub>r</sub> , Rise time	V <sub>O</sub> = 0.4V to 2V		1.0		ns
t <sub>f</sub> , Fall time	V <sub>O</sub> = 2V to 0.4V		1.1		

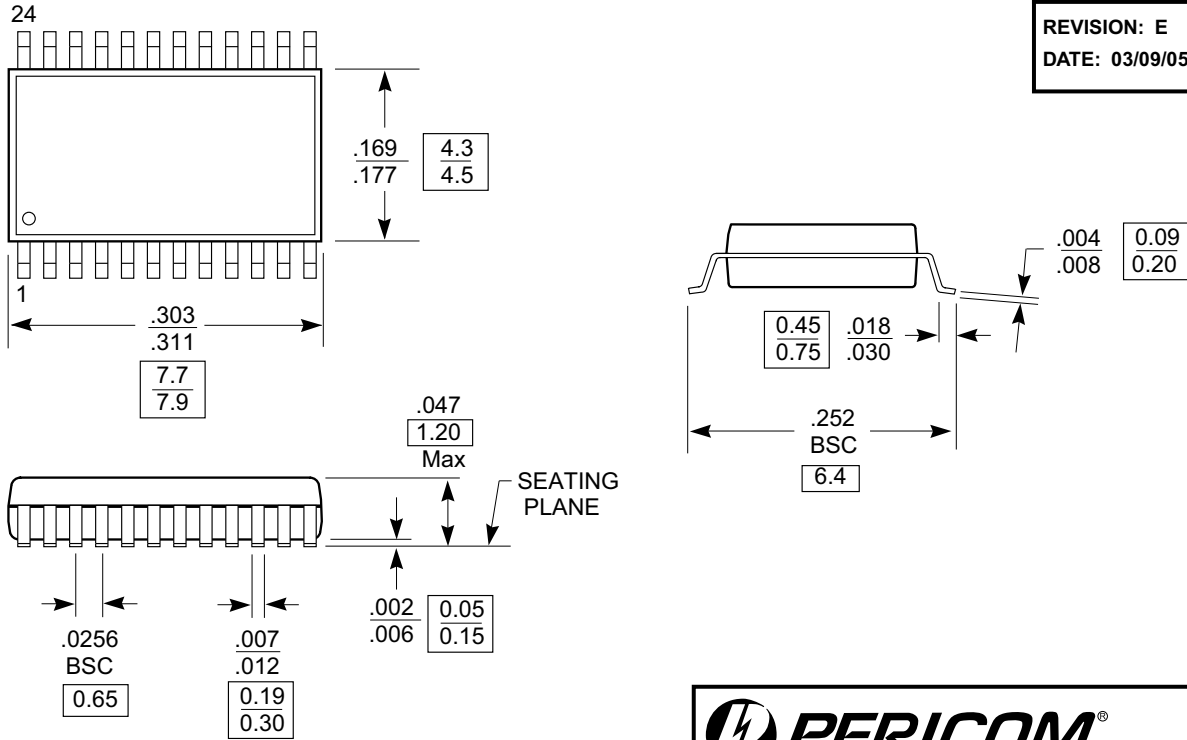

### Switching characteristics

(Over recommended ranges of supply voltage and industrial temperature, V<sub>CC</sub>=3.3V ±0.165V, T<sub>A</sub>=-40~85°C, C<sub>L</sub>=15pF)

Parameter	Test Conditions	Min.	Typ.	Max.	Units
t <sub>pe</sub> , Phase error	CLK_IN to FB_IN, f = 125 MHz	-150		150	ps
t <sub>j</sub> , Jitter (cycle-to-cycle)	f = 125 MHz	-75		75	
t <sub>sk</sub> , Output skew	Yn or FB_OUT to Yn or FB_OUT			150	
t <sub>dc</sub> , Duty cycle	f = 125 MHz, V <sub>CC</sub> /2	45	50	55	%
t <sub>r</sub> , Rise time	V <sub>O</sub> = 0.4V to 2V		1.0		ns
t <sub>f</sub> , Fall time	V <sub>O</sub> = 2V to 0.4V		1.1		

**Note:** These switching parameters are guaranteed, but not production tested.

**Packaging Mechanical: 24-pin Plastic Thin Shrink Small-Outline (L)**

	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="text-align: center;">DOCUMENT CONTROL NO. PD - 1312</td> </tr> <tr> <td style="text-align: center;">REVISION: E DATE: 03/09/05</td> </tr> </table>	DOCUMENT CONTROL NO. PD - 1312	REVISION: E DATE: 03/09/05
DOCUMENT CONTROL NO. PD - 1312			
REVISION: E DATE: 03/09/05			
<p><b>Note:</b></p> <ol style="list-style-type: none"> <li>1. Package Outline Exclusive of Mold Flash and Metal Burr</li> <li>2. Controlling dimensions in millimeters</li> <li>3. Ref: JEDEC MO-153F/AD</li> </ol>	 <p>Pericom Semiconductor Corporation 3545 N. 1st Street, San Jose, CA 95134 1-800-435-2335 • www.pericom.com</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">DESCRIPTION: 24-Pin, 173-Mil Wide, TSSOP</td> </tr> <tr> <td style="padding: 2px;">PACKAGE CODE: L</td> </tr> </table>	DESCRIPTION: 24-Pin, 173-Mil Wide, TSSOP	PACKAGE CODE: L
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**Note:**

• For latest package info, please check: <http://www.pericom.com/products/packaging/mechanicals.php>

**Ordering Information**

Ordering Code	Packaging Code	Package Types
PI6C2509-133LEX	L	Pb-free and Green, 24-pin, 173 mil TSSOP

**Notes:**

- Thermal characteristics can be found on the company web site at [www.pericom.com/packaging/](http://www.pericom.com/packaging/)
- E = Pb-free and Green
- Adding an X suffix = Tape/Reel