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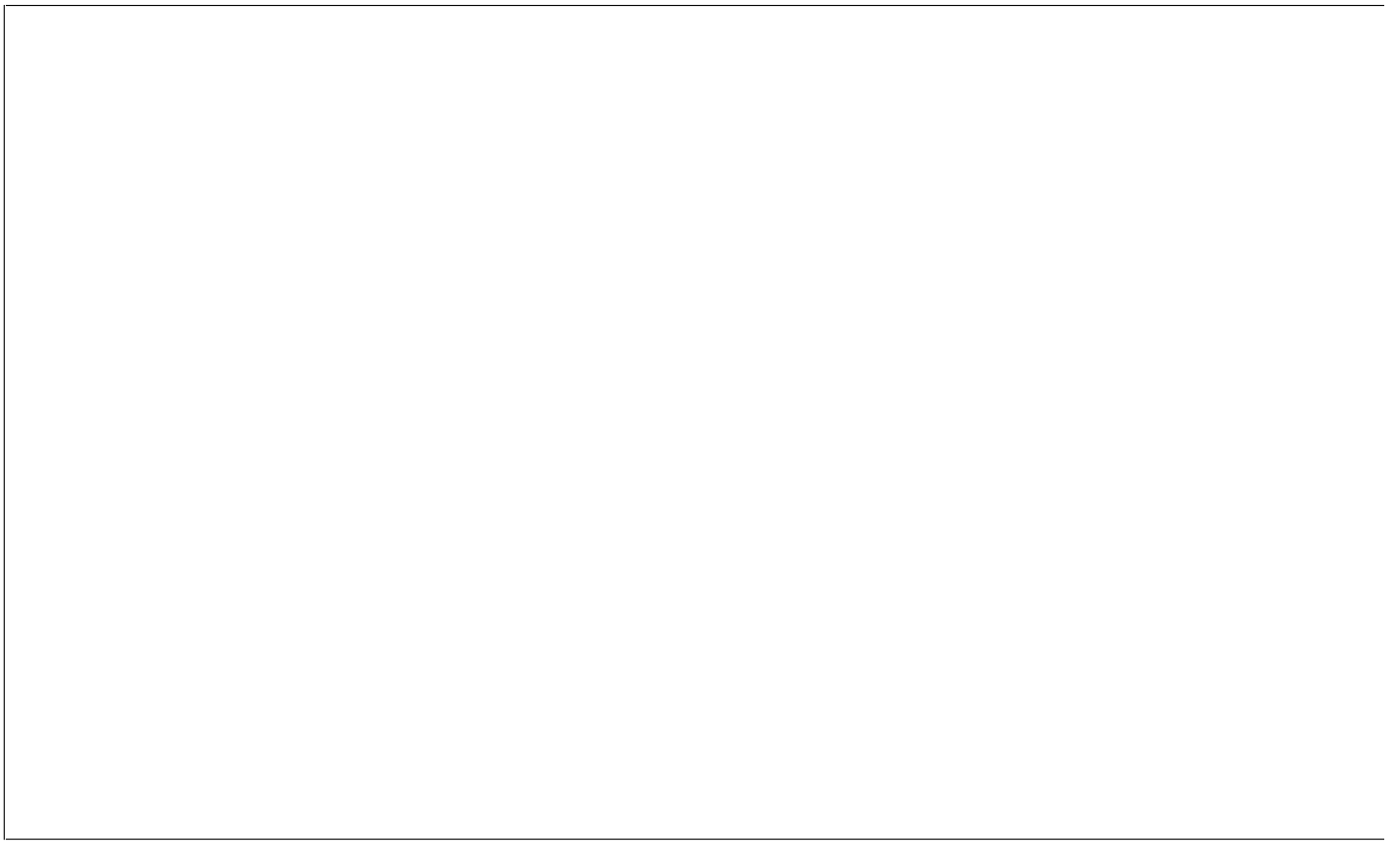

Standard EEPROM ICs

SLx 25C160

16 Kbit (2048 × 8 bit)
Serial CMOS-EEPROM with
Serial Peripheral Interface (SPI) Synchronous Bus

Data Sheet Preliminary 1999-03-15

SLx 25C160 Revision History:		Current Version: Preliminary 1999-03-15
Previous Version:		199-02-02
Page (in previous Version)	Page (in current Version)	Subjects (major changes since last revision)
23	23	Text changed to “The write or erase cycle is finished after 2.5 ms (typical)”
14	14	Figure 7 has changed
19	19	Figure 11 has changed

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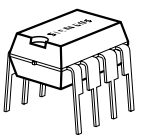
16 Kbit (2048 × 8 bit) Serial CMOS EEPROMs, Serial Peripheral Interface (SPI) Synchronous Bus

SLx 25C160

Preliminary

1 Overview

1.1 Features



P-DIP-8-3

P-DSO-8-2

- **Serial peripheral interface (SPI) compatible, supports SPI Modes 0,0 and 1,1**
- **Page Protection Mode™ for protecting the EEPROM against unintended data changes (SLx 25C160.../P types only)**
- **Low power CMOS**
- **Clock frequency up to 2.1 MHz**
- **V_{CC} = 2.7 to 5.5 V operation**
- **32-byte page mode**
- **Write protect ($\overline{WP}$) pin and write disable instruction for both hardware and software data protection**
- **Block write protection**
  - Protect 1/4, 1/2 or entire array
- **Filtered inputs for noise suppression with Schmitt trigger**
- **High programming flexibility**
  - Internal programming voltage
  - Self timed write cycle including erase (5 ms typical) for up to 32 bytes
  - Byte-write and page-write programming, between 1 and 32 bytes
- **High reliability**
  - Endurance 10^6 cycles[1)]
  - Data retention 40 years[1)]
  - ESD protection > 4000 V on all pins
- **8 pin DIP/DSO packages**
- **Available for extended temperature ranges**
  - Industrial: – 40 °C to + 85 °C
  - Automotive: – 40 °C to + 125 °C
    (– 40 °C to + 150 °C on request)

[1)] Values are temperature dependent, for further information please refer to your Siemens sales office.

Table 1
Ordering Information

Type	Ordering Code	Package	Temperature	Voltage
SLA 25C160-D SLA 25C160-D/P	on request	P-DIP-8-3	– 40 °C … + 85 °C	2.7 V … 5.5 V
SLA 25C160-S SLA 25C160-S/P	on request	P-DSO-8-2	– 40 °C … + 85 °C	2.7 V … 5.5 V
SLE 25C160-D SLE 25C160-D/P	on request	P-DIP-8-3	– 40 °C … + 125 °C	2.7 V … 5.5 V
SLE 25C160-S SLE 25C160-S/P	on request	P-DSO-8-2	– 40 °C … + 125 °C	2.7 V … 5.5 V

Other types are available on request:

- Temperature range (– 40 °C … + 150 °C)
- Packages (TSSOP-8, die, wafer delivery)

1.2 Pin Configuration

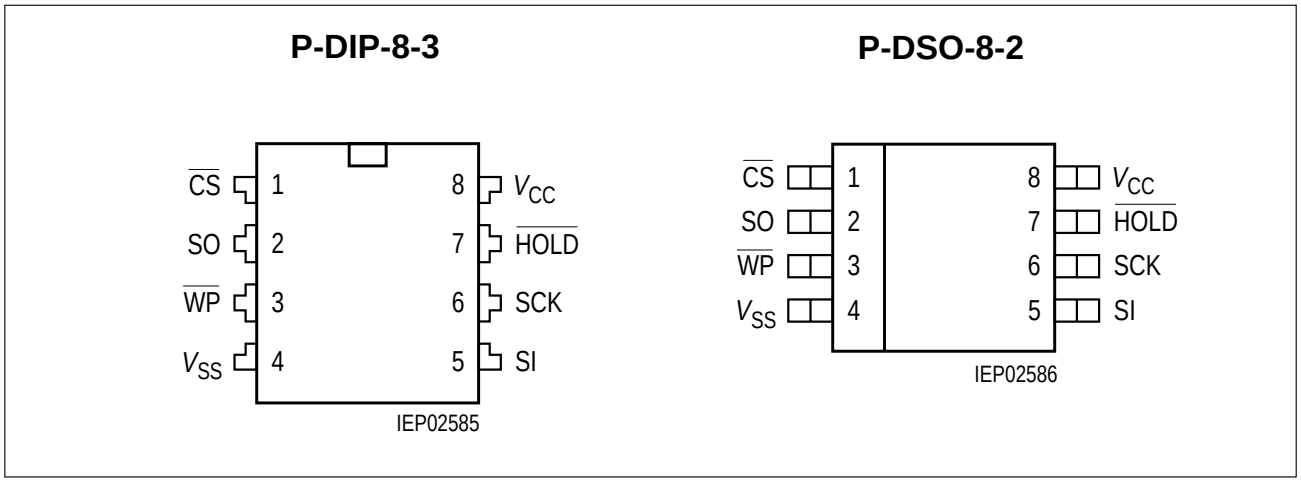


Figure 1
Pin Configuration (top view)

Pin Definitions and Functions.

Table 2

Pin No.	Symbol	Function
1	$\overline{CS}$	Chip select input
2	SO	Serial output
3	$\overline{WP}$	Write protection input
4	V_{SS}	Ground
5	SI	Serial input
6	SCK	Serial clock input
7	$\overline{HOLD}$	Hold input
8	V_{CC}	Supply voltage

Pin Description

Serial Input (SI)

The SI pin is an input and used to clock all instructions, byte addresses and data into the device. Input data is latched on the rising edge of the serial clock.

Serial Output (SO)

The SO pin is an output and used to shift data out of the device. Data is clocked out by the falling edge of the serial clock.

Serial Clock (SCK)

The SCK pin is an input and used to synchronize the communication between the master and the EEPROM.

Chip Select ($\overline{CS}$)

The $\overline{CS}$ pin is an input and used to enable or disable the device. When the $\overline{CS}$ pin is low, the device is enabled. When the $\overline{CS}$ pin is high, the device is disabled and, if no internal programming cycle is in process, forced into the standby mode.

After power up, a high-to-low transition of the $\overline{CS}$ pin is required prior to the start of any operation.

A low-to-high transition of the $\overline{CS}$ pin after a valid write or erase command starts an internal programming cycle. Independent of the $\overline{CS}$ pin an already started programming cycle will be finished and then the device forced into the standby mode. When the device is deselected, SO goes to the high impedance state, allowing multiple parts to share the same SPI bus.

Write Protect ($\overline{WP}$)

The $\overline{WP}$ pin is an input and used to enable or disable write operations to the status register. When the $\overline{WP}$ pin is high, write operations to the status register are allowed. When the $\overline{WP}$ pin is low, all write operations to the status register are disabled, but write operations to the memory are not effected. If the internal programming cycle has already been initiated, a high to low transition of the $\overline{WP}$ pin will have no influence on the programming cycle.

*Note: The function of the $\overline{WP}$ pin can be blocked by setting the WPEN (Write Protect Enable) bit in the status register to "0" (refer to **chapter 4** Status Register). In this case write operations to the status register are possible independent of the status of the $\overline{WP}$ pin.*

When the WPEN bit is "1", it cannot be changed back to "0", as long as the $\overline{WP}$ pin is held low.

HOLD ($\overline{HOLD}$)

The $\overline{Hold}$ pin is an input. When the device is selected with $\overline{CS}$ pin low, the $\overline{Hold}$ pin can be used to pause the serial communication with the master and to continue the communication later without resetting the serial sequence.

To pause the communication the $\overline{Hold}$ pin must be brought low while the SCK pin is low. Inputs to the SI pin will be ignored and the SO pin is in the high impedance state. SCK may still toggle during $\overline{Hold}$. To continue the communication the $\overline{Hold}$ pin must be brought high while the SCK pin is low.

The $\overline{Hold}$ pin must be held high any time this function is not being used.

2 Description

SLx 25C160 is a serial electrically erasable and programmable read only memory (EEPROM), organized as 2048 × 8 bit. The data memory is divided into 64 pages. Up to 32 bytes of a page can be programmed simultaneously.

The device is accessed via a Serial Peripheral Interface (SPI) compatible bus (SPI Modes 0,0 and 1,1). The required bus signals are clock input (SCK) plus separate data in (SI) and data out (SO) lines. Access to the device is controlled through the chip select input ($\overline{CS}$), allowing any number of devices to share the same bus.

For applications with high security requirements against unintended data changes devices with Page Protection Mode™ (SLx 25C160.../P types only, refer to **chapter 7**) are available.

Low voltage design permits operation down to 2.7 V with low active and standby currents. All devices have a minimum endurance of 10^6 erase/write cycles[1)].

The device operates with a maximum clock frequency of 2.1 MHz, a voltage range of V_{CC} = 2.7 … 5.5 V and is available in two temperature ranges for industrial and automotive applications. The device is available in eight-pin DIP and DSO packages; additionally the device may be purchased in die or wafer format.

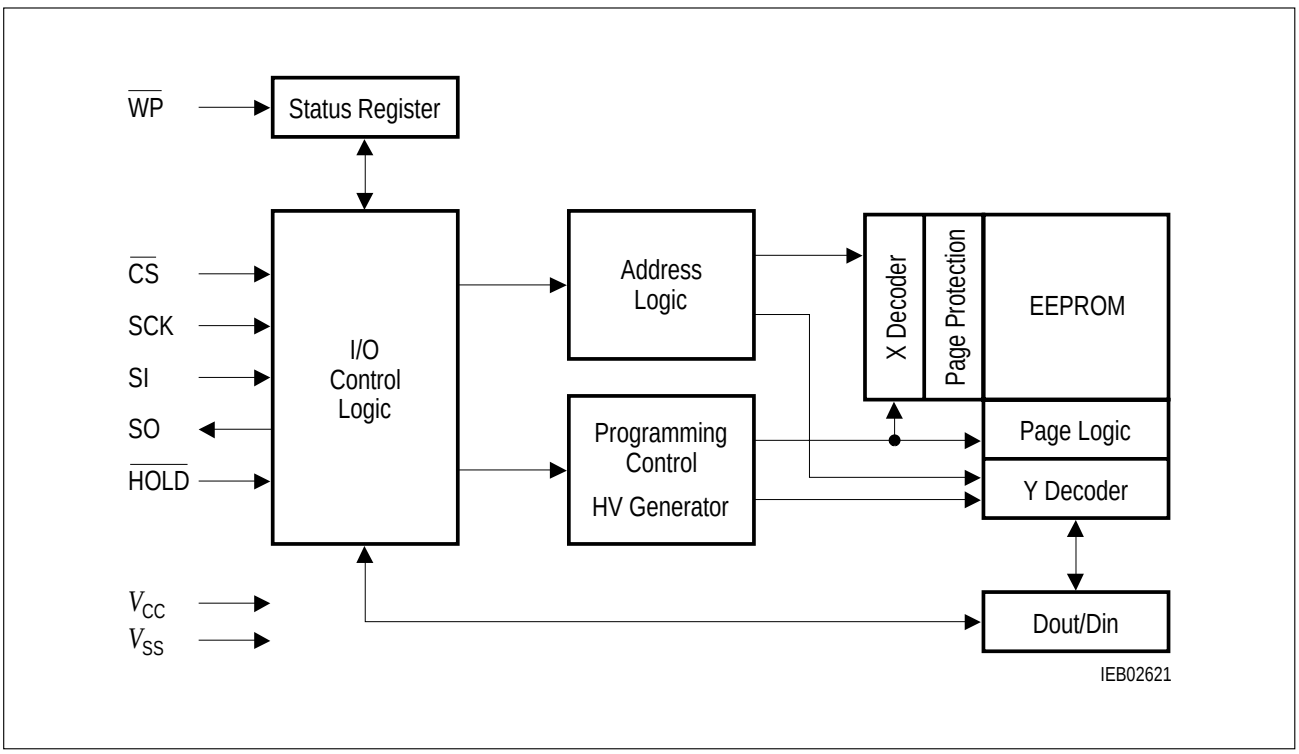


Figure 2
Block Diagram

1) Values are temperature dependent, for further information please refer to your Siemens sales office.

3 SPI Bus Characteristics

Access to the SLx 25C160 device is given via the SPI bus. This bus consists of three wires: SCK for clock, SI for input data from the master to the device and SO for output data from the device to the master. The protocol is master/slave oriented, where the serial EEPROM always takes the role of a slave. The device is selected via the $\overline{CS}$ pin.

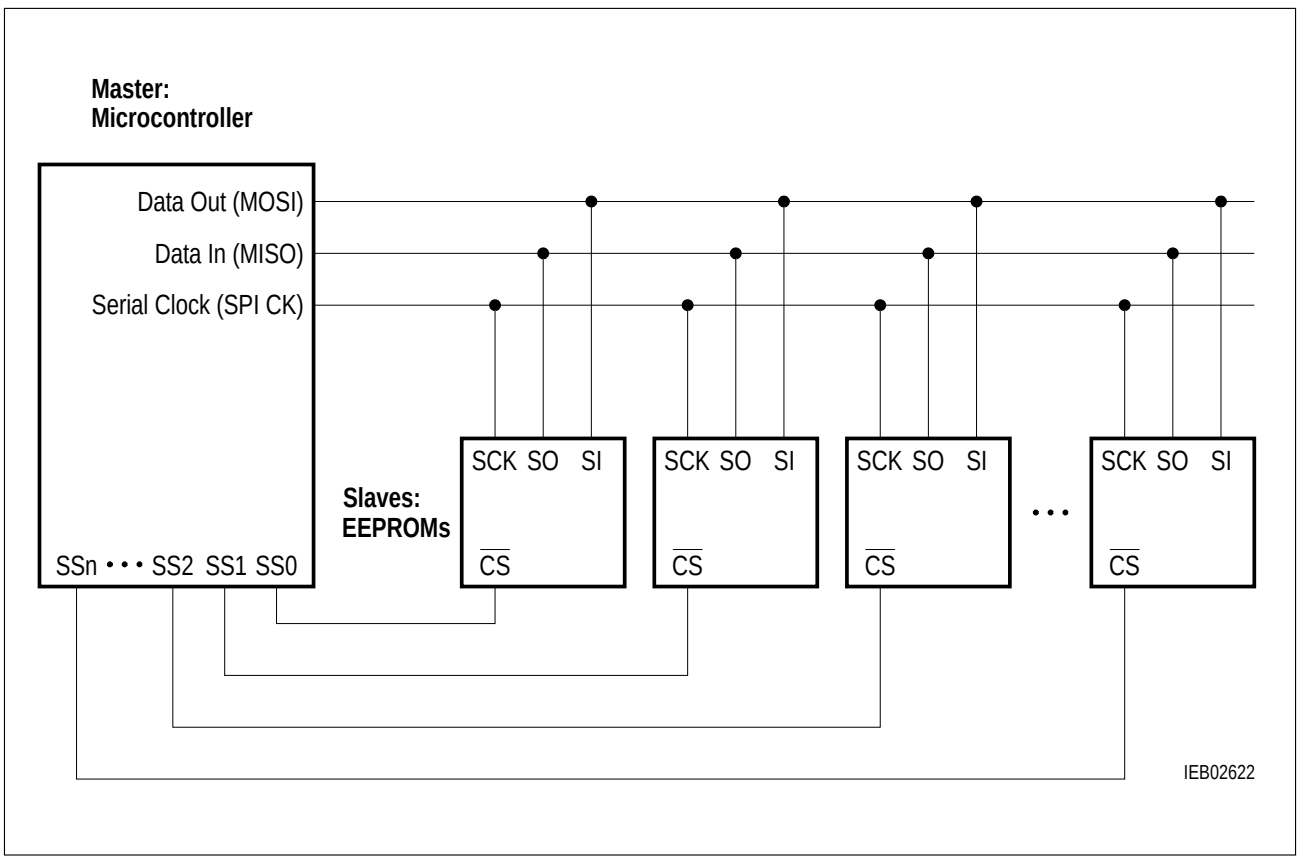


Figure 3
Bus Configuration

Master	Device that initiates the transfer of data and provides the clock for transmit and receive operations. MOSI = Master Output Slave Input MISO = Master Input Slave Output
Slave	Device addressed by the master, capable of receiving and transmitting data.
Transmitter/ Receiver	The SLx 25C160 has separate pins for data transmission (SO) and reception (SI).

SPI Modes 0,0 and 1,1

SPI modes 0,0 and 1,1 means for the slave that the input data is latched on the rising edge of the serial clock and the output data clocked out by the falling edge of the serial clock.

MSB

The Most Significant Bit (MSB) is the first bit transmitted and received.

Invalid instruction

If an invalid instruction is received, the data will be ignored by the device, and the serial output pin (SO) will remain in a high impedance state until the falling edge of $\overline{CS}$ is detected again. This will reinitialize the serial communication.

4 Status Register

SLx 25C160 has a status register indicating the actual status of the device. Read operations are allowed to all bits of the status register via the command byte RDSR (Read Status Register), whereas write operations are only allowed to bit 2-3 (BP0,BP1) and bit 7 (WPEN) via the command byte WRSR (Write Status Register).

Bit 1 (WEL) indicates whether the device is enabled or disabled for write operations. Its status can only be changed via the command bytes WREN (Write Enable, bit 1 = “1”) and WRDI (Write Disable, bit 1 = “0”). All write operations to the status register *and* to the entire memory has to be preceded by the command byte WREN.

The definition of the status register is shown in **table 3**.

Table 3
Definition of the Status Register

Bit	Name	Definition
0	WIP	Write In Process: “0” indicates the device is ready. “1” indicates that a programming cycle is in process (bit 0: read only).
1	WEL	Write Enable Latches: “0” indicates the device is *not* enabled for write operations. “1” indicates the device is enabled for write operations (bit 1: read only).
2	BP0	The Block Protect Bits indicate which blocks are currently write protected (see **table 6**) (bits 2/3: read/write).
3	BP1	
4	x	These bits are not used and always read as “1” (bits 3/4: read only).
5	x	
6	PPA	SLx 25C160... (without Page Protection Mode™): No special function, always read as “1” (bit 6: read only).
		SLx 25C160.../P (with Page Protection Mode™, refer to **chapter 7**): “0” indicates a write or erase operation of the PPM-bits is finished successfully. “1” indicates a write or erase operation of the PPM-bits failed or is still in process. *Note: After power-up PPA is read as “1” (bit 6: read only).*
7	WPEN	Write Protect Enable Bit: “0” blocks the function of the $\overline{WP}$ pin. Independent of the $\overline{WP}$ pin the user can write to the status register. “1” enables the function of the $\overline{WP}$ pin (refer to **chapter 1** Pin Description) (bit 7: read/write).

Note: Bit 0-7 are read as “1” during an internal programming cycle.

4.1 Write Enable and Disable Instructions for Status Register and Memory

Table 4
Write Enable and Disable Instructions

Command Byte	Definition								Function
	b7	b6	b5	b4	b3	b2	b1	b0	
WREN	0	0	0	0	0	1	1	0	Set the write enable latch (enable write operations).
WRDI	0	0	0	0	0	1	0	0	Reset the write enable latch (disable write operations).

Write Enable (WREN)

The device will power up in the write disable state when V_{CC} is applied. All programming commands for the status register and for the memory must therefore be preceded by the write enable command byte WREN. This command sets the WEL bit to “1”.

After the $\overline{CS}$ line is pulled low to select the device, the command byte WREN is transmitted via the SI line. After the transmission of the command byte, the $\overline{CS}$ pin has to be driven high.

Note: After a programming command to the status register or to the memory, the device is automatically returned to the write disable state (WEL = “0”).

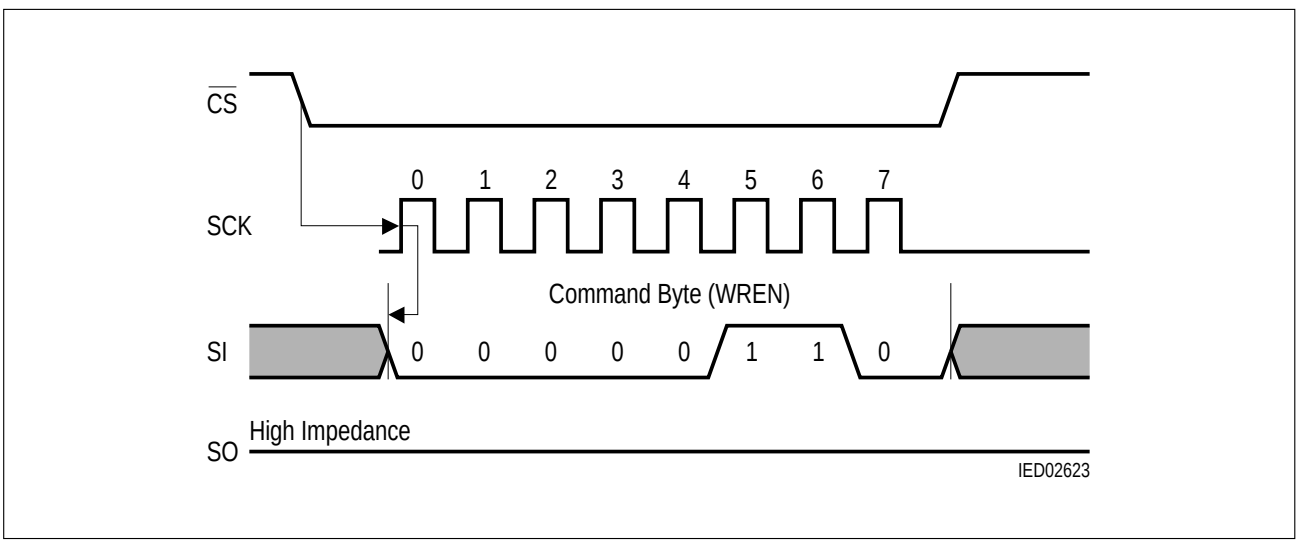


Figure 4
Write Enable (WREN) Sequence

Write Disable (WRDI)

To protect the device against inadvertent writes, the command byte WRDI sets the WEL bit to “0” and therefore all programming modes are disabled.

After the $\overline{CS}$ line is pulled low to select the device, the command byte WRDI is transmitted via the SI line. After the transmission of the command byte the $\overline{CS}$ pin has to be driven high.

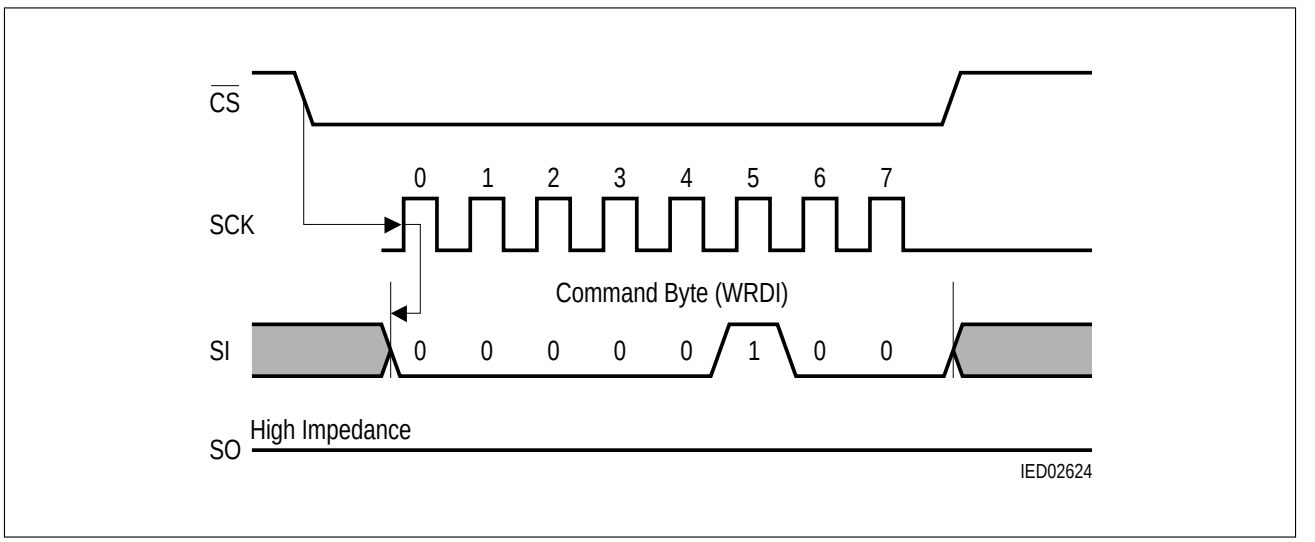


Figure 5
Write Disable (WRDI) Sequence

4.2 Write Operation to the Status Register

Table 5
Write Instruction for the Status Register

Command Byte	Definition								Function
	b7	b6	b5	b4	b3	b2	b1	b0	
WRSR	0	0	0	0	0	0	0	1	Write status register

Write Status Register (WRSR)

The command byte WRSR allows the user to change the status of the BP0, BP1 and WPEN bits in the status register. All other bits in the status register are for read only. In order to start a write operation to the status register, two separate command bytes must be executed. First, the device must be write enabled via the write enable command byte WREN. Then the write status register command byte WRSR can be executed.

Writing to the status register via the SI input requires the following sequence. After the $\overline{CS}$ line is pulled low to select the device, the command byte WRSR is transmitted via

the SI line followed by the status register byte to be programmed (bit 6-4 and 1-0 are don't care bits). Programming will start after the $\overline{CS}$ pin is brought high.

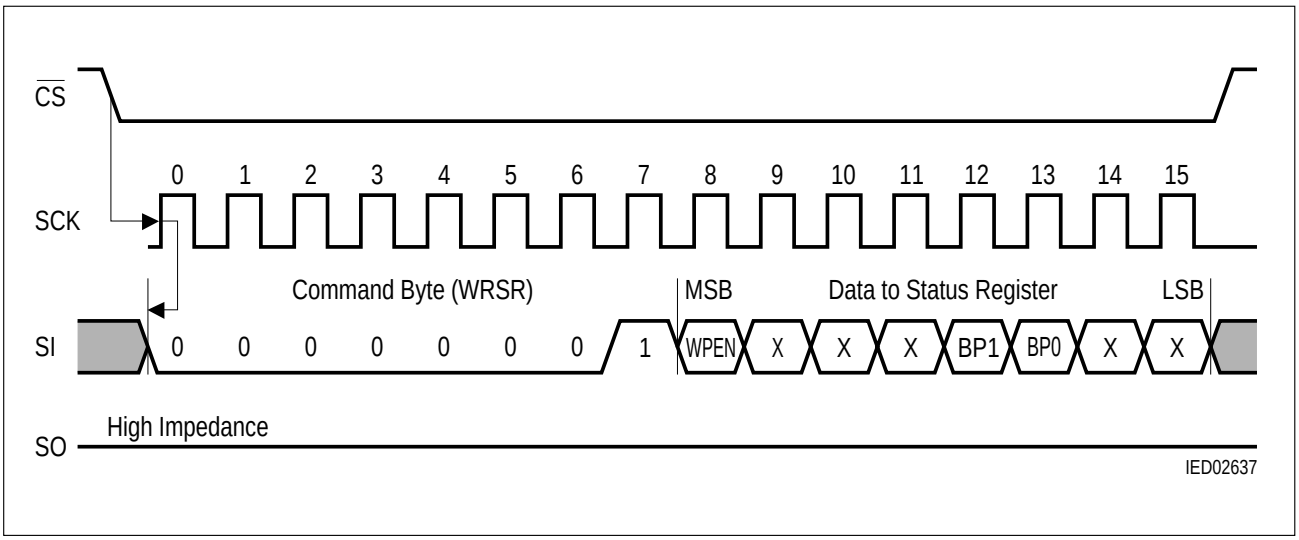


Figure 6
Write to Status Register (WRSR) Sequence

Memory blocks can be protected using BP0 and BP1 according to **table 6**. Data protected in this manner can be read only.

Table 6
Block Write Protection Bits

BP1	BP0	Array Address Protected	Protected Block
0	0	-	0
0	1	$600-$7FF	upper 1/4
1	0	$400-$7FF	upper 1/2
1	1	$000-$7FF	all

The command byte WRSR also allows the user to enable or disable the function of the $\overline{WP}$ pin through the use of the write protect enable bit WPEN. When WPEN is "0" all changes to BP0, BP1 and WPEN are allowed independent of the status of the $\overline{WP}$ pin. WPEN = "1" enables the function of the $\overline{WP}$ pin (refer to **chapter 1** Pin Description).

4.3 Read Operation to the Status Register

Table 7
Read Instruction for the Status Register

Command Byte	Definition								Function
	b7	b6	b5	b4	b3	b2	b1	b0	
RDSR	0	0	0	0	0	1	0	1	Read status register

Read Status Register (RDSR)

The command byte RDSR provides read access to the status register. The status register can be read at any time, even during an internal programming cycle.

Reading the status register via the SO output requires the following sequence. After the $\overline{CS}$ line is pulled low to select a device, the RDSR command byte is transmitted via the SI line. The content of the status register is then shifted out onto the SO line. The $\overline{CS}$ pin should be driven high after data come out.

Note: During an internal programming cycle bit 0-7 of the status register are read as "1".

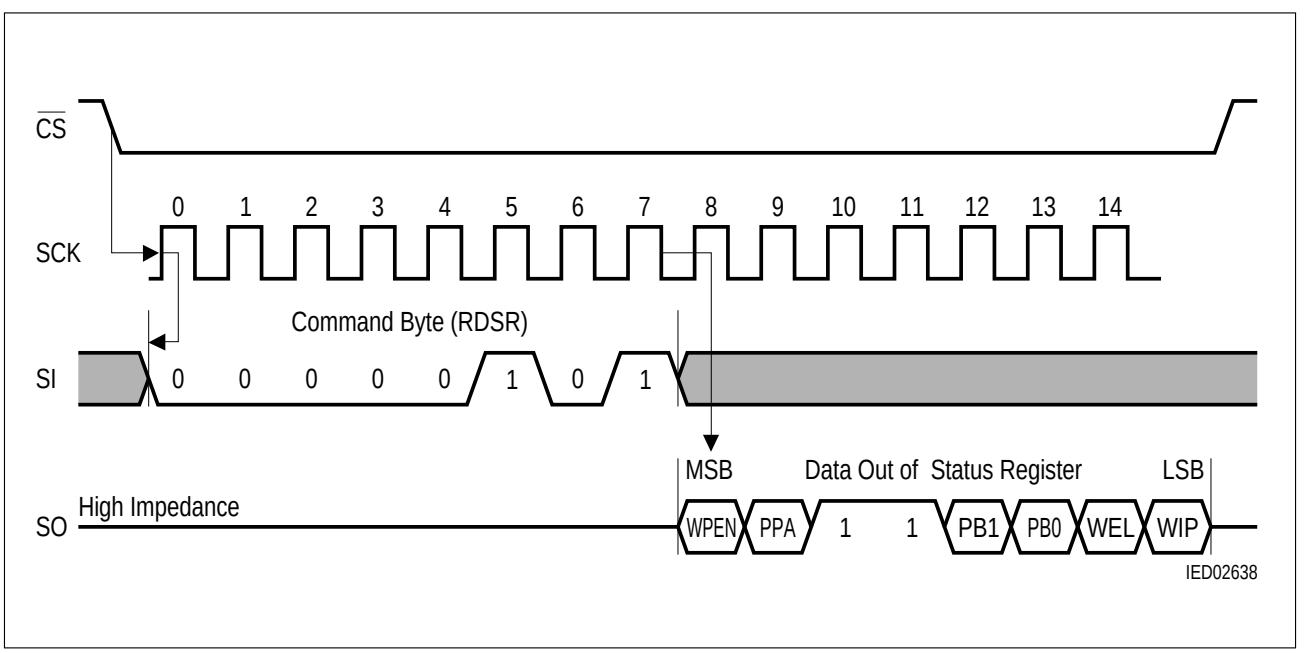


Figure 7
Read from Status Register (RDSR) Sequence

5 Write Operations

In order to start a write operation, two separate operations must be executed. First, the device must be write enabled via the write enable command byte WREN. Then the write operation can be executed. Either one byte (Byte Write) or up to 32 byte (Page Write) can be modified in one programming procedure. During an internal programming cycle, all commands will be ignored except the command byte RDSR (read status register).

*Note: Write operations to the memory can only be executed to blocks that are not write protected by the status register bits BP0 and PB1 and to pages that are not write protected by a Page Protection bit (*SLx 25C160*.../P only, refer to* ***chapter 7****).*

Table 8
Write Instruction

Command Byte	Definition								Function
	b7	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**	
WRITE	0	0	0	0	0	0	1	0	Write data to memory array beginning at selected address.

5.1 Byte Write

A write operation requires the following sequence. After the $\overline{CS}$ line is pulled low to select the device, the command byte WRITE is transmitted via the SI line followed by the byte address (A15-A11 are don't care bits, A10-A0) and the data (D7-D0) to be programmed. Programming will start after the $\overline{CS}$ pin is brought high.

The ready/busy status of the device can be determined by initiating a read to the status register with RDSR. If WIP = "0". the programming cycle is finished. After execution of the command byte WRITE the EEPROM is automatically returned to the write disable state.

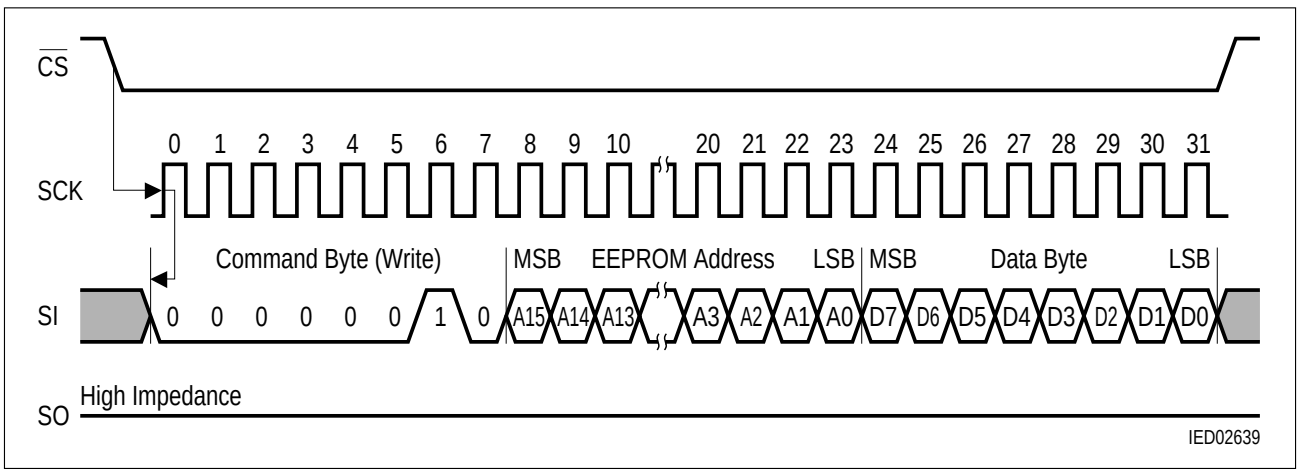


Figure 8
Byte Write Sequence

5.2 Page Write

The page write procedure is the same as the byte write procedure up to the first data byte. In a page write procedure however, the EEPROM address bytes is followed by a sequence of one to a maximum of 32 data bytes with new data to be programmed. If more than 32 bytes of data are transmitted, the address counter will roll over and the previously transmitted data will be overwritten, i.e. only the last 32 transmitted bytes will be programmed. Programming will start after the $\overline{CS}$ pin is brought high.

The ready/busy status of the device can be determined by initiating a read to the status register with RDSR. If WIP = “0”. the programming cycle is finished. After execution of the command byte WRITE the EEPROM is automatically returned to the write disable state.

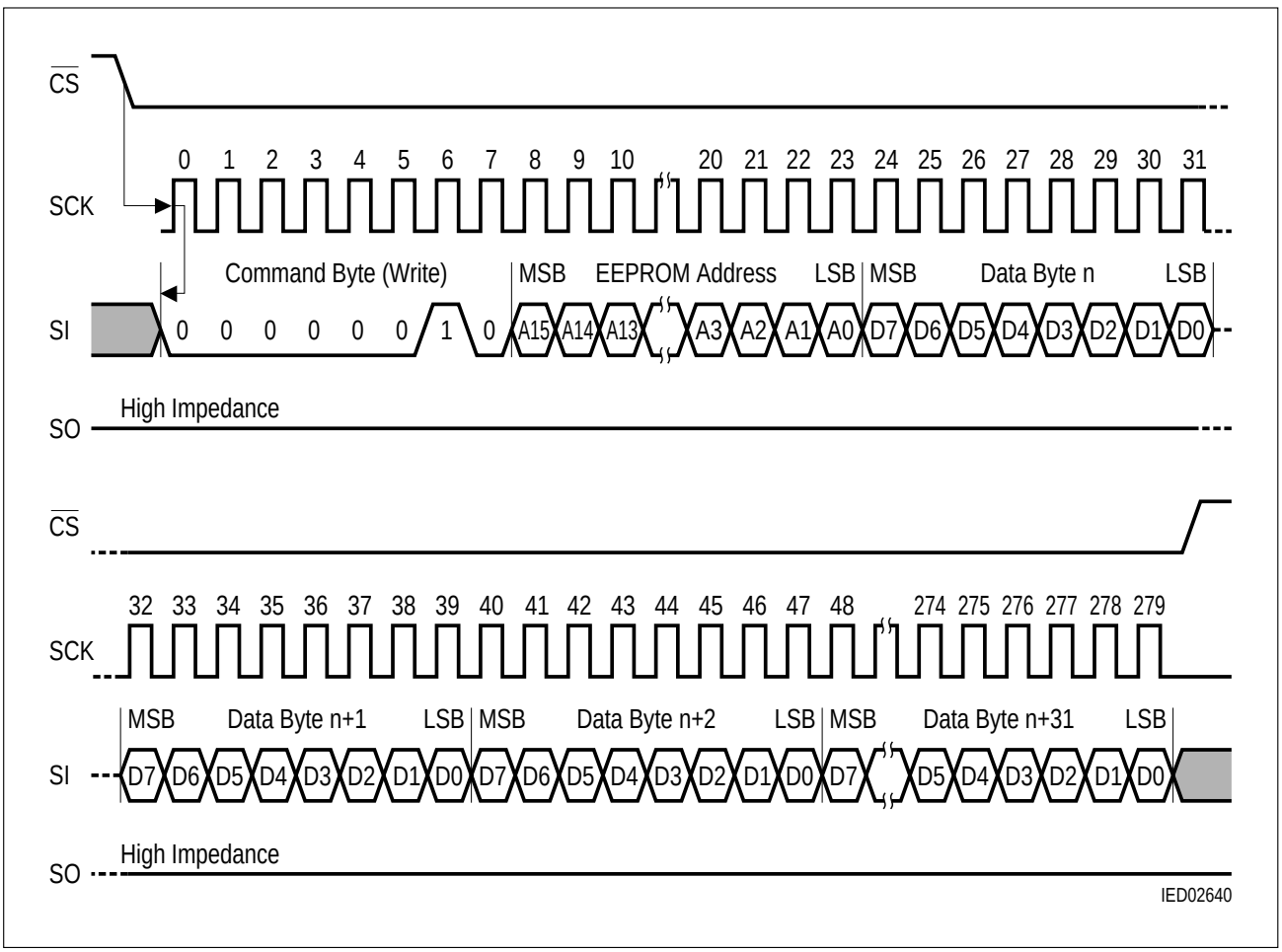


Figure 9
Page Write Sequence

6 Read Operations

Either one byte (Byte Read) or any number of bytes up to the whole memory (Sequential Read) can be read in one sequence.

Table 9
Read Instruction

Command Byte	Definition								Function
	b7	b6	b5	b4	b3	b2	b1	b0	
READ	0	0	0	0	0	0	1	1	Read data from memory array beginning at the selected address.

6.1 Byte Read

Reading the EEPROM via the SO output requires the following sequence. After the $\overline{CS}$ line is pulled low to select the device, the READ command byte is transmitted via the SI line followed by the address to be read (A15-A11 are don't care bits, A10-A0). The data (D7-D0) at the specified address are then shifted out onto the SO line. During this time, any data on the SI line will be ignored. If only one byte is to be read, the $\overline{CS}$ line should be driven high after data come out.

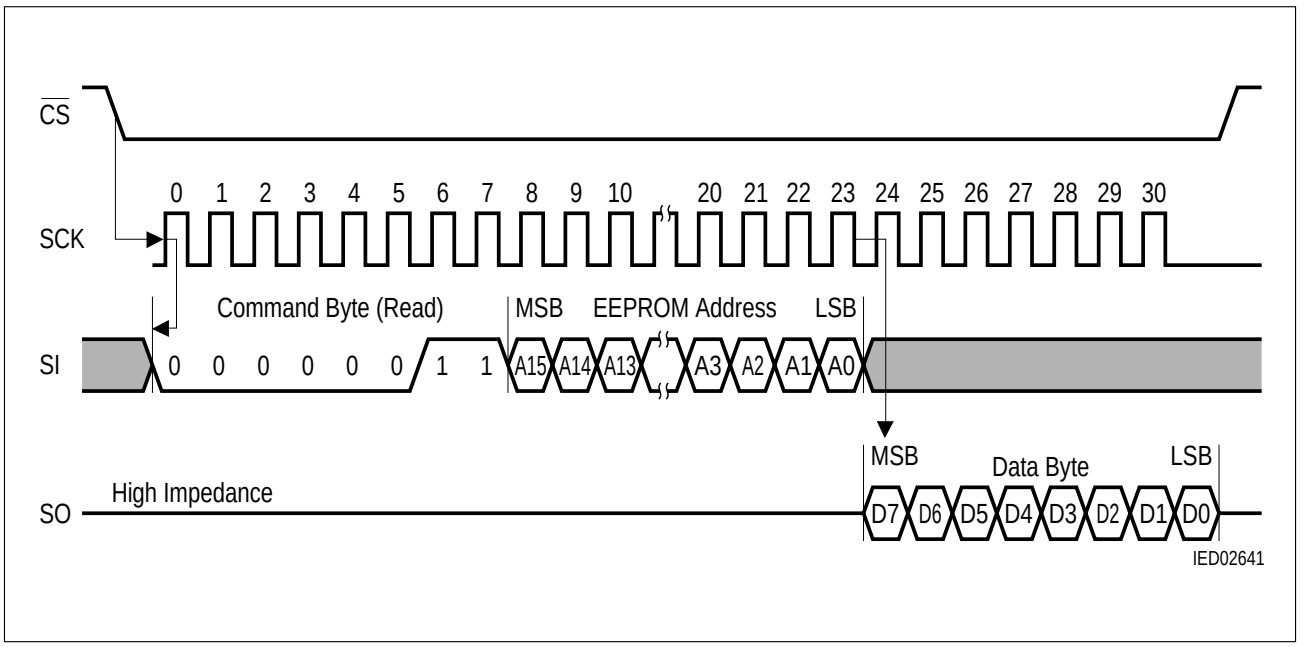


Figure 10
Read Byte Sequence

6.2 Sequential Read

The sequential read procedure is the same as the byte read procedure up to the first data byte is shifted out on the SO line. The read can be continued since the byte address is automatically incremented and data will continue to be shifted out. The read sequence is terminated by pulling up the $\overline{CS}$ line.

Note: When the highest address is reached, the address counter will roll over to the lowest address allowing the entire memory to be read out in one continuous read cycle.

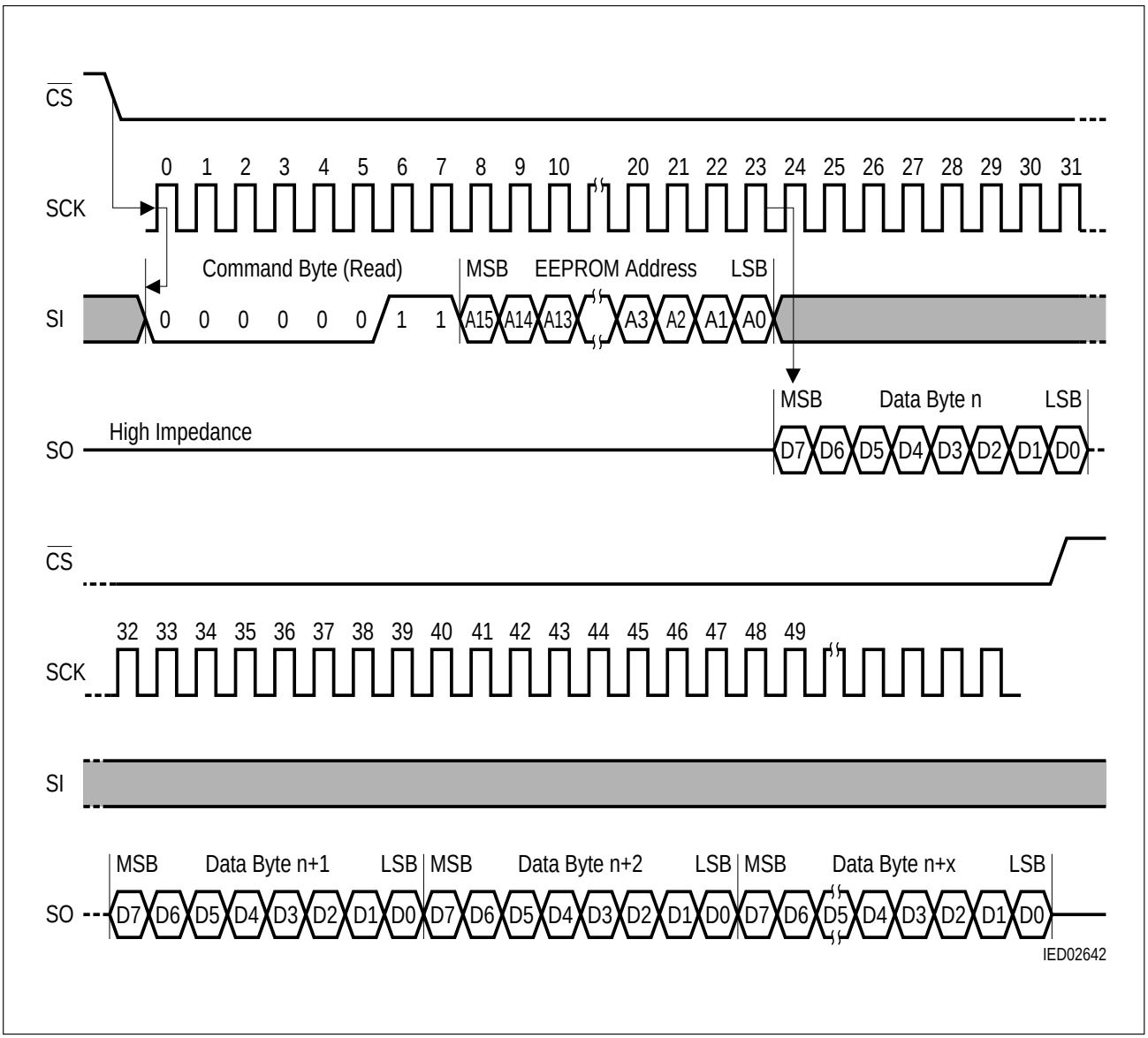


Figure 11
Sequential Read Sequence

7 Page Protection Mode™

The page protection mode is supported by the SLx 25C160.../P types only. For example SLA 25C160-D/P has the same functionality as SLA 25C160-D enhanced by page protection mode.

Each page (32 bytes) in the data memory can be protected against unintended data changes by an associated protection bit. The protection bit memory consists of an additional EEPROM of 64 bit (**figure 12**).

Data in the data memory can be modified only if the assigned protection bit is erased (logical state “1”). After writing the data bytes to a page, the protection is achieved by writing the associated protection bit (logical state “0”). Further changes of data within a protected page is possible only after erasing the protection bit.

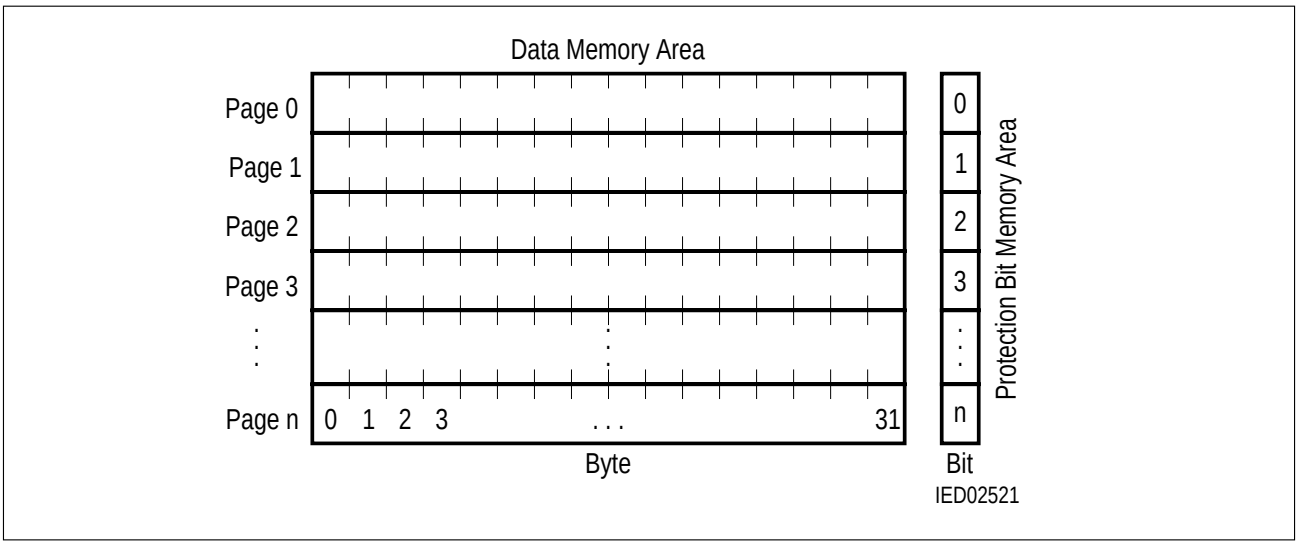


Figure 12
Data Page and Assigned Protection Memory

A special procedure to write or erase a protection bit guarantees proper activation or deactivation of page protection. For protection bit write or erase, all 32 data bytes of the respective page have to be entered for verification. The data then are compared internally with the data to be protected. In case of identity the protection bit is written or erased correspondingly.

7.1 Protection Bit Handling

The bits of the protection memory can be addressed directly for reading or programming. A protection bit address corresponds to the lowest address within the respective page (A15-A11 are don't care bits, A10-A5, A4 to A0 = "0"). The status of each protection bit is sensed internally. A written state ("0") prevents programming in the associated page. If an already protected memory page is accidentally addressed for programming, the programming procedure is suppressed.

For devices with page protection mode, an additional instruction set for addressing and manipulation of protection bits is implemented. For protection bit handling there are three additional command bytes for write, erase and read of a protection bit. These three command bytes are listed below (**table 10**).

Table 10
Instructions for Protection Bit Manipulation

Command Byte	Definition								Function
	b7	b6	b5	b4	b3	b2	b1	b0	
WRPB	0	0	1	0	0	0	1	0	Write page protection bit of selected page.
ERPB	0	0	1	1	0	0	1	0	Erase page protection bit of selected page.
RDPB	0	0	0	1	0	0	1	1	Read page protection bit of selected page.

7.2 Protection Bit Write and Erase

For writing or erasing a protection bit, the data of the respective page have to be known by the master. The master has to present the page data as a reference for comparison by the EEPROM. A successful comparison is necessary in order to change the status of the protection bit.

The data of the page are not effected by the write or erase procedure of the protection bit. The SPI bus protocol is shown in **figure 13** for protection bit write and in **figure 14** for protection bit erase.

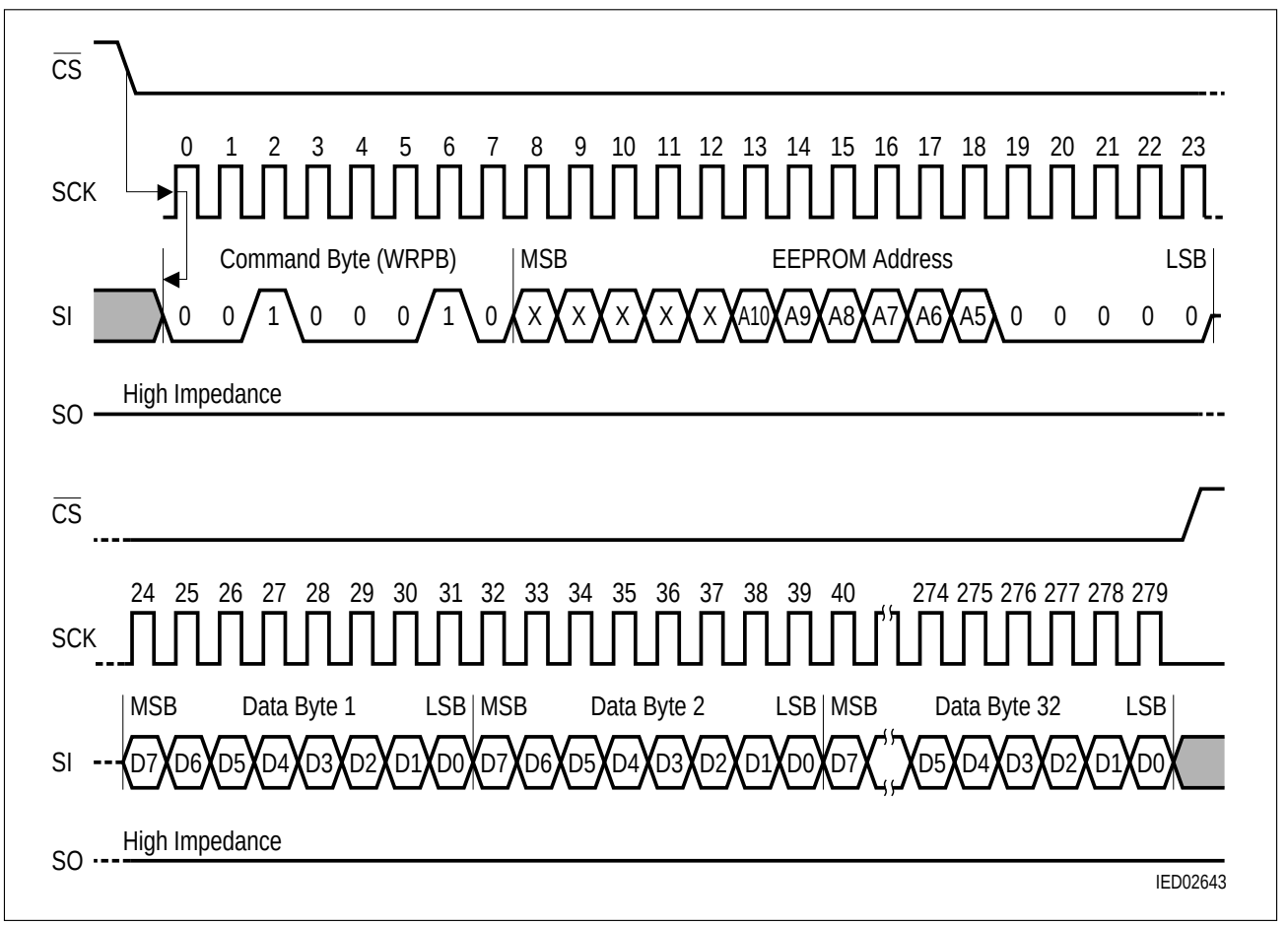


Figure 13
Sequence for Protection Bit Write

A write or erase operation to a page protection bit requires the following sequence. After the $\overline{CS}$ line is pulled low to select the device, the command byte WRPB for protection bit write (or ERPB for protection bit erase) is transmitted via the SI line followed by the address bytes (A15-A11 are don't care bits, A10-A5, A4 to A0 = "0").The address of the protection bit corresponds to the address of the first byte of the page to protect (or unprotect). The address bytes are followed by 32 parameter bytes identical to the 32 data bytes of the page to be protected or unprotected. The data of the first entered byte must be identical to the data byte stored at the lowest address of the current page.

The other 31 bytes have to be identical to the bytes stored in ascending address order within the same page. Programming will start after the $\overline{CS}$ pin is brought high.

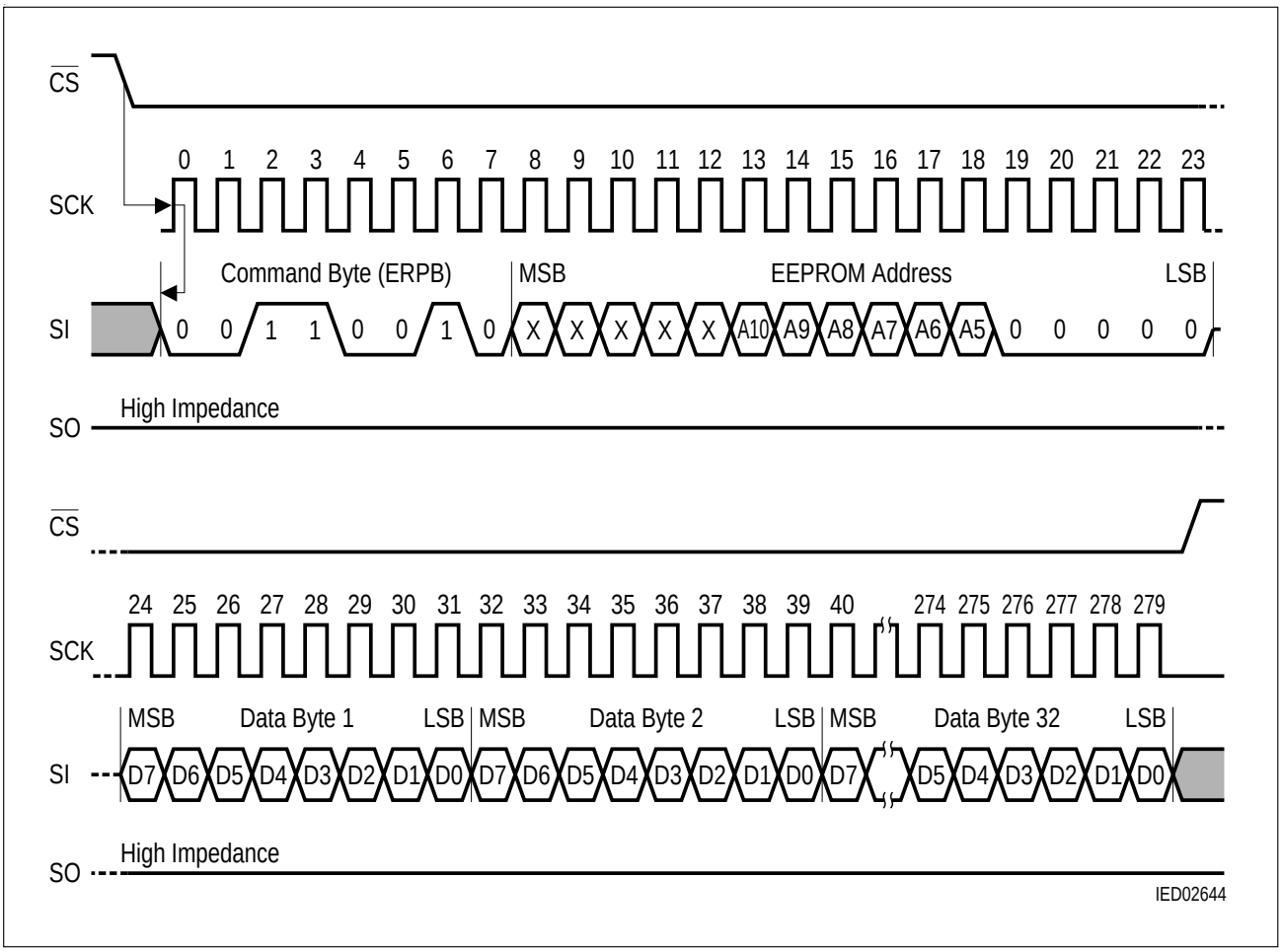


Figure 14
Sequence for Protection Bit Erase

For a successful programming of a protection bit, three conditions have to be fulfilled.

1. The page must be located within a block which is *not* protected by the status register bits PB0 and PB1.
2. The device must be write enabled via the write enable instruction (WREN), before the write (WRPB) or erase (ERPB) instruction can be executed.
3. All 256 bits of a page have to be verified successfully.

A successful programming is indicated by the EEPROM by setting the PPA-bit to “0” in the status register. The write or erase cycle is finished after 2.5 ms (typical).

7.3 Protection Bit Read

The status of the protection bit can be requested by the master. The byte sequence for protection bit read is shown in **figure 15**.

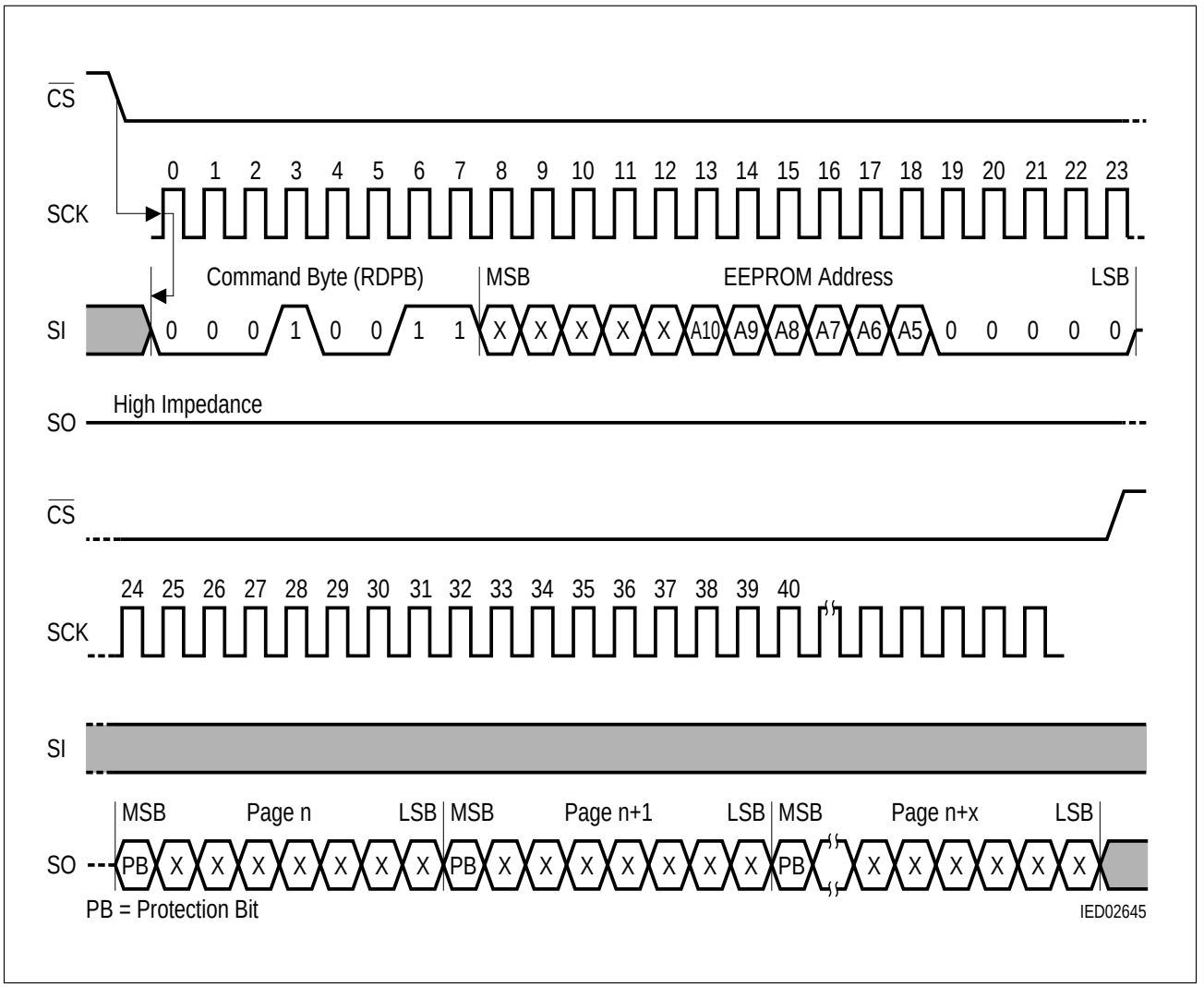


Figure 15
Byte Sequence for Protection Bit Read

To read the status of a protection bit the device must be selected with a high to low transition of the $\overline{CS}$ pin, then the RDPB command has to be send followed by the basis address of the respective page (A15-A11 are don't care bits, A10-A5, A4 to A0 = "0"). The first bit (MSB) of the transferred byte indicates the status of the protection bit of the addressed page. The other 7 bits are not valid. The page protection status is indicated as follows:

Protection Bit = 1: The Page Protection Mode™ is deactivated.

Protection Bit = 0: The Page Protection Mode™ is activated and data in the associated page are protected against changes.

To stop the transmission the device has to be deselected with a low to high transition of the $\overline{CS}$ pin. If not, the address counter is incremented automatically and the device will send the protection bit status of the next page. If the address of the highest page is reached, the address counter will roll over to the address of the lowest page.

8 Electrical Characteristics

The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at T_A = 25 °C and the given supply voltage.

8.1 Absolute Maximum Ratings

Stresses above those listed here may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this data sheet is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Table 11

Parameter		Limit Values	Units
Operating temperature	range 1 (industrial) range 2 (automotive)	– 40 to + 85 – 40 to + 125 (– 40 to + 150 on request)	°C °C °C
Storage temperature		– 65 to + 150	°C
Supply voltage		– 0.3 to + 7.0	V
All inputs and outputs with respect to ground		– 0.3 to V_{CC} + 0.5	V
ESD protection (human body model)		> 4000	V

8.2 DC Characteristics

Table 12

Parameter	Symbol	Limit Values			Units	Test Condition
		min.	typ.	max.		
Supply voltage	V_{CC}	2.7		5.5	V	
Supply current[1] (read)	I_{CC}		0.5		mA	V_{CC} = 5 V; f_c = 2.1 MHz
Supply current[1] (write)	I_{CC}		1		mA	V_{CC} = 5 V; f_c = 2.1 MHz
Standby current[2]	I_{SB}			3	µA	V_{CC} = 5 V

Table 12 (cont'd)

Parameter	Symbol	Limit Values			Units	Test Condition
		min.	typ.	max.		
Input leakage current	I_{LI}		0.1	3	µA	$V_{IN} = V_{CC}$ or V_{SS}
Output leakage current	I_{LO}		0.1	3	µA	$V_{OUT} = V_{CC}$ or V_{SS}
Input low voltage	V_{IL}	– 0.3		$0.3 \times V_{CC}$	V	
Input high voltage	V_{IH}	$0.7 \times V_{CC}$		V_{CC} + 0.5	V	
Output low voltage	V_{OL}			0.4	V	I_{OL} = 3 mA; V_{CC} = 5 V I_{OL} = 2.1 mA; V_{CC} = 3 V
Input/output capacitance (SI/SO)	$C_{I/O}$			8[3)]	pF	V_{IN} = 0 V; V_{CC} = 2.7 V
Input capacitance (other pins)	C_{IN}			6[3)]	pF	V_{IN} = 0 V; V_{CC} = 2.7 V

1) The values for I_{cc} are maximum peak values

2) Valid over the whole temperature range

3) This parameter is characterized only

8.3 AC Characteristics

Table 13

Parameter	Symbol	Limit Values V_{cc} = 2.7 - 5.5 V			Units
		min.	typ.	max.	
SCK clock frequency	f_{SCK}	0		2.1	MHz
Cycle time	t_{CYC}	475			ns
$\overline{CS}$ lead time	t_{LEAD}	250			ns
$\overline{CS}$ lag time	t_{LAG}	250			ns
Clock HIGH time	t_{WH}	200			ns
Clock LOW time	t_{WL}	200			ns
Data setup time	t_{SU}	100			ns
Data hold time	t_{H}	100			ns

Table 13 (cont'd)

Parameter	Symbol	Limit Values V_{CC} = 2.7 - 5.5 V			Units
		min.	typ.	max.	
Clock rise time	t_{RI}			2	µs
Clock fall time	t_{FI}			2	µs
$\overline{\text{Hold}}$ setup time	t_{HD}	100			ns
$\overline{\text{Hold}}$ hold time	t_{CD}	100			ns
$\overline{\text{CS}}$ deselect time	t_{CS}	500			ns
Output disable time	t_{DIS}			250	ns
Output valid from Clock LOW	t_V			200	ns
Output hold time	t_{HO}	0			ns
Output rise time	$t^{1)}_{RO}$			200	ns
Output fall time	$t^{1)}_{FO}$			200	ns
Rising edge of $\overline{\text{Hold}}$ to output out of Z	t_{LZ}			100	ns
Falling edge of $\overline{\text{Hold}}$ to output on Z	t_{HZ}			100	ns
SI/SO and SCK spike suppression time at constant inputs	t_I		50		ns

1) This parameter is characterized only

8.4 Erase and Write Characteristics

Table 14

Parameter	Symbol	Limit Values V_{CC} = 2.7-5.5 V		Units
		typ.	max.	
Erase + write cycle (per page)	t_{WC}	5	8	ms
Erase page protection bit		2.5	4	ms
Write page protection bit		2.5	4	ms

8.5 Timing Diagrams

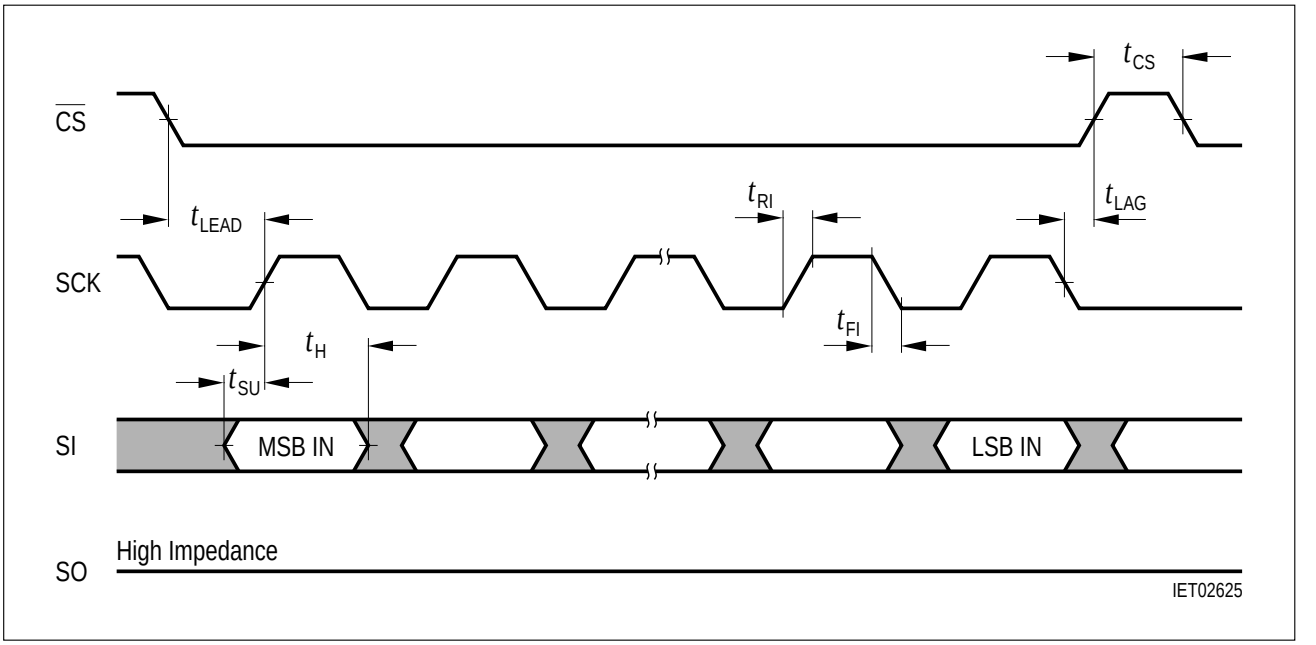


Figure 16
Bus Timing for Serial Input

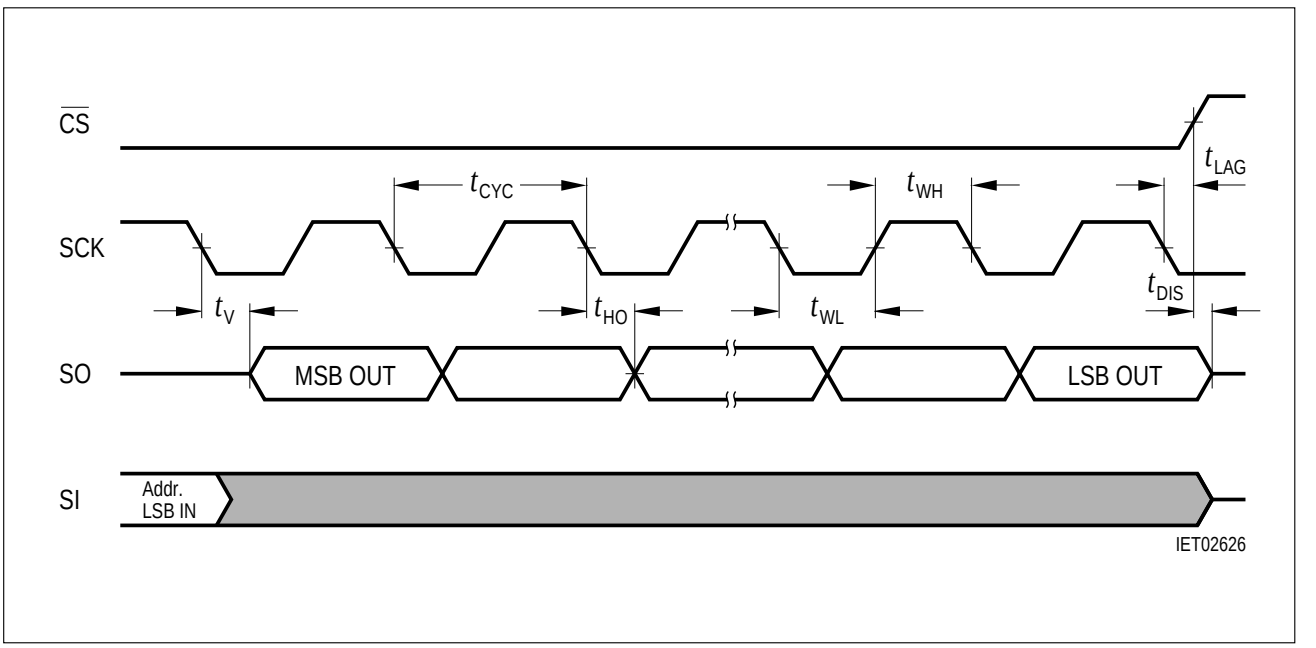


Figure 17
Bus Timing for Serial Output

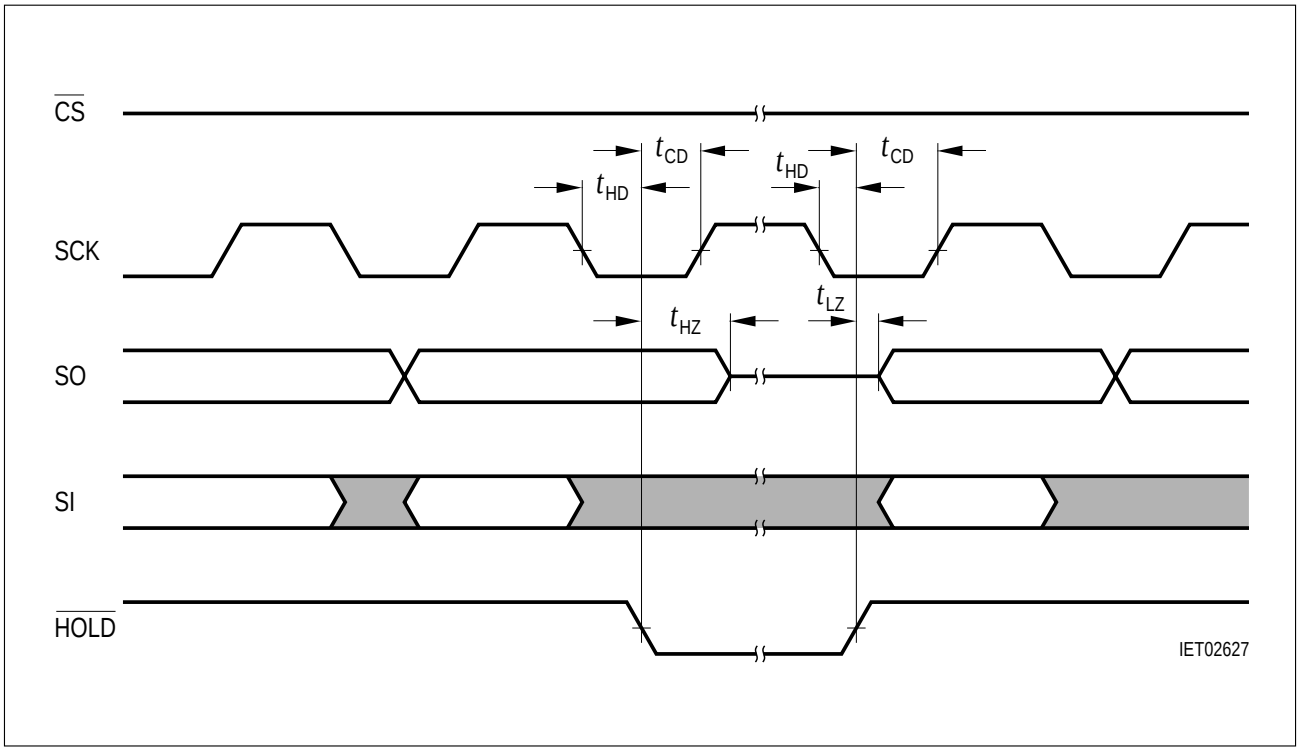
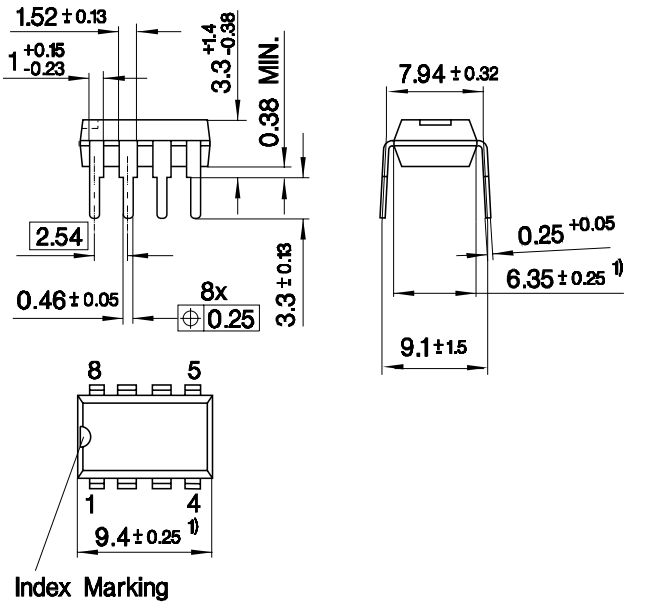


Figure 18
Hold Timing

9 Package Outlines

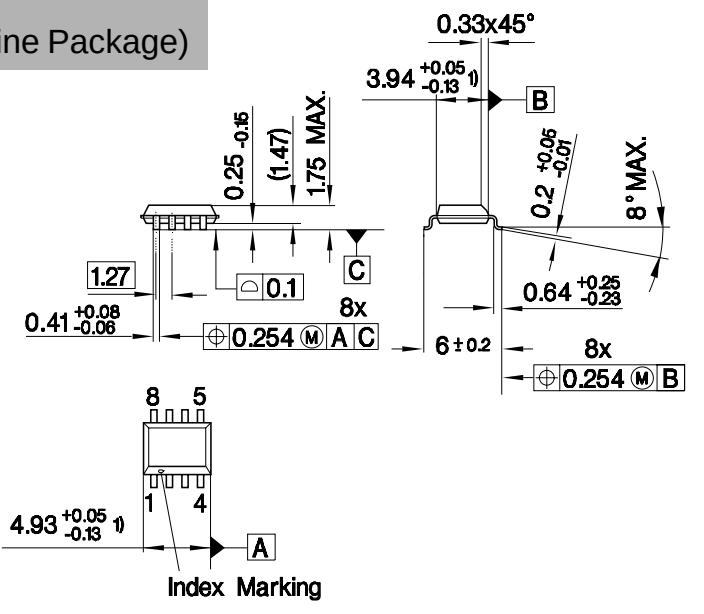
P-DIP-8-3
(Plastic Dual In-line Package)



1) Does not include plastic or metal protrusion of 0.25 max. per side

GPD05696

P-DSO-8-2
(Plastic Dual Small Outline Package)



1) Does not include plastic or metal protrusion of 0.15 max. per side

GPS05473

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

SMD = Surface Mounted Device

Dimensions in mm