XC2318/L HardWire™ Array Family

Product Specification

Features

- Mask-programmed version of Xilinx Field Programmable Gate Arrays (FPGA)
  - Cost reduction for high volume applications
  - Transparent conversion from FPGA device
  - On-chip scan path test latches
  - High Performance CMOS process
  - 70 MHz flip-flop toggle rate
  - 5 volt and 3.3 volt operation
- Easy conversion from Programmable FPGA
  - Architecturally identical to Programmable FPGA
  - Pin and performance compatible
  - Same specifications as Programmable FPGA
  - Supports daisy-chained configuration
  - Test program automatically generated
- Flexible High-Performance Architecture
  - User-definable I/O functions
  - 100% factory tested
  - Low-power CMOS technology
  - Complete development system support

Description

The Xilinx Logic Cell Array family provides a group of high-performance, high-density digital integrated circuits. Their regular, extendable, flexible architecture is composed of three types of configurable elements: a perimeter of IOBs, a core array of CLBs and circuitry for interconnection. The general structure of a Logic Cell Array device is shown in Figure 1.

The Xilinx XC2318 HardWire Array device is a mask programmed version of the Xilinx XC2018 and XC2064 FPGA. In high-volume applications where the design is stable, the FPGAs used for prototyping and initial production can be replaced by their HardWire array equivalents. This offers a significant cost reduction with virtually no risk or engineering resources required.

In an FPGA device the logic functions and interconnections are determined by the configuration program data loaded and stored in internal static memory cells. The HardWire LCA architecture identical to the FPGA it replaces. All CLBs, IOBs, interconnect topology, power distribution and other elements the same. In the HardWire array the memory cells and the logic they control are replaced by metal connections. Thus the HardWire array is a semicustom device manufactured to provide a customer specific function, yet is completely compatible with the FPGA device it replaces.

Xilinx manufactures the HardWire Array using information from the FPGA design file. Since the HardWire Array device is both pinout and architecturally identical with the FPGA, it is easily created without the need for all the costly and time-consuming engineering activities which other semicustom solutions would require. No redesign time; no expensive and time consuming simulation runs; no place and route; no test vector generation. The combination of the Programmable and HardWire Array products simply offer the fastest and easiest way to get your product to market, and ensures a subsequent low-cost, low-risk high-volume cost reduction path.

Electrical Characteristics

The XC2318 HardWire Array family is form, fit and function compatible with the XC3000 FPGA family.

Table 1. Summary of HardWire Product Availability For the XC2000 Family

HardWire Device	Replacement for Pin-Compatible Programmable Device	Total Available Gates	Maximum Flip-Flop Toggle Frequency	Packages						
					VQFP	PLCC		PQFP		TQFP VQFP
				Pins	64	68	84	64	100	100
XC2318/L	XC2018, XC2064	1800	70 MHz	I/Os	54	58	74	54	74	74

Accordingly, all XC2318 HardWire devices meet the electrical specifications of the respective XC2000 FPGA device for the -100 Speed Grade. For specific data, please see the XC2000 section of the Xilinx Programmable Logic Data Book. Absolute Maximum Ratings, Operating Conditions, DC Characteristics and Switching Characteristics of the -100 Speed Grade of the appropriate device type apply.

Architecture

As shown in Figure 1, the HardWire Array has the same architecture as the FPGA it replaces. The perimeter of I/O Blocks (IOBs) provides an interface between the internal logic array and the device package pins. The array of Configurable Logic Blocks (CLBs) performs user-specified logic functions. The interconnect resources are programmed to form networks carrying logic signals among blocks, analogous to printed circuit board traces connecting SSI/MSI packages.

The logic functions of the blocks are implemented by look-up tables. Functional options are implemented by user-defined multiplexers. Interconnecting networks between blocks are implemented with user-defined fixed metal connections.

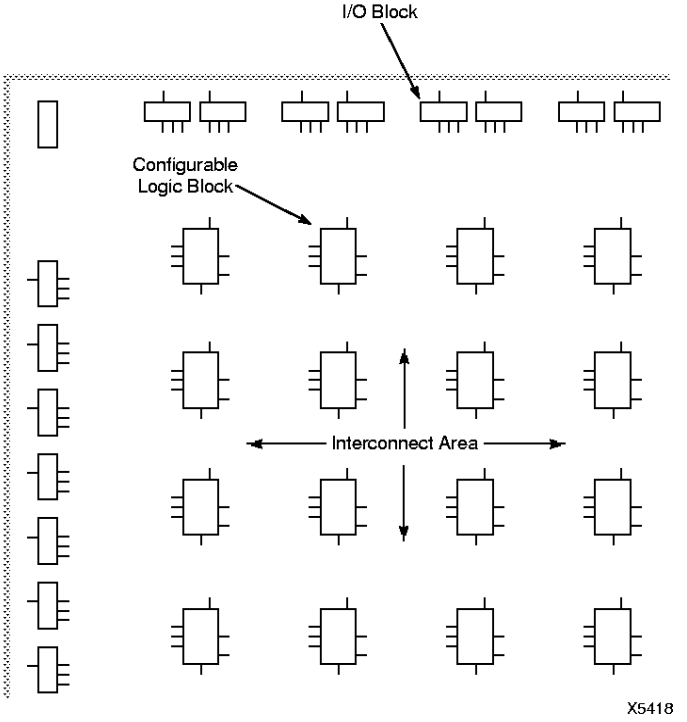


Figure 1. Logic Cell Array Structure

I/O Block

Each user-defined IOB (shown in Figure 2) provides an interface between the external package pin of the device and the internal user logic. The IOB is identical with that used in the FPGA. There are a wide variety of I/O options available to the user.

Summary of I/O Options

- Inputs
  - Direct/Flip-flop
  - CMOS/TTL threshold (chip inputs)
  - Pull-up resistor/open circuit
- Outputs
  - 3-state/on/off
  - 3-state/output enable (inverse)

Configurable Logic Block

The array of Configurable Logic Blocks (CLBs) provides the functional elements from which the user's logic is constructed. The logic blocks are arranged in a matrix within the perimeter of IOBs. The XC2318 has 100 such blocks arranged in 10 rows and 10 columns.

The configurable logic block is identical to that used in the XC2000 family of FPGA devices. Each configurable logic block has a combinatorial logic section, a storage element, and an internal routing and control section. Each CLB has four general-purpose inputs: A, B, C and D; and a special clock input (K), which may be driven from the interconnect adjacent to the block. Each CLB also has two outputs, X and Y, which may drive interconnect networks. Figure 3 shows the resources of a Configurable Logic Block.

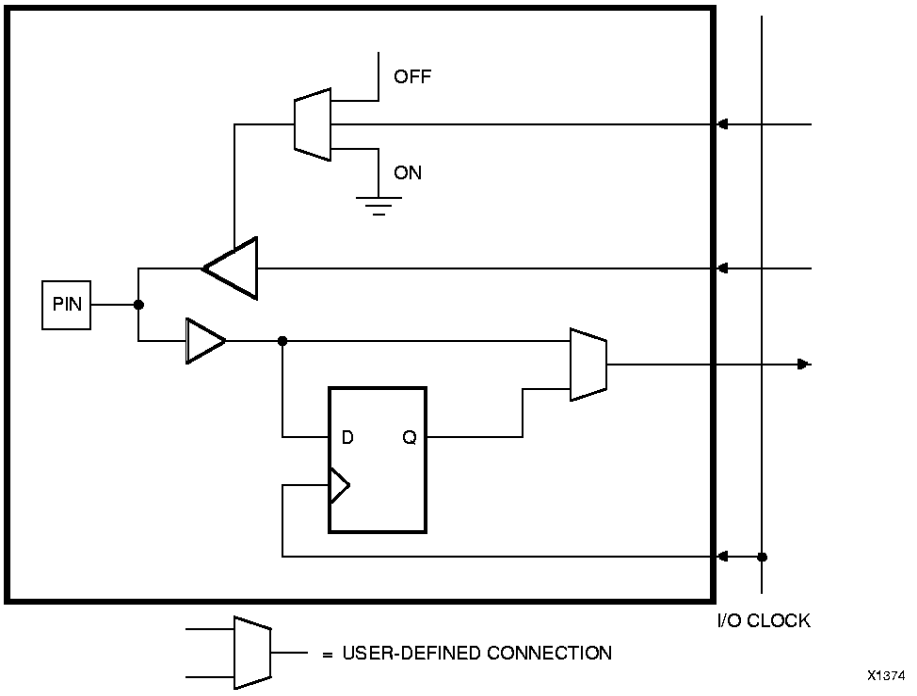


Figure 2. Input/Output Block. Each IOB includes an input storage element and I/O options pre-defined by the user. Passive pull-up can only be enabled on inputs, not on outputs. All user inputs are selectable for TTL or CMOS thresholds.

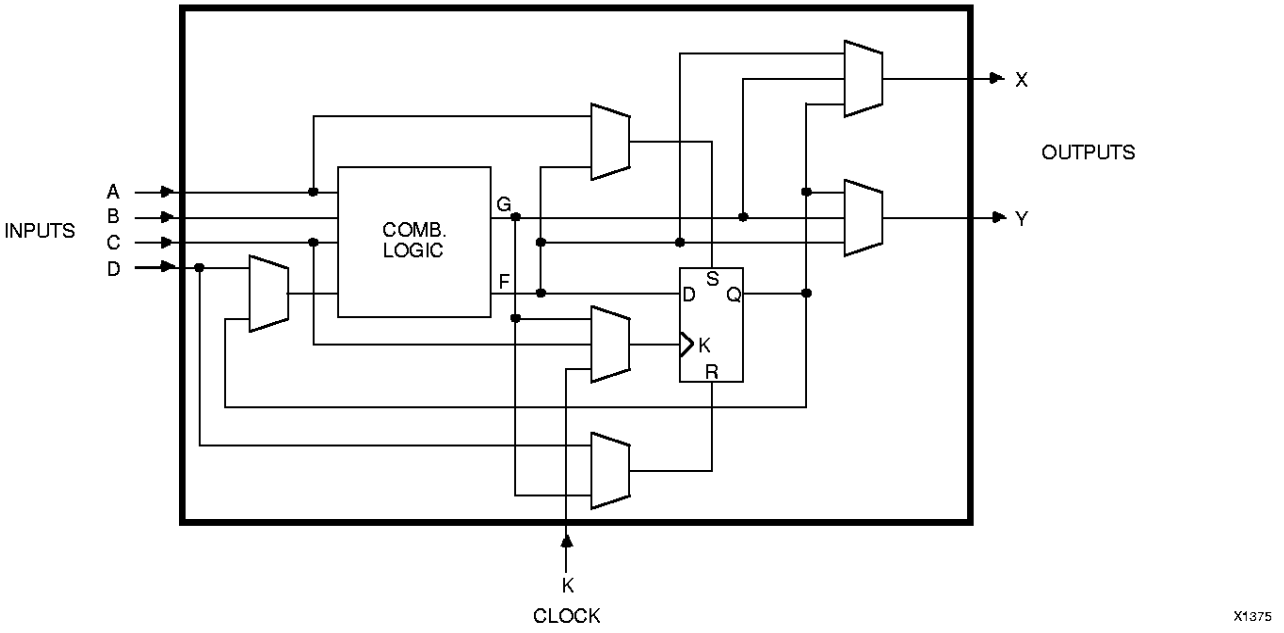


Figure 3. Configurable Logic Block

Interconnect

User-defined interconnect resources in the Logic Cell Array provide routing paths to connect inputs and outputs of the I/O and logic blocks into logic networks. Interconnections between blocks are composed from a two-layer grid of metal segments. The XACT development system provides automatic routing of these interconnections. The inputs of the IOBs and CLBs are multiplexers that are defined to select an input network from the adjacent interconnect segments.

Three types of metal resources are provided to accommodate various network interconnect requirements:

- General Purpose Interconnect
- Direct Connection
- Long Lines

The topology of all these interconnect resources is identical with that of the FPGA, but the speed of the interconnect paths is significantly faster (since all interconnections are fixed metal connections).

Configuration and Start-Up

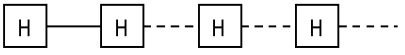
The start-up sequence of the XC2318 HardWire Array is generally similar to that of the XC2000 FPGA. However, there are some differences which need to be considered before using the HardWire device in a socket designed for the programmable part. While the XC2318 does not require the loading of configuration data, it does support certain configuration modes.

Configuration

The XC2318 HardWire device can be used stand-alone or in a daisy chain with other arrays. It does not produce CCLKs, and therefore cannot operate in Master Mode. Peripheral Mode is also not supported.

Example 1. As a stand alone HardWire Array.

Example 2. As a daisy chain of all HardWire Arrays.



Example 3. As a HardWire Array or programmable slave in a daisy chain with a Programmable device as a master.

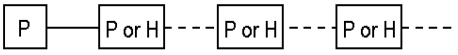


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Figure 4.

A HardWire device will not "swallow" its own configuration data. If the appropriate mask option is selected, whatever configuration bits are fed into the DIN pin will appear on the DOUT pin after a delay. If not, DOUT will be held in a high impedance state. In any case where a HardWire Array device is ahead of a FPGA in a daisy chain (as in example 3 shown below) the configuration data will need to be modified. (See Mask Options Applications Note page 5-3 for further information).

Start-up Sequence

The XC2318 HardWire Array start-up sequence has a number of differences from that of the XC2000 FPGAs. An internal power-on-reset circuit is triggered when power is applied. When V_{CC} reaches the voltage at which portions of the array begin to operate, the device enters a time-out period. During the time-out period the I/O buffers are disabled and a high-impedance pull-up resistor is provided for the user I/O pins. The length of this time-out period is user-defined to be either 64 µs or 16 ms.

The 64 µs period is used for a rapid reset cycle; the 16 ms period emulates the power-on sequence of an FPGA device.

After the time-out period the D/P pin will be released. When it goes High the I/O pins become active immediately, and the HDC and LDC pins become inactive. The time-out period can be extended by holding the D/P pin Low. If the XC2318 is in a daisy chain with FPGAs all the D/P pins should be tied together. This will ensure a synchronous start-up of all devices in the chain.

Performance

The single parameter which most accurately describes the overall performance of the Logic Cell Array is the maximum toggle rate for a logic block storage element configured as a toggle flip-flop. The configuration for determining the toggle performance of the Logic Cell Array is shown in Figure 5. The clock for the storage element is provided by the global clock buffer and the flip-flop output Q is fed back through the combinatorial logic to form the data input for the next clock edge.

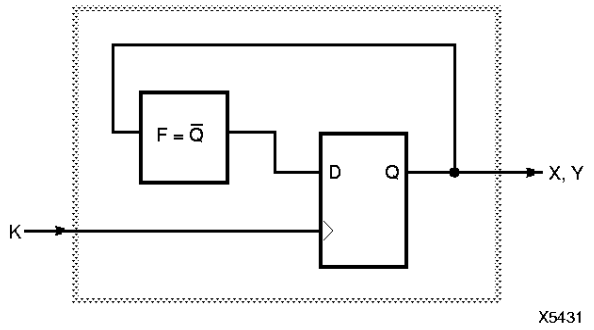

Figure 5. Logic Block Configuration for Toggle Rate Measurement

Actual array performance is determined by the timing of critical paths, including the timing for the logic and storage elements in that path and the timing of the associated interconnect. HardWire logic block performance is equal to or slightly faster than the equivalent FPGA device, while the interconnect performance is significantly faster.

All HardWire devices are specified and tested for operation at the fastest equivalent FPGA speed available at the time the HardWire device is introduced. For the XC2318, this means all parts are guaranteed to the -70 speed grade. Since the finished HardWire array product is customized for a specific customer and application, speed grading is not available.

Power

Power for the HardWire array is distributed through a grid to achieve high noise immunity and isolation between logic and I/O. Inside the array, dedicated V_{CC} and ground rings surround the logic array and provide power to the I/O drivers. (See Figure 6.) An independent matrix of V_{CC} and ground lines supplies the interior logic of the device. This power distribution grid provides a stable supply and ground for all internal logic, providing the external package power pins are all connected and appropriately decoupled. Typically a 0.1 µF capacitor connected near the V_{CC} and ground pins will provide adequate decoupling.

Output buffers capable of driving the specified 4 mA loads under worst-case conditions may be capable of driving 25 to 30 times that current in a best case. Noise can be reduced by minimizing external load capacitance and reducing simultaneous output transitions in the same direction. It may also be beneficial to locate heavily loaded output buffers near the ground pads.

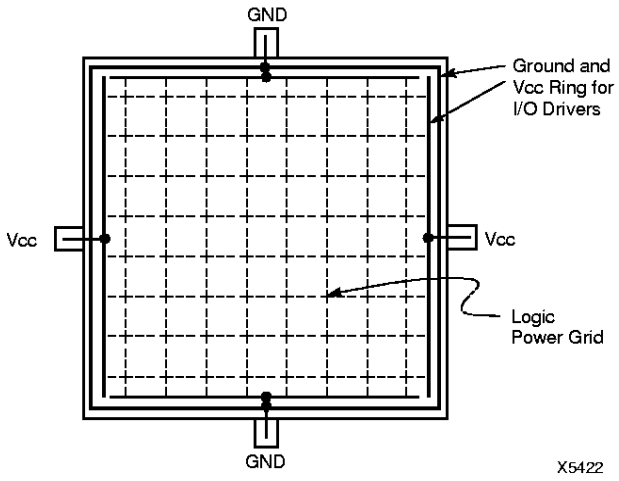

Figure 6. LCA Power Distribution.

3 V/5 V Considerations

The XC2300 HardWire Array can operate either as 5 volt only, or as a 5 volt tolerent 3.3 volt device (part number XC2300L).

Table 2. 5 Volt and 3.3 Volt Operation

	5 Volt Operation				3.3 Volt Operation			
	Vil (max)	Vih (min)	Vol (max)	Voh (min)	Vil (max)	Vih (min)	Vol (max)	Voh (min)
XC2300	0.80	2.00	0.40	2.40	0.80	2.00	0.40	2.40

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HardWire Array Testability

The HardWire Array products contain significant on-chip logic to facilitate manufacturability and testing. This logic, combined with Xilinx's internal Automatic Test Generation (ATG) software, assures 100% functionality. In fact, the HardWire Array can be 100% functionally tested by Xilinx without the need for customer generated test vectors (as is required with custom gate arrays).

This section examines the two basic block structures and the special test circuitry in the HardWire Array.

Test Architecture

The HardWire Array contains two types of internal blocks: the Input/Output Block (IOB) and the Configurable Logic Block (CLB). To accomplish 100% functional testing, special test circuitry is designed into the device. This circuitry allows testing of each block (CLB and IOB) in a synchronized procedure known as "Scan Test". Special dedicated test latches (called TBLKs) are included on all HardWire devices. They are completely transparent to the normal operation of the circuit. Scan testing allows the contents of all internal flip-flops to be serially shifted off-chip, and for Xilinx generated test vectors to be shifted into the device, thus enabling all flip-flops to be initialized to any desired state.

These special dedicated test latches are placed into each CLB and IOB. Each CLB has four internal test latches, (placed at the CLB outputs), while each IOB contains four test latches (placed at the IOB inputs) as shown in Figures 7 and 8. The placement of these test latches is very important, since each CLB output or IOB input can fanout to multiple destinations. All sources and destinations of logic blocks come from other logic blocks. Therefore, this placement of the latches provides complete access to all nets and synchronized control of all CLBs and IOBs.

The test latches are connected into a daisy chain which passes through every flip-flop in the array. Figure 9 shows an overview of the scan path. The path begins at the Scan In pin, sequences through each CLB, then through the IOBs, and finally exits at the Scan Out pin. This scan path can be seen in more detail in Figure 10, which shows the precise sequence with which the CLB and IOB internal test latches are loaded or read.

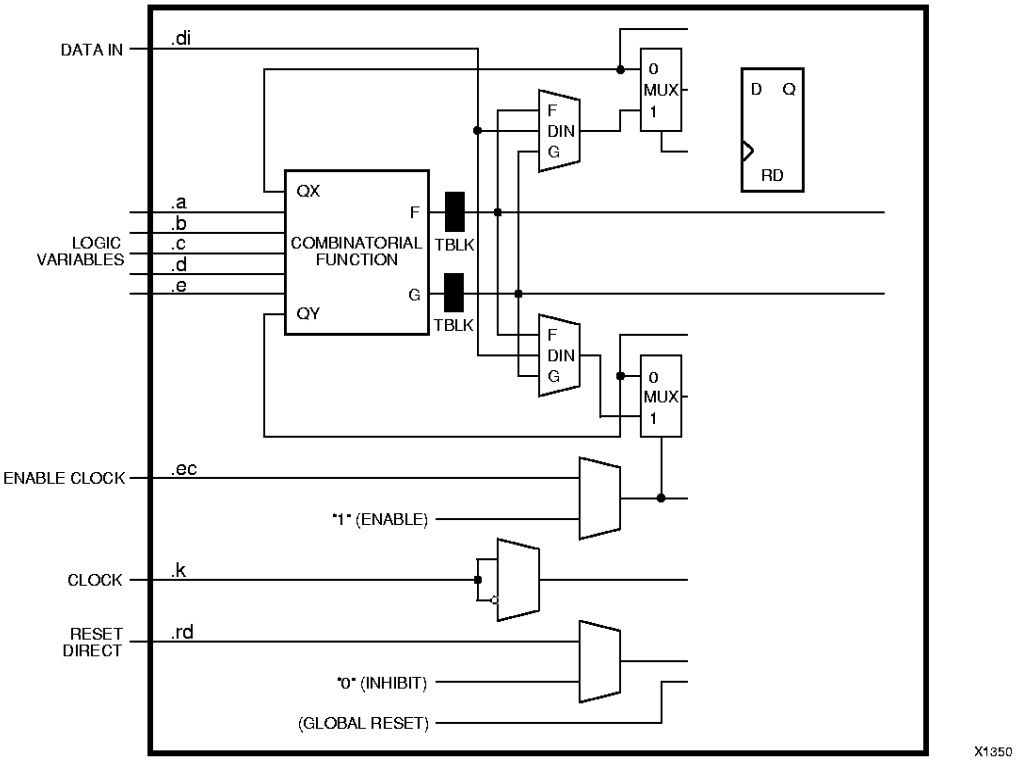

Figure 7. HardWire CLB Test Latch Locations

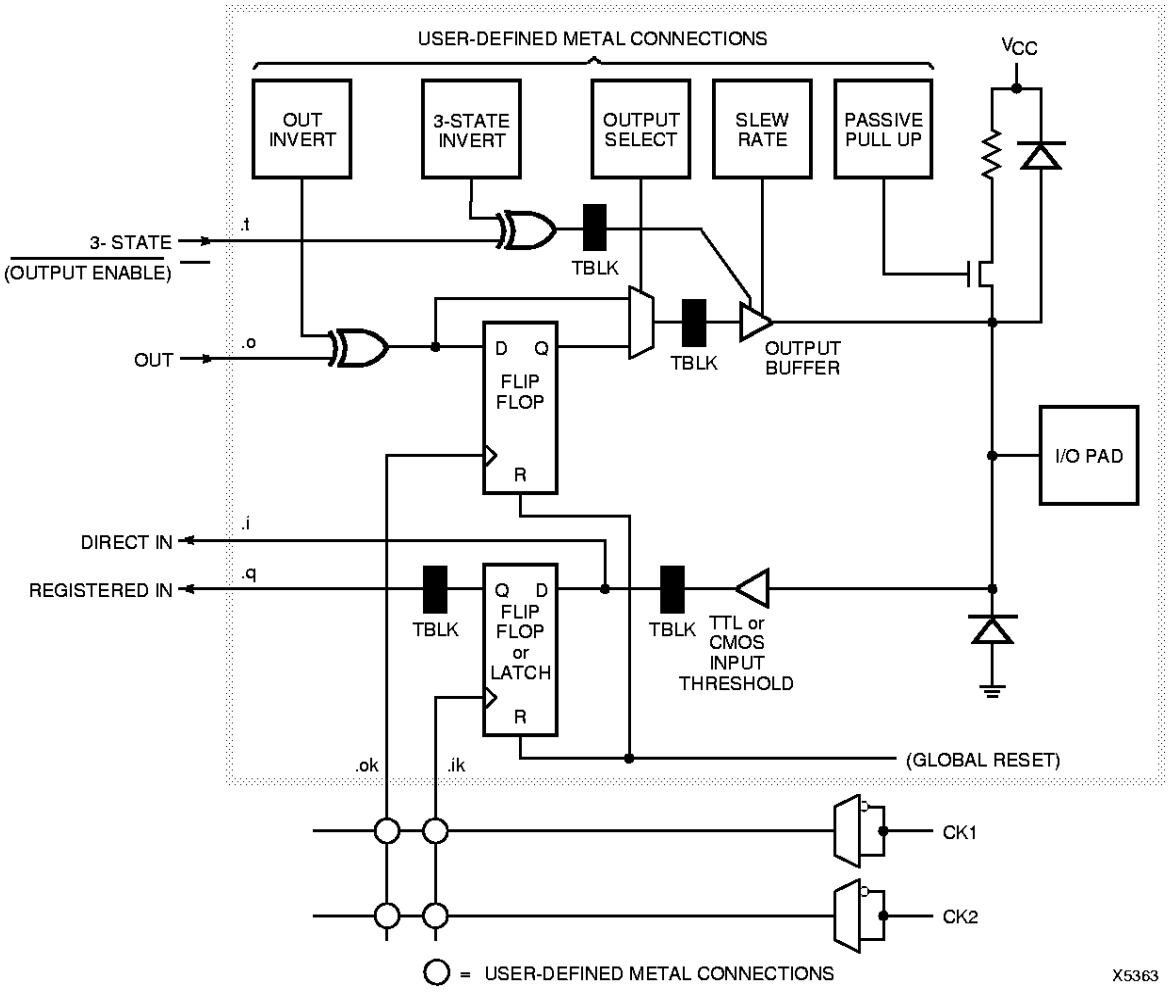

Figure 8. HardWire IOB Test Latch Location

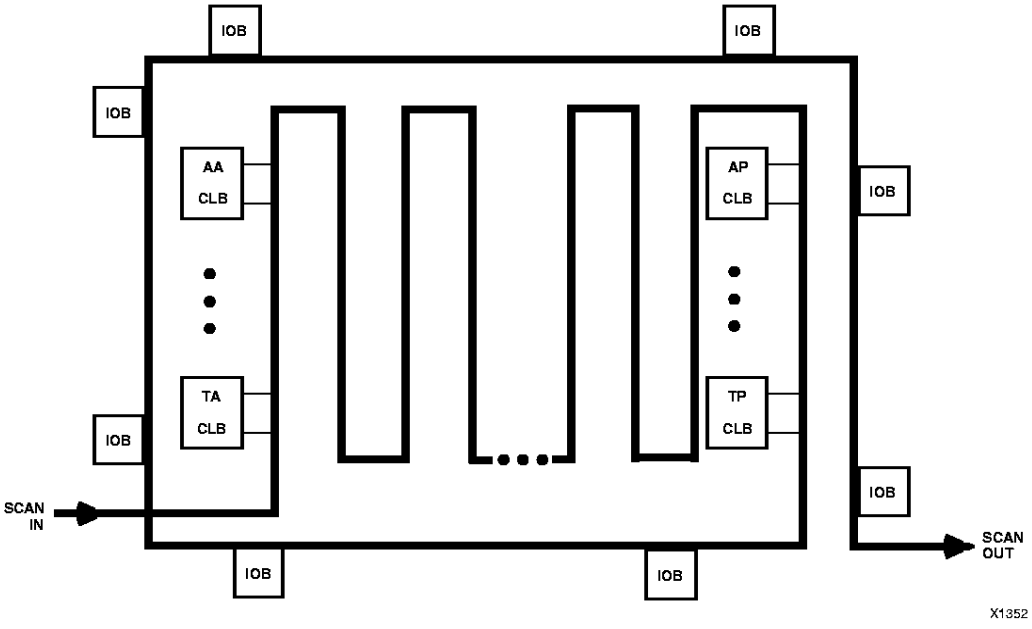

Figure 9. Scan Path Overview

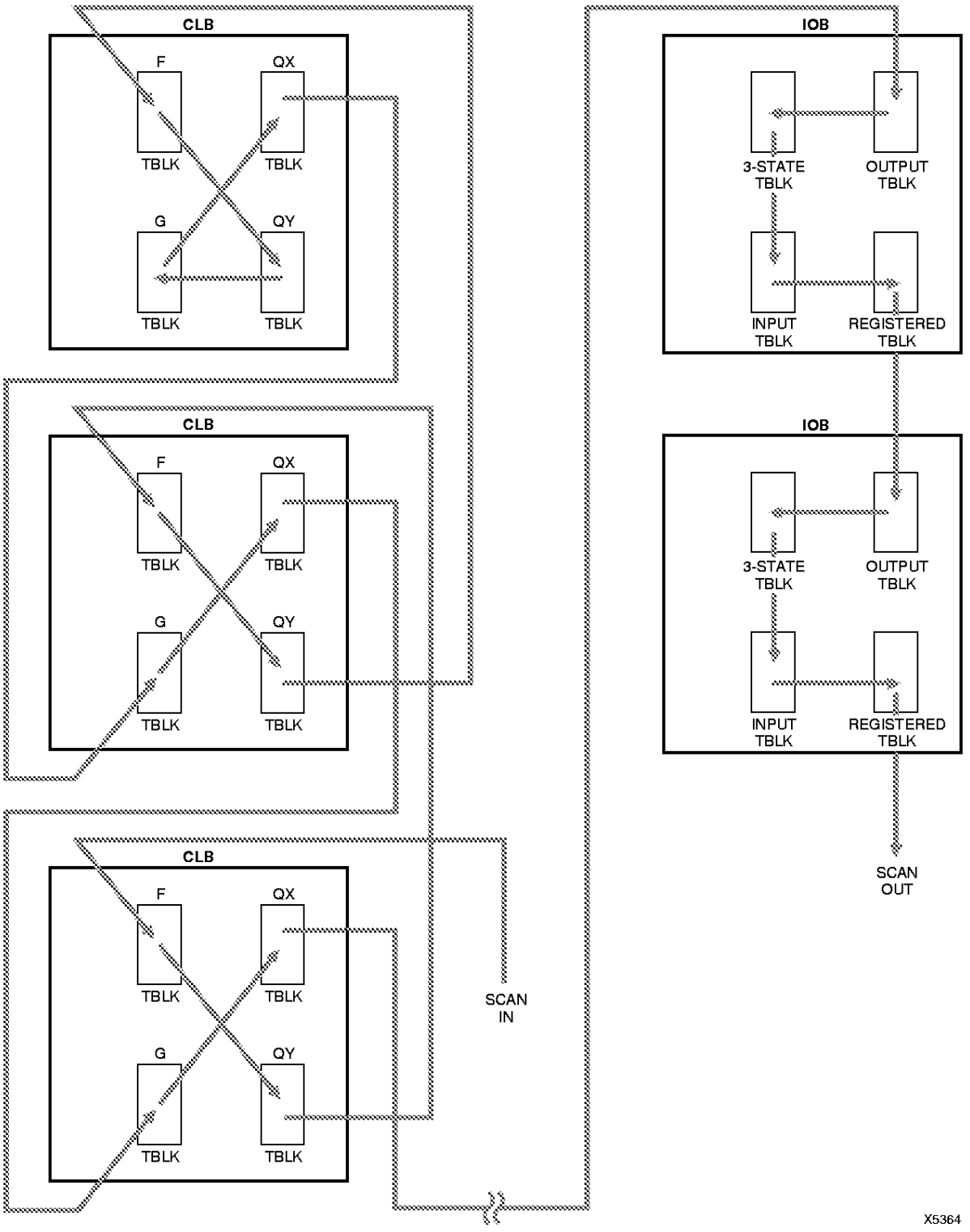

Figure 10. Detailed Scan Path

The internal architecture of a TBLK is shown in Figure 11. In the normal operation mode of the HardWire array, SW1 is in position A and all the test latches are bypassed completely. The HardWire Array device is set into Test Mode (SW1 = position B) by Xilinx ATG software. This software inputs unique conditions on several control pins while serially loading a "password" into the device. For this reason, it is not possible for a customer design to inadvertently place the HardWire Array into Test Mode. When SW1 is in position B (Test Mode) all the latches can receive data from either the CLB output or the previous latch in the daisy chain (SQn).

Synchronized together by a special test clock, all the test latches operate in two phases. The first phase serially loads all the latches to place a specific vector at the inputs of the logic block to be tested. The second phase is a parallel load of all latches, storing the expected output data of the logic block being tested (SW2 = A). At this point testing returns to phase one and serially clocks out the results, while simultaneously clocking in a new input vector.

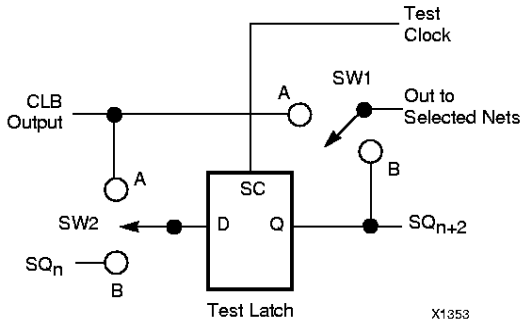

Figure 11. TBLK Block Diagram

Scan Test

To see how scan testing can be used to provide complete functional test coverage, consider the logic shown in Figure 12. This diagram shows a CLB (CLB2) with two inputs being driven by two different CLBs and the other two inputs being driven by two different IOBs. If we apply every possible combination of inputs to CLB2 and all expected output conditions are met, then CLB2 has been 100% functionally tested. The input conditions applied also include any register control signals (such as Clock, Reset, or Clock Enable). The same procedure is used for testing IOBs.

Looking again at Figure 12, CLB2 is tested by first serially loading the X output latches of CLB1 and CLB3 and the input latches of IOB1 and IOB2. Note that the latches on CLB2's outputs are also loaded in this first phase. Not all CLBs and IOBs can be tested at once, due to signal dependencies. To position the correct data into the latches all unused latches still need "don't cares" loaded. Regardless of which CLBs and IOBs are being tested by a particular scan vector, the complete scan path is always shifted in and out for testing and verification. The state of CLB2's output latches will be opposite to their expected results in phase two. This guarantees that CLB2's input data changed the state of its output latches and therefore, is current data.

CLB or IOB data registers using a synchronous or asynchronous clock are not a problem during this special test mode. All customer-used registers are clock inhibited during the phase one load. The inhibit of register clocking is accomplished by logically "ANDing" the register clocks with the global inhibit control line.

The test vectors needed to perform this thorough testing are created by Xilinx. No additional effort or engineering time is required from the user to ensure proper device performance. The customer design file used to create the HardWire Array is used in conjunction with specially developed Xilinx Automatic Test Generation software. This creates the complete set of test vectors required to perform 100% functional testing. This software creates the data for all possible input conditions and corresponding output data for each CLB and IOB used in the customer design. This data is then compiled into the test vectors used to perform the actual testing.

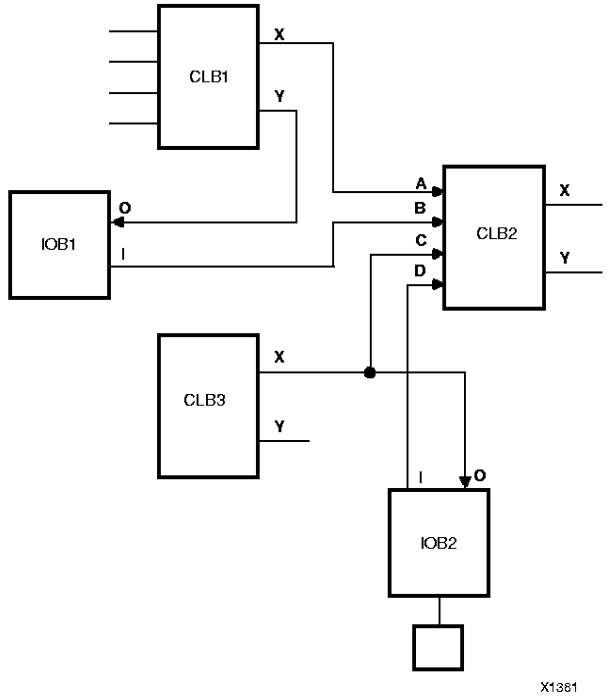

Figure 12. Four Input CLB (CLB2) Driven by Two Different CLB Outputs and Two different IOB Outputs

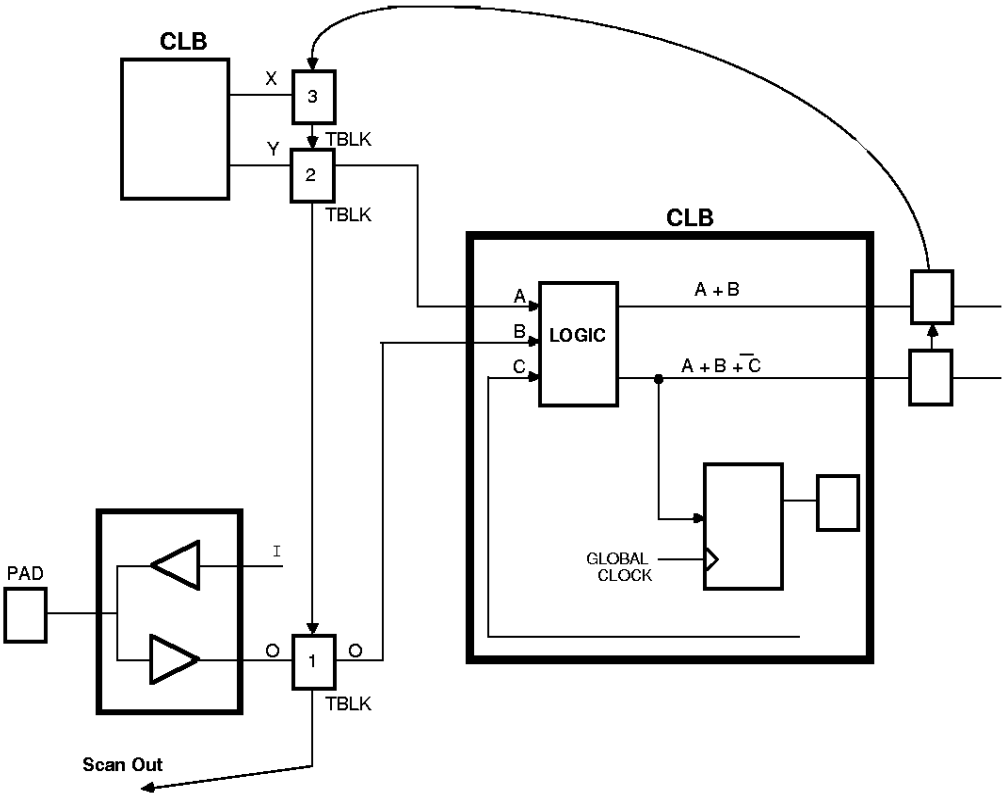

Figure 13. XC2318 Scan Test Example

The following vectors and comments show the testing of one input condition (input A of the CLB under test).

SCAN CLOCK	SCAN IN	SCAN OUT	GLOBAL CLOCK	COMMENTS
C	1	X	X	Load a 1 into Scan In pin, knowing it will be positioned in latch #1, input B. The global clock is inhibited and the scan out data are "don't cares".
C	1	X	X	Load a 1 into Scan In pin for input A.
C	X	X	X	Load a "don't care" (0 or 1) into latch #3, not used.
C	0	X	X	Load a 0 into latch #4, expecting the X output to be a 1 after phase two.
C	0	X	X	Load a 0 into latch #5, expecting the Y output to be a 1 after phase two.
C	0	X	X	Load a 0 into Scan #6, expecting the register output to be a 1 after phase two.
At this point all the latches are loaded. Enter phase two by changing the control pin (not shown here).				
0	X	X	C	Clock the data register after entering phase two. Now the register data is current but Latch #6 still has a 0 inside.
C	X	X	0	Load all the latches with their functional results.
This completes phase two. Return to phase one and load the next set of input data, while simultaneously verifying the scan out pin. We expect to see latches 4, 5, and 6 with ones as we scan the data out.				
C	1	X	X	Load a 1 into Scan In pin, knowing it will be positioned in latch #1, input B.
				The global clock is inhibited and the first three Scan Out data are "don't cares".
C	0	X	X	Load a 0 into Scan In pin for input A. This is the difference from the first load.
C	X	X	X	Load a "don't care" into latch #3, not used.
C	1	1	X	Load a 1 into latch #4, expecting the X output to be a 0 after phase two (input A = 0).
				The Scan Out pin will be showing the results of latch 4 from the previous load.
C	0	1	X	Load a 0 into latch #5, expecting the Y output to be a 1 after phase two.
				The Scan Out pin shows latch 5 results.
C	0	1	X	Load a 0 into latch #6, expecting the register output to be a 1 after phase two.
				Scan Out pin shows latch 6 results.

Figure 14. Sample Test Vectors for XC2318 Simple Design Example

CONFIGURATION MODE		64 VQFP	68 PLCC	84 PLCC		100 TQFP/ VQFP	USER OPERATION
GND		8	1	1		13	GND
<<HIGH>>		9	2	2		14	I/O
				3		15	
				4		16	
		10	3	5		17	
		11	4	6		18	
		12	5	7		19	
		13	6	8		20	
		14	7	9		21	
		15	8	10		22	
		16	9	11		23	
PWRDWN (I)		17	10	12		26	PWR DWN
<<HIGH>>		18	11	13		27	I/O
		19	12	14		29	
		20	13	15		30	
			14	16		32	
		21	15	17		33	
				18		34	
		22	16	19		35	
				20		36	
		23	17	21		37	
Vcc		24	18	22		38	Vcc
<<HIGH>>		25	19	23		39	I/O
				24		40	
		26	20	25		41	
				26		42	
		27	21	27		43	
		28	22	28		45	
		29	23	29		47	
		30	24	30		48	
M1 (LOW or HIGH)		31	25	31		49	M1 (LOW or HIGH)
M0 (LOW or HIGH)		32	26	32		51	M0 (LOW or HIGH)
		33	27	33		53	I/O
HDC (HIGH)		34	28	34		54	
<<HIGH>>		35	29	35		55	
LDC (LOW)		36	30	36		56	
<<HIGH>>		37	31	37		57	
		38	32	38		58	
				39		59	
		39	33	40		60	
		40	34	41		61	
				42		62	
GND		41	35	43		63	GND
<<HIGH>>				44		64	I/O
		42	36	45		65	
			37	46		66	
		43	38	47		67	
				48		68	
		44	39	49		69	
			40	50		70	
		45	41	51		71	
		46	42	52		72	
		47	43	53		73	XTL2 OR I/O
		48	44	54		75	RESET
DONE (O)		49	45	55		77	PROG (I)
<<HIGH>>		50	46	56		78	XTL1 OR I/O
		51	47	57		79	I/O
		52	48	58		80	
				59		82	
		53	49	60		84	
				61		85	
		54	50	62		86	
		55	51	63		87	
Vcc		56	52	64		88	Vcc
<<HIGH>>		57	53	65		89	I/O
		58	54	66		90	
				67		91	
		59	55	68		92	
				69		93	
		60	56	70		95	
		61	57	71		96	
DIN (I)		62	58	72		97	
DOUT (O)		63	59	73		98	
CCLK (I)		64	60	74		99	CCLK (I)
<<HIGH>>		1	61	75		2	I/O
		2	62	76		3	
		3	63	77		5	
		4	64	78		6	
			65	79		7	
		5	66	80		8	
		6	67	81		9	
				82		10	
				83		11	
		7	68	84		12	

<<HIGH>> IS HIGH IMPEDANCE WITH A 20-5 kΩ INTERNAL PULL-UP DURING CONFIGURATION

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Table 3. XC2318 Pin Assignments