54F/74F825

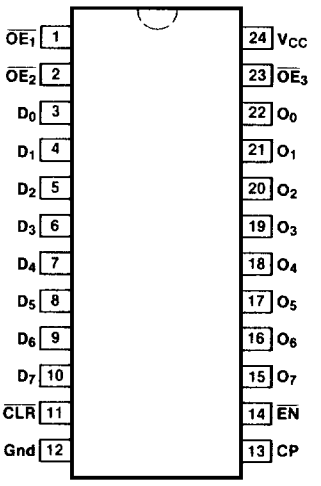
8-Bit D-Type Flip Flop

Description
The 'F825 is an 8-bit buffered register. It has Clock Enable and Clear features which are ideal for parity bus interfacing in high performance microprogramming systems. Also included in the 'F825 are multiple enables that allow multiuser control of the interface.

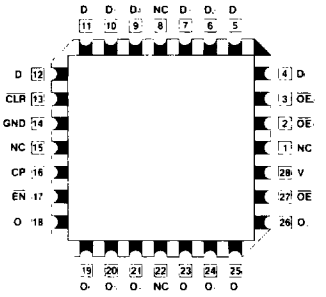
The 'F825 is fully compatible with AMD's AM29825.

Ordering Code: See Section 5

Connection Diagrams

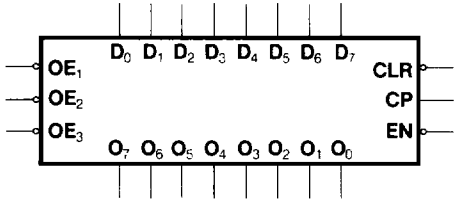


Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Logic Symbol



Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
D_0-D_7	Data Inputs	0.5/0.375
O_0-O_7	Data Outputs	75/15 (12.5)
$\overline{OE}_1$, $\overline{OE}_2$, $\overline{OE}_3$	Output Enable	0.5/0.375
$\overline{EN}$	Clock Enable	0.5/0.375
$\overline{CLR}$	Clear	0.5/0.375
CP	Clock Input	0.5/0.75

Functional Description

The 'F825 consists of eight D-type edge-triggered flip-flops. This device has 3-state true outputs for bus systems, organized in a broadside pinning. In addition to the clock and output enable pins, the buffered clock (CP) and buffered Output Enable ($\overline{OE}$) are common to all flip-flops. The flip-flops will store the state of their individual D inputs that meet the setup and hold times requirements on the LOW-to-HIGH CP transition. With the $\overline{OE}$ LOW, the contents of the flip-flops are available at the outputs. When the $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops. The 'F825 has Clear ($\overline{CLR}$) and Clock Enable ($\overline{EN}$) pins. These pins are ideal for parity bus interfacing in high performance systems.

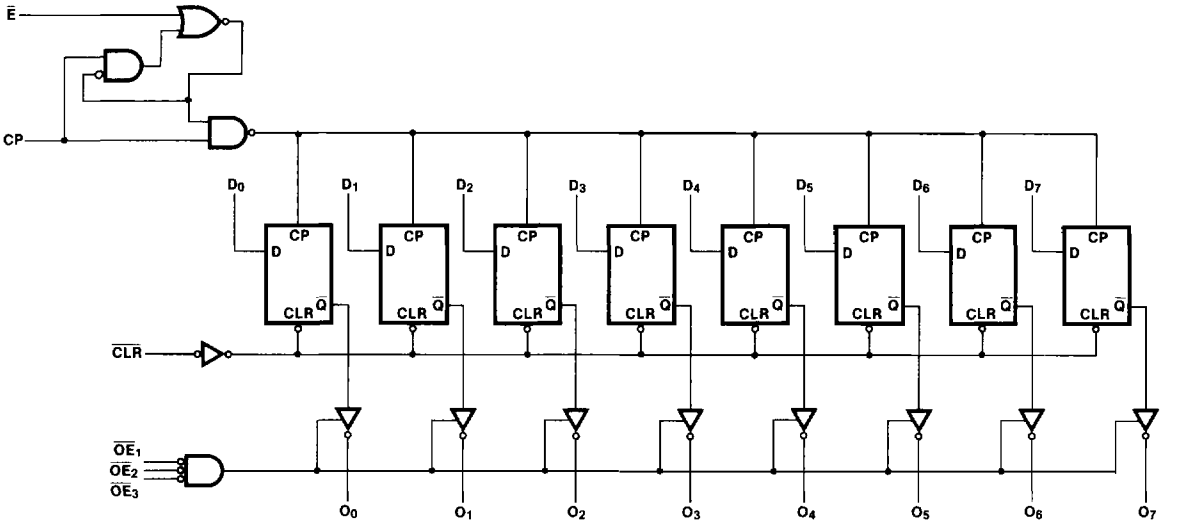
When the $\overline{CLR}$ is LOW and the $\overline{OE}$ is LOW the outputs are LOW. When $\overline{CLR}$ is HIGH, data can be entered into the flip-flops. When $\overline{EN}$ is LOW, data on the inputs is transferred to the outputs on the LOW-to-HIGH clock transition. When the $\overline{EN}$ is HIGH the outputs do not change state, regardless of the data or clock input transitions.

Function Table

Inputs					Internal	Output	Function
$\overline{OE}$	$\overline{CLR}$	EN	CP	D	Q	O	
H	X	L	↑	L	L	Z	High Z
H	X	L	↑	H	H	Z	High Z
H	L	X	X	X	L	Z	Clear
L	L	X	X	X	L	L	Clear
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	Hold
H	H	L	↑	L	L	Z	Load
H	H	L	↑	H	H	Z	Load
L	H	L	↑	L	L	L	Load
L	H	L	↑	H	H	H	Load

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
↑ = LOW-to-HIGH Transition
NC = No Change

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current			86	mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V, C_L = 50 pF			T_A, V_{CC} = Mil, C_L = 50 pF		T_A, V_{CC} = Com, C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	100							MHz	3-1,
t_{PLH} t_{PHL}	Propagation Delay CP to O_n		7.5 9.5						ns	3-1 3-7
t_{PHL}	Propagation Delay $\overline{CLR}$ to O_n		15.0						ns	3-1 3-9
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to O_n		11.5 7.5						ns	3-1 3-12 3-13
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to O_n		7.0 5.5							

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F	54F	74F	Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$	T_A, V_{CC} = Mil	T_A, V_{CC} = Com		
		Min Typ Max	Min Max	Min Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW D to CP	2.0 2.0			ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW D to CP	2.0 2.0				
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW $\overline{EN}$ to CP	3.0 3.0			ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW $\overline{EN}$ to CP	0 0				
$t_w(H)$ $t_w(L)$	CP Pulse Width HIGH or LOW	5.0 5.0			ns	3-7
$t_w(L)$	$\overline{CLR}$ Pulse Width, LOW	5.0			ns	3-9
t_{rec}	$\overline{CLR}$ Recovery Time	5.0			ns	3-11