

## 54AC/74AC109 • 54ACT/74ACT109

### Dual $\overline{JK}$ Positive Edge-Triggered Flip-Flop

#### Description

The 'AC/'ACT109 consists of two high-speed completely independent transition clocked  $\overline{JK}$  flip-flops. The clocking operation is independent of rise and fall times of the clock waveform. The  $\overline{JK}$  design allows operation as a D flip-flop (refer to 'AC/'ACT74 data sheet) by connecting the J and  $\overline{K}$  inputs together.

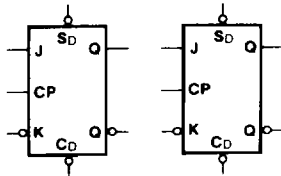
#### Asynchronous Inputs:

- LOW input to  $\overline{S}_D$  (Set) sets Q to HIGH level
- LOW input to  $\overline{C}_D$  (Clear) sets Q to LOW level
- Clear and Set are independent of clock
- Simultaneous LOW on  $\overline{C}_D$  and  $\overline{S}_D$  makes both Q and  $\overline{Q}$  HIGH

- Outputs Source/Sink 24 mA
- 'ACT109 has TTL-Compatible Inputs

**Ordering Code:** See Section 6

#### Logic Symbol

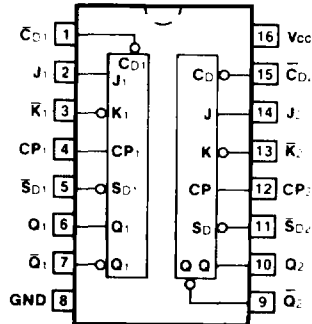


#### Truth Table

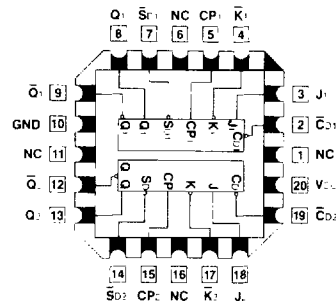
Inputs					Outputs	
$\overline{S}_D$	$\overline{C}_D$	CP	J	$\overline{K}$	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H	H
H	H	$\downarrow$	L	L	L	H
H	H	$\downarrow$	H	L	Toggle	
H	H	$\downarrow$	L	H	Q <sub>0</sub>	$\overline{Q}_0$
H	H	$\downarrow$	H	H	H	L
H	H	L	X	X	Q <sub>0</sub>	$\overline{Q}_0$

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 $\downarrow$  = LOW-to-HIGH Transition  
 X = Immaterial  
 Q<sub>0</sub>( $\overline{Q}_0$ ) = Previous Q<sub>0</sub>( $\overline{Q}_0$ ) before  
 LOW-to-HIGH Transition of Clock

#### Connection Diagrams



**Pin Assignment  
for DIP, Flatpak and SOIC**



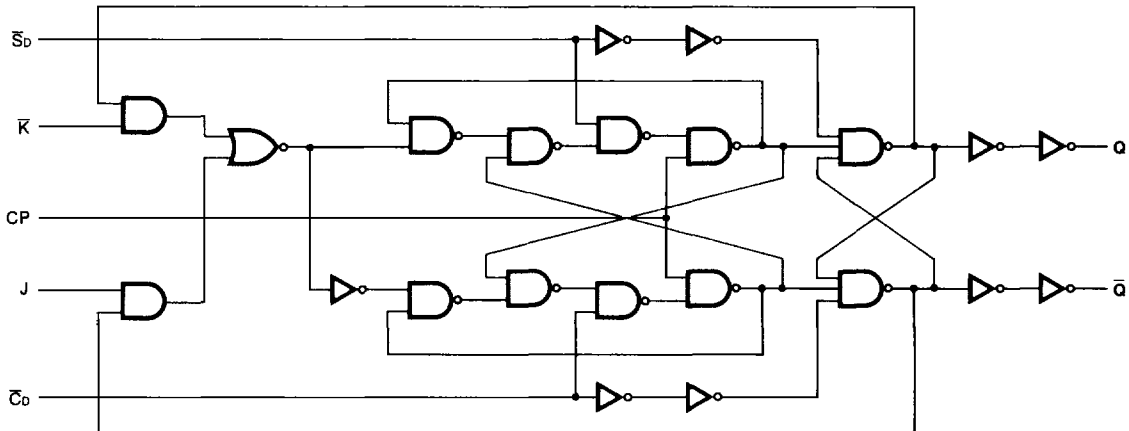
**Pin Assignment  
for LCC**

#### Pin Names

- J<sub>1</sub>, J<sub>2</sub>,  $\overline{K}_1$ ,  $\overline{K}_2$  Data Inputs
- CP<sub>1</sub>, CP<sub>2</sub> Clock Pulse Inputs
- $\overline{C}_D1$ ,  $\overline{C}_D2$  Direct Clear Inputs
- $\overline{S}_D1$ ,  $\overline{S}_D2$  Direct Set Inputs
- Q<sub>1</sub>, Q<sub>2</sub>,  $\overline{Q}_1$ ,  $\overline{Q}_2$  Outputs

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**Logic Diagram** (one half shown)



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC/ACT	74AC/ACT	Units	Conditions
$I_{CC}$	Maximum Quiescent Supply Current	80	40	$\mu A$	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5 V$ , $T_A = \text{Worst Case}$
$I_{CC}$	Maximum Quiescent Supply Current	4.0	4.0	$\mu A$	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5 V$ , $T_A = 25^\circ C$
$I_{CCT}$	Maximum Additional $I_{CC}/\text{Input}$ ('ACT109)	1.6	1.5	mA	$V_{IN} = V_{CC} - 2.1 V$ $V_{CC} = 5.5 V$ , $T_A = \text{Worst Case}$

**AC Characteristics**

Symbol	Parameter	Vcc* (V)	74AC			54AC		74AC		Units	Fig. No.
			TA = +25°C CL = 50 pF			TA = -55°C to +125°C CL = 50 pF		TA = -40°C to +85°C CL = 50 pF			
			Min	Typ	Max	Min	Max	Min	Max		
f <sub>max</sub>	Maximum Clock Frequency	3.3 5.0	125 150	150 175		90 95		100 125	MHz	3-3	
t <sub>PLH</sub>	Propagation Delay CP <sub>n</sub> to Q <sub>n</sub> or Q̄ <sub>n</sub>	3.3 5.0	1.0 1.0	8.0 6.0	13.5 10.0	1.0 1.0	17.5 11.0	1.0 1.0	16.0 10.5	ns	3-6
t <sub>PHL</sub>	Propagation Delay CP <sub>n</sub> to Q <sub>n</sub> or Q̄ <sub>n</sub>	3.3 5.0	1.0 1.0	8.0 6.0	14.0 10.0	1.0 1.0	16.0 11.5	1.0 1.0	14.5 10.5	ns	3-6
t <sub>PLH</sub>	Propagation Delay C̄D <sub>n</sub> or S̄D <sub>n</sub> to Q <sub>n</sub> or Q̄ <sub>n</sub>	3.3 5.0	1.0 1.0	8.0 6.0	12.0 9.0	1.0 1.0	14.5 10.5	1.0 1.0	13.0 10.0	ns	3-6
t <sub>PHL</sub>	Propagation Delay C̄D <sub>n</sub> or S̄D <sub>n</sub> to Q <sub>n</sub> or Q̄ <sub>n</sub>	3.3 5.0	1.0 1.0	10.0 7.5	12.0 9.5	1.0 1.0	20.0 14.5	1.0 1.0	13.5 10.5	ns	3-6

\*Voltage Range 3.3 is 3.3 V ± 0.3 V  
Voltage Range 5.0 is 5.0 V ± 0.5 V

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**AC Operating Requirements**

Symbol	Parameter	Vcc* (V)	74AC		54AC		74AC		Units	Fig. No.
			TA = +25°C CL = 50 pF		TA = -55°C to +125°C CL = 50 pF		TA = -40°C to +85°C CL = 50 pF			
			Typ	Guaranteed Minimum						
t <sub>s</sub>	Set-up Time, HIGH or LOW J <sub>n</sub> or K̄ <sub>n</sub> to CP <sub>n</sub>	3.3 5.0	3.5 2.0	6.5 4.5	8.0 5.5	7.5 5.0			ns	3-9
t <sub>h</sub>	Hold Time, HIGH or LOW J <sub>n</sub> or K̄ <sub>n</sub> to CP <sub>n</sub>	3.3 5.0	-1.5 -0.5	0 0.5	1.0 1.0	0 0.5			ns	3-9
t <sub>w</sub>	Pulse Width CP <sub>n</sub> or C̄D <sub>n</sub> or S̄D <sub>n</sub>	3.3 5.0	2.0 2.0	4.0 3.5	8.0 5.5	4.5 3.5			ns	3-6
t <sub>rec</sub>	Recovery Time C̄D <sub>n</sub> or S̄D <sub>n</sub> to CP	3.3 5.0	-2.5 -1.5	0 0	0 0	0 0			ns	3-9

\*Voltage Range 3.3 is 3.3 V ± 0.3 V  
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

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## AC Characteristics

Symbol	Parameter	Vcc* (V)	74ACT			54ACT		74ACT		Units	Fig. No.
			TA = +25°C CL = 50 pF			TA = -55°C to +125°C CL = 50 pF		TA = -40°C to +85°C CL = 50 pF			
			Min	Typ	Max	Min	Max	Min	Max		
fmax	Maximum Clock Frequency	5.0	145	210		95		125	MHz	3-3	
tPLH	Propagation Delay CPn to Qn or Q̄n	5.0	1.0	7.0	11.0	1.0	14.0	1.0	13.0	ns	3-6
tPHL	Propagation Delay CPn to Qn or Q̄n	5.0	1.0	6.0	10.0	1.0	12.0	1.0	11.5	ns	3-6
tPLH	Propagation Delay C̄Dn or S̄Dn to Qn or Q̄n	5.0	1.0	5.5	9.5	1.0	11.5	1.0	10.5	ns	3-6
tPHL	Propagation Delay C̄Dn or S̄Dn to Qn or Q̄n	5.0	1.0	6.0	10.0	1.0	12.5	1.0	11.5	ns	3-6

\*Voltage Range 5.0 is 5.0 V ± 0.5 V

## AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74ACT		54ACT		74ACT		Units	Fig. No.
			TA = +25°C CL = 50 pF		TA = -55°C to +125°C CL = 50 pF		TA = -40°C to +85°C CL = 50 pF			
			Typ	Guaranteed Minimum						
ts	Set-up Time, HIGH or LOW Jn or K̄n to CPn	5.0	0.5	2.0		2.5		2.5	ns	3-9
th	Hold Time, HIGH or LOW Jn or K̄n to CPn	5.0	0	2.0		2.0		2.0	ns	3-9
tw	Pulse Width CPn or C̄Dn or S̄Dn	5.0	3.0	5.0		6.5		6.0	ns	3-6
trec	Recovery Time C̄Dn or S̄Dn to CP	5.0	-2.5	0		0		0	ns	3-9

\*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

**Capacitance**

<b>Symbol</b>	<b>Parameter</b>	<b>54/74AC/ACT</b>	<b>Units</b>	<b>Conditions</b>
		<b>Typ</b>		
C <sub>IN</sub>	Input Capacitance	4.5	pF	V <sub>CC</sub> = 5.5 V
C <sub>PD</sub>	Power Dissipation Capacitance	35.0	pF	V <sub>CC</sub> = 5.5 V