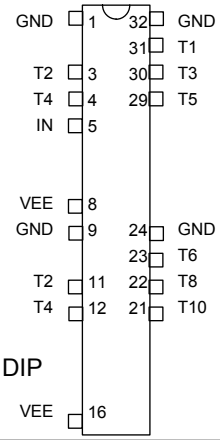
5-TAP, ECL-INTERFACED FIXED DELAY LINE (SERIES DDU12H)

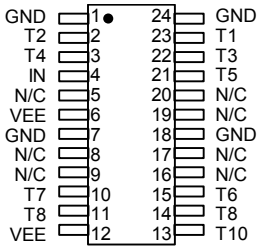
FEATURES

- Ten equally spaced outputs
- Fits in 300 mil 32-pin DIP socket
- Input & outputs fully 10KH-ECL interfaced & buffered

PACKAGES



DDU12H-xx DIP
DDU12H-xxM Military DIP



DDU12H-xxC4 SMD
DDU12H-xxMC4 Mil SMD

FUNCTIONAL DESCRIPTION

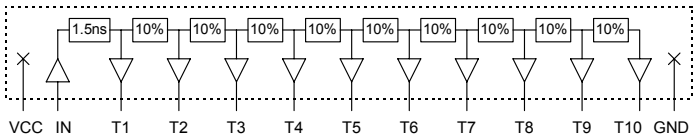
The DDU12H-series device is a 10-tap digitally buffered delay line. The signal input (IN) is reproduced at the outputs (T1-T10), shifted in time by an amount determined by the device dash number (See Table). For dash numbers less than 20, the total delay of the line is measured from T1 to T10. The nominal tap-to-tap delay increment is given by one-ninth of the total delay, and the inherent delay from IN to T1 is nominally 1.5ns. For dash numbers greater than or equal to 20, the total delay of the line is measured from IN to T10. The nominal tap-to-tap delay increment is given by one-tenth of this number.

PIN DESCRIPTIONS

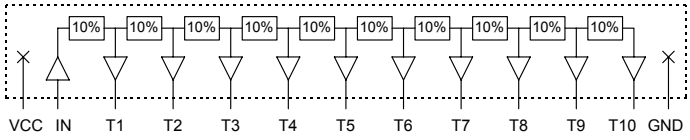
IN	Signal Input
T1-T10	Tap Outputs
VEE	-5 Volts
GND	Ground

SERIES SPECIFICATIONS

- **Minimum input pulse width:** 10% of total delay
- **Output rise time:** 2ns typical
- **Supply voltage:** -5VDC ± 5%
- **Power dissipation:** 400mw typical (no load)
- **Operating temperature:** -30° to 85° C
- **Temp. coefficient of total delay:** 100 PPM/°C



Functional diagram for dash numbers < 20



Functional diagram for dash numbers >= 20

DASH NUMBER SPECIFICATIONS

Part Number	Total Delay (ns)	Delay Per Tap (ns)
DDU12H-10	9 ± 1.0 *	1.0 ± 0.3
DDU12H-20	20 ± 2.0	2.0 ± 0.4
DDU12H-25	25 ± 2.0	2.5 ± 0.4
DDU12H-40	40 ± 2.0	4.0 ± 0.5
DDU12H-50	50 ± 2.5	5.0 ± 1.0
DDU12H-75	75 ± 4.0	7.5 ± 1.5
DDU12H-100	100 ± 5.0	10.0 ± 2.0
DDU12H-150	150 ± 7.5	15.0 ± 2.0
DDU12H-200	200 ± 10.0	20.0 ± 2.0
DDU12H-250	250 ± 12.5	25.0 ± 2.0
DDU12H-300	300 ± 15.0	30.0 ± 2.0
DDU12H-400	400 ± 20.0	40.0 ± 2.0
DDU12H-500	500 ± 25.0	50.0 ± 2.5
DDU12H-750	750 ± 37.5	75.0 ± 4.0
DDU12H-1000	1000 ± 50.0	100.0 ± 5.0
DDU12H-1500	1500 ± 75.0	150.0 ± 7.0

*** Total delay is referenced to first tap output**
Input to first tap = 1.5ns ± 1ns

NOTE: Any dash number between 10 and 1500 not shown is also available.

APPLICATION NOTES

HIGH FREQUENCY RESPONSE

The DDU12H tolerances are guaranteed for input pulse widths and periods greater than those specified in the test conditions. Although the device will function properly for pulse widths as small as 10% of the total delay and periods as small as 20% of the total delay (for a symmetric input), the delays may deviate from their values at low frequency. However, for a given input condition, the deviation will be repeatable from pulse to pulse. Contact technical support at Data Delay Devices if your application requires device testing at a specific input condition.

POWER SUPPLY BYPASSING

The DDU12H relies on a stable power supply to produce repeatable delays within the stated tolerances. A 0.1uf capacitor from VEE to GND, located as close as possible to the VEE pin, is recommended. A wide VEE trace and a clean ground plane should be used.

DEVICE SPECIFICATIONS

TABLE 1: ABSOLUTE MAXIMUM RATINGS

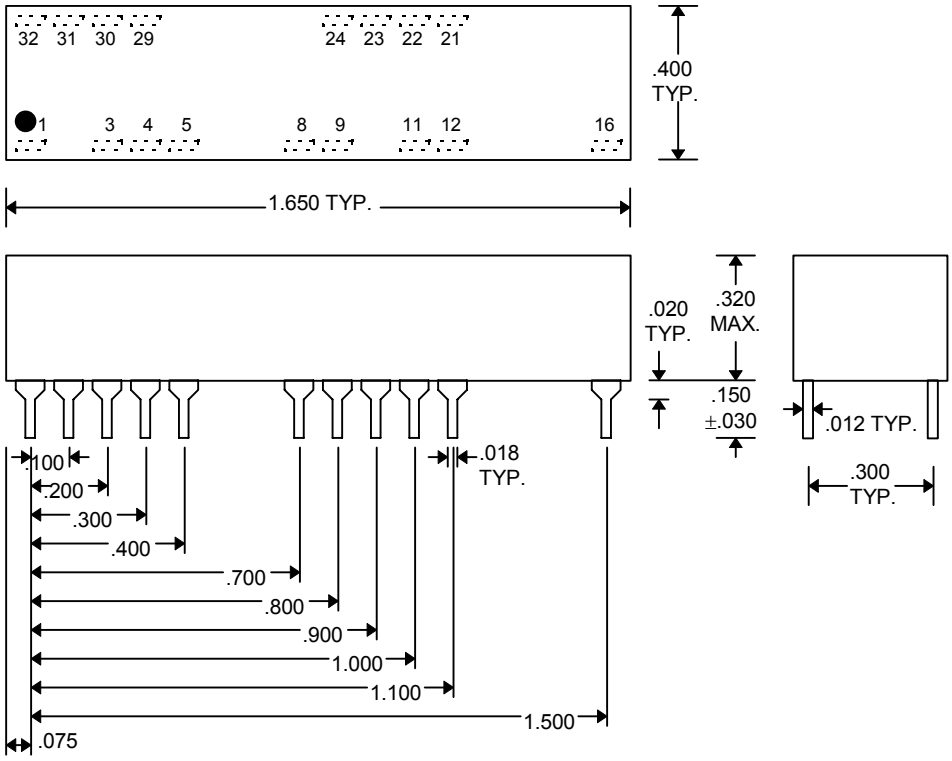
PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
DC Supply Voltage	V_{EE}	-7.0	0.3	V	
Input Pin Voltage	V_{IN}	V_{EE} - 0.3	0.3	V	
Storage Temperature	T_{STRG}	-55	150	C	
Lead Temperature	T_{LEAD}		300	C	10 sec

TABLE 2: DC ELECTRICAL CHARACTERISTICS

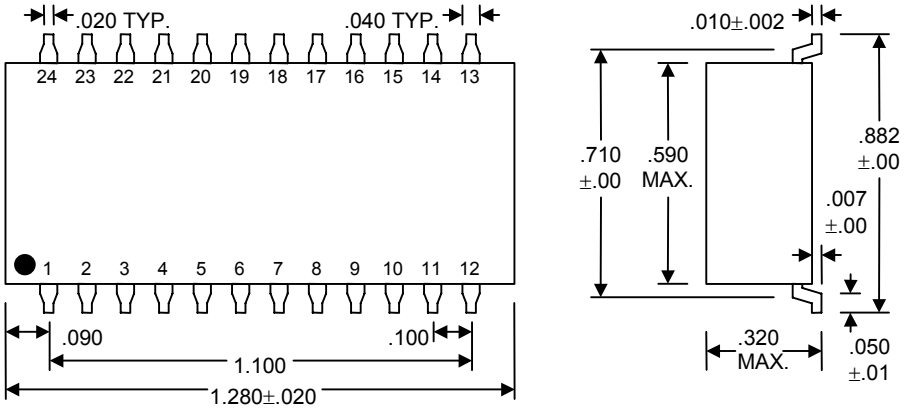
(0C to 75C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
High Level Output Voltage	V_{OH}	-1.020		-0.735	V	V_{IH} = MAX,50Ω to -2V
Low Level Output Voltage	V_{OL}	-1.950		-1.600	V	V_{IL} = MIN, 50Ω to -2V
High Level Input Voltage	V_{IH}			-1.070	V	
Low Level Input Voltage	V_{IL}	-1.480			V	
High Level Input Current	I_{IH}			475	μA	V_{IH} = MAX
Low Level Input Current	I_{IL}	0.5			μA	V_{IL} = MIN

PACKAGE DIMENSIONS



DDU12H-xx (Commercial DIP)
DDU12H-xxM (Military DIP)



DDU12H-xxC4 (Commercial SMD)
DDU12H-xxMC4 (Military SMD)

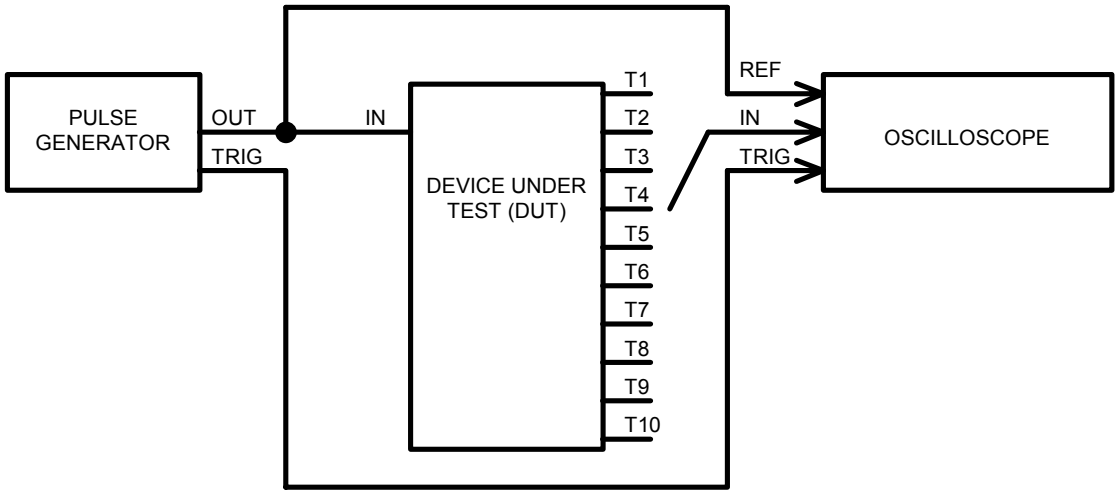
DELAY LINE AUTOMATED TESTING

TEST CONDITIONS

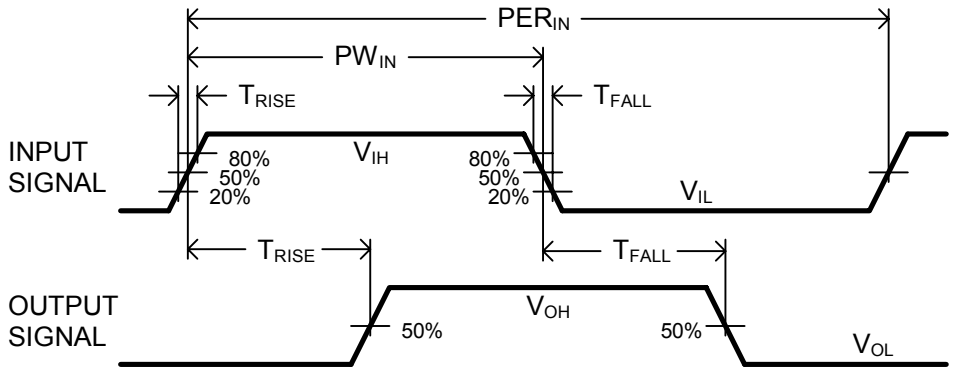
INPUT:
Ambient Temperature: 25°C ± 3°C
Supply Voltage (Vcc): -5.0V ± 0.1V
Input Pulse: Standard 10KH ECL levels
Source Impedance: 50Ω Max.
Rise/Fall Time: 2.0 ns Max. (measured between 20% and 80%)
Pulse Width: PW_{IN} = 1.5 x Total Delay
Period: PER_{IN} = 10 x Total Delay

OUTPUT:
Load: 50Ω to -2V
C_{load}: 5pf ± 10%
Threshold: (V_{OH} + V_{OL}) / 2 (Rising & Falling)

NOTE: The above conditions are for test only and do not in any way restrict the operation of the device.



Test Setup



Timing Diagram For Testing