Signetics

FAST Products

FAST 74F838

Microprogram Sequence Controller

Preliminary Specification

FEATURES

- **5-bit address generator (32 micro-instruction addressability)**
- **Two subroutine branching capability**
- **Interrupt branching**
- **Cascadable for increased addressing**
- **Direct branching over full address range**

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F838	90MHz	mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F838N
20-Pin SOL	N74F838D

DESCRIPTION

The 74F838 Microprogram Sequence Controller generates addresses to access instructions from a microprogram memory.

This high speed device provides an efficient means of controlling the flow through a microprgram by providing a powerful set of sequencing functions.

In addition to providing branching facility over the entire address range, the device also supports two subroutines and an interrupt level.

The 74F838 can directly address up to 32 micro-instructions: two or more of these devices may be cascaded for increased addressing. For example, two devices can address 1K and three devices can address up to 32K of program storage.

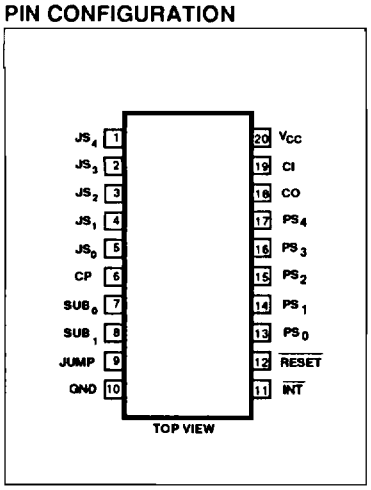
Combined with memory, the 74F838 form a powerful control section for CPUs and I/O controllers.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

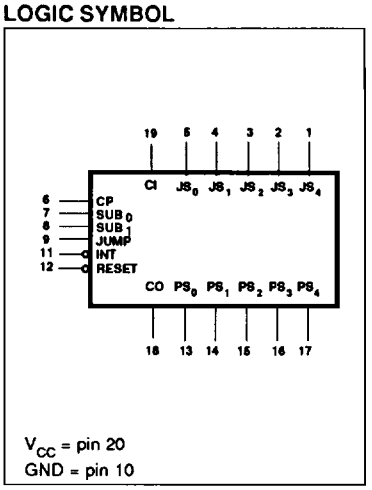
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
JS_0 - JS_4	Jump state inputs	1.0/1.0	20µA/0.6mA
JMP	Jump input	1.0/1.0	20µA/0.6mA
SUB_0, SUB_1	Subroutine inputs	1.0/1.0	20µA/0.6mA
$\overline{INT}$	Interrupt input	1.0/1.0	20µA/0.6mA
CP	Clock input	1.0/1.0	20µA/0.6mA
CI	Cascade In input	1.0/1.0	20µA/0.6mA
$\overline{RESET}$	Reset input	1.0/1.0	20µA/0.6mA
PS_0 - PS_4	Present state outputs	150/40	3.0mA/24mA
CO	Cascade Out output	150/40	3.0mA/24mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

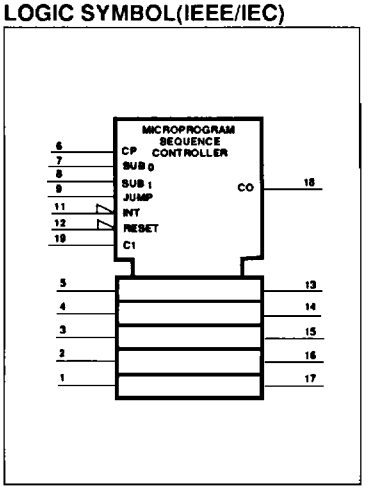
PIN CONFIGURATION



LOGIC SYMBOL



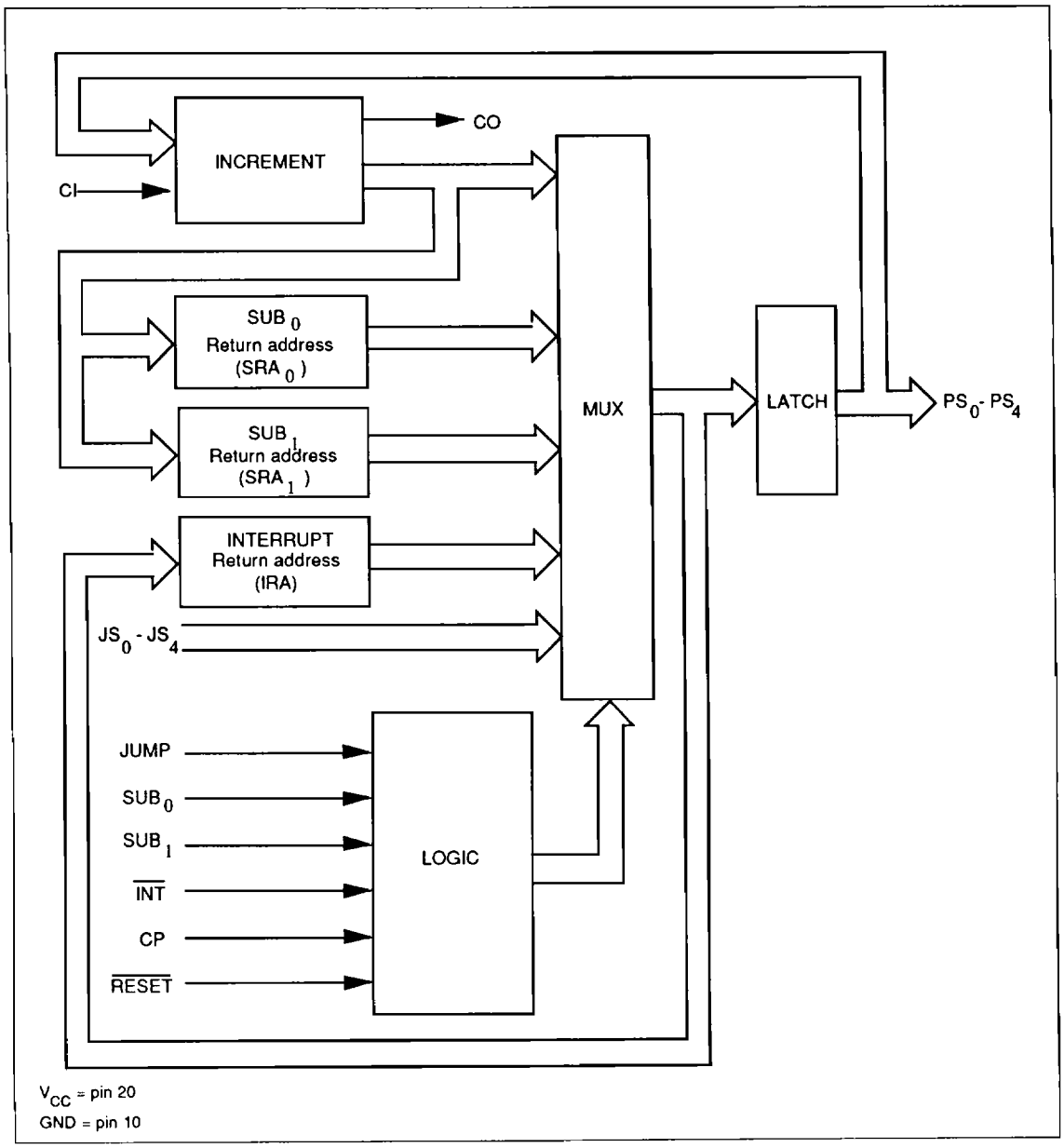
LOGIC SYMBOL(IEEE/IEC)



PIN DESCRIPTION

PIN NO.	SYMBOL	TYPE	FUNCTION	DESCRIPTION
5 4 3 2 1	JS_0 JS_1 JS_2 JS_3 JS_4	Input	Jump State	Address on these inputs is transferred to the PS_0-PS_4 outputs if the JMP input is High or the SUB_0 or SUB_1 inputs change from Low-to-High. These inputs are ignored if neither of the above conditions is true.
7 8	SUB_0 SUB_1	Input	Subroutine	On a Low-to-High transition, the Present State address (PS_0-PS_4) plus one is saved internally as a return address, and address on pins JS_0-JS_4 will be transferred to the PS_0-PS_4 outputs. On a High-to-Low transition, the saved return address state will be enabled onto the PS_0-PS_4 outputs.
9	JMP	Input	Jump	When JMP is High, the next state address will be JS_0-JS_4.
11	$\overline{INT}$	Input	Interrupt	On a High-to-Low transition, the next address to appear on the PS_0-PS_4 output is saved internally as a return address and PS_0-PS_4 are forced to all ones. If this feature is used, a micromode jump would normally be stored at state address 11111. SUB_0 or SUB_1 inputs are ignored when $\overline{INT}$ is Low. On a Low-to-High transition, the saved return address state is enabled onto the PS_0-PS_4 outputs.
6	CP	Input	Clock	This clock determines the sequence rate of the controller.
12	$\overline{RESET}$	Input	Reset	When Low, all internal registers and PS_0-PS_4 are set to zeros.
19	CI	Input	Cascade In	This input should be tied to V_{CC} for the least significant device. For all other devices, CI is connected to CO of the previous device.
18	CO	Output	Cascade Out	This signal is connected to CI of the next device. One device permits 32 states: two devices allow 1024 states; three devices allow 32,768 states.
13 14 15 16 17	PS_0 PS_1 PS_2 PS_3 PS_4	Output	Present state	The address of the present state.

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS							OUTPUTS				OPERATING MODE
								INTERNAL REGISTERS			
$\overline{RESET}$	$\overline{INT}$	JUMP	SUB_0	SUB_1	CP	JS_n	PS_0-PS_4	SRA_0	SRA_1	IRA	
L	X	X	X	X	X	X	00000	0	0	0	Reset
H	H	L	H or L	H or L	↑	X	PS_{n+1}				Increment
H	L	L	X	X	↑	X	PS_{n+1}				
H	L	H	X	X	↑	JS_n	JS_n				Jump
H	H	H	↓	↓	↑	JS_n	JS_n				
H	H	X	↑	H or L	↑	JS_n	JS_n	PS_{n+1}			Subroutine Call
H	H	X	H or L	↑	↑	JS_n	JS_n		PS_{n+1}		
H	H	X	↑	↑	↑	JS_n	JS_n	PS_{n+1}	PS_{n+1}		
H	H	L	↓	H or L	↑	X	SRA_0				Return from Subroutine
H	H	L	H or L	↓	↑	X	SRA_1				
H	↓	L	H or L	H or L	↑	X	11111			PS_{n+1}	Interrupt Call
H	↓	H	H or L	H or L	↑	JS_n	11111			JS_n	
H	↓	X	↑	H or L	↑	JS_n	11111	PS_{n+1}		JS_n	
H	↓	X	H or L	↑	↑	JS_n	11111		PS_{n+1}	JS_n	
H	↓	X	↑	↑	↑	JS_n	11111	PS_{n+1}	PS_{n+1}	JS_n	
H	↓	L	↓	H or L	↑	X	11111			SRA_0	
H	↓	L	H or L	↓	↑	X	11111			SRA_1	Return from Interrupt
H	↑	X	X	X	↑	X	IRA				Illegal
H	H	H	↓	H or L	↑	JS_n	$JS_n + SRA_0$				
H	H	H	H or L	↓	↑	JS_n	$JS_n + SRA_1$				
H	H	L	↓	↓	↑	X	$SRA_0 + SRA_1$				
H	H	H	↓	↓	↑	JS_n	$JS_n + SRA_0 + SRA_1$				
H	↓	H	↓	H or L	↑	JS_n	11111			$JS_n + SRA_0$	
H	↓	H	H or L	↓	↑	JS_n	11111			$JS_n + SRA_1$	
H	↓	L	↓	↓	↑	X	11111			$SRA_0 + SRA_1$	
H	↓	H	↓	↓	↑	JS_n	11111			$JS_n + SRA_0 + SRA_1$	

H = High voltage level.
L = Low voltage level.
X = Don't care.

↓ = High-to-Low clock transition.

↓ = Antything except a High-to-Low clock transition.

↑ = Low-to-High clock transition.

H or L = Either High or Low

0 = Low output

1 = High output

To avoid timing problems $\overline{INT}$ is sampled on the falling edge of the clock and serviced on the next rising edge.

APPLICATION

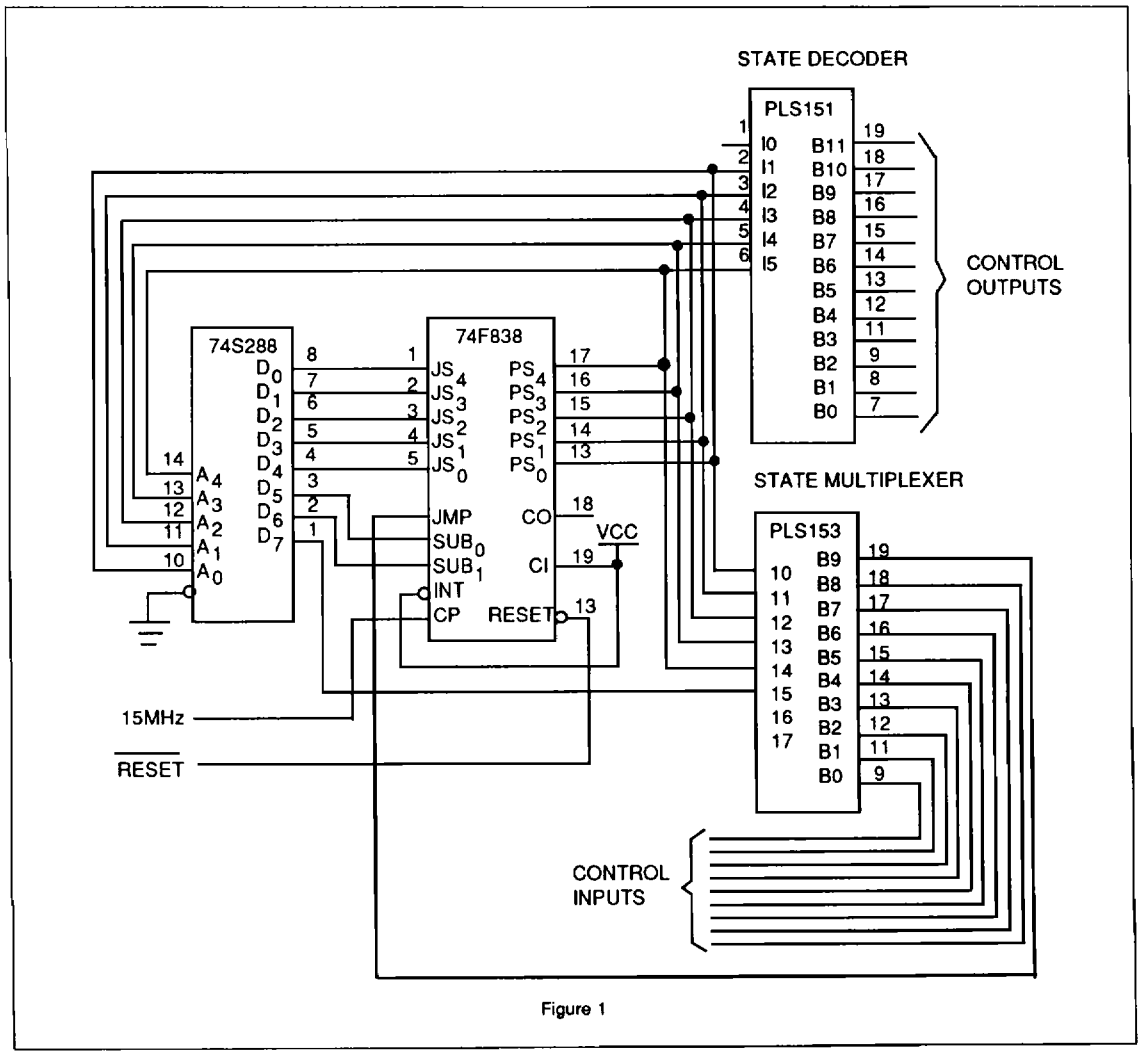


Figure 1

As shown in Figure 1, a PROM paired with a 74F838 creates a state machine. When reset, the PS_0-PS_4 outputs are zero. The present state is decoded to generate control inputs. In this application, a PLS151 acts as the state decoder. When a state has a branch option based on the state of a control signal, the Present is used as the address input to a multiplexer. The output of the multiplexer connects to the JUMP input of the 74F838. When the proper state is decoded, the associated control input is passed on to the JUMP input. In this application, to allow a forced jump, D_0 is also a control input. All state changes occur on the rising edge of the Clock input. However, since the interrupt input ($\overline{INT}$) is normally asynchronous in many applications, to avoid timing problems, $\overline{INT}$ is sampled on the falling edge of the Clock.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-3	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.35	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximun input voltage		V_{CC} =MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} =MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} =MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short circuit output current[3]		V_{CC} =MAX, V_O= 2.25V		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} =MAX				90	mA
		I_{CCL}					90	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

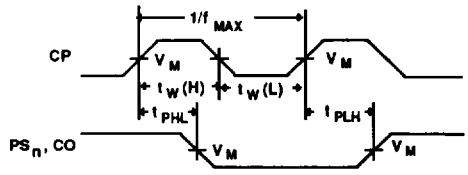
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	70	90				MHz
t_{PLH} t_{PHL}	Propagation delay CP to PS_n or CO	Waveform 1						ns
t_{PHL}	Propagation delay $\overline{RESET}$ to PS_n or CO.	Waveform 2						ns

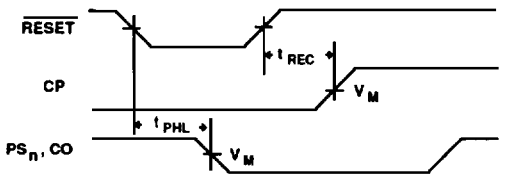
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low JS_n to CP	Waveform 3						ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low JS_n to CP	Waveform 3						ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low JMP to CP	Waveform 3						ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low JMP to CP	Waveform 3						ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{INT}$ to CP	Waveform 3						ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{INT}$ to CP	Waveform 3						ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low SUB_n to CP	Waveform 3						ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low SUB_n to CP	Waveform 3						ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low CI to CP	Waveform 3						ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low CI to CP	Waveform 3						ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low	Waveform 1						ns
$t_w(L)$	$\overline{RESET}$ Pulse width, Low	Waveform 2						ns
t_{REC}	Recovery Time, $\overline{RESET}$ to CP	Waveform 2						ns

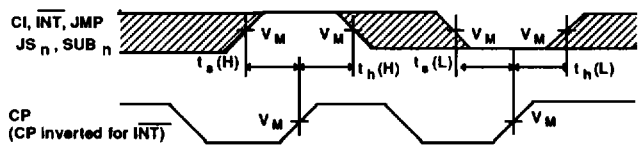
AC WAVEFORMS



Waveform 1. Propagation Delay, Clock To Output, Clock Pulse Width, Maximum Clock Frequency



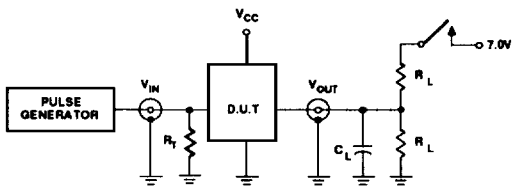
Waveform 2. Propagation Delay, Reset To Output, Reset To Clock Pulse Recovery Time



Waveform 3. Setup And Hold Times

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

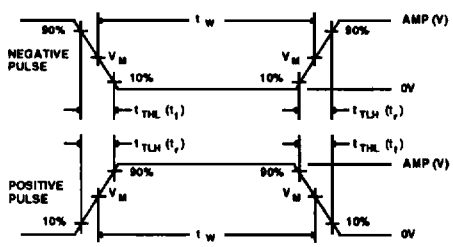
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns