

Actual Size = 5 x 7mm



Product Features

- 5V CMOS/TTL compatible logic levels
- Pin-compatible with standard 5x7mm packages
- Designed for standard reflow and washing techniques
- Output Tri-state function
- Pb-free and RoHS/Green compliant

Product Description

The S1615 Series is a 5V crystal clock oscillator that achieves superb jitter and stability over a broad range of operating conditions and frequencies. The output clock signal, generated internally with a non-PLL oscillator design, is compatible with CMOS/TTL logic levels. The device, available on tape and reel, is contained in a 5x7mm surface-mount ceramic package.

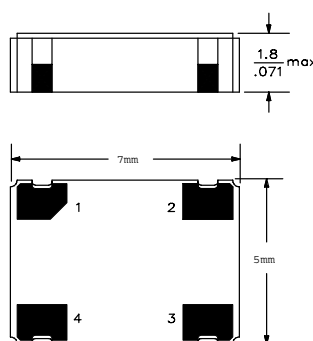
Applications

The S1615 Series is an ideal reference clock for applications requiring low jitter or tight stability, including:

- Ethernet
- FibreChannel
- Serial Attached SCSI (SAS)
- Server & Storage platforms
- SONET/SDH linecards
- T1/E1, T3/E3 linecards
- DSLAM
- 802.11a/b/g WiFi



Packaging Outline



Pin Functions

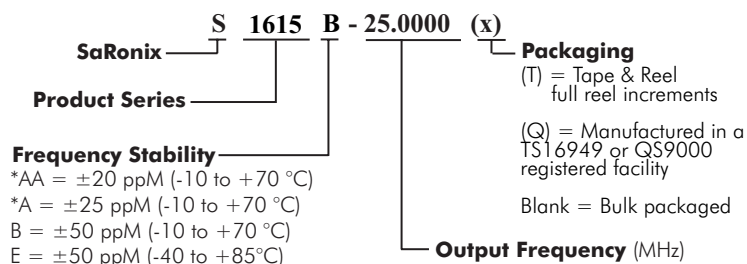
Pin	Function
1	OE Function
2	Ground
3	Clock Output
4	V _{DD}

Common Frequencies

Contact SaRonix for additional frequencies

1.5440 Mhz	22.0000 MHz	44.7360 MHz
2.0480 MHz	24.5760 MHz	48.0000 MHz
3.6864 MHz	25.0000 MHz	50.0000 MHz
8.0000 MHz	32.0000 MHz	60.0000 MHz
10.0000 MHz	32.7680 MHz	66.0000 MHz
14.3181 MHz	33.0000 MHz	66.6667 MHz
16.0000 MHz	34.3680 MHz	74.2500 MHz
16.3840 MHz	35.3280 MHz	75.0000 MHz
18.4320 MHz	38.8800 MHz	77.7600 MHz
19.4400 MHz	40.0000 MHz	80.0000 MHz
20.0000 MHz	44.0000 MHz	90.0000 MHz

Ordering Information



* Availability varies by frequency.

Electrical Performance

Parameter		Min.	Typ.	Max.	Units	Notes
Output frequency		1.544		106.25	MHz	As specified
Supply voltage		+4.5	+5.0	+5.5	V	
Supply current, output enabled				27	mA	1.544 to 32 MHz
				50		>32 to 50 MHz
				65		>50 to 106.25 MHz
Frequency stability				±20 to ±50	ppM	See Note 1 below
Operating temperature		-40		+85	°C	As specified
Output logic 0, VOL				10% V _{DD}	V	HCMOS
				+0.4	V	TTL
Output logic 1, VOH		90% V _{DD}			V	HCMOS
		+3.9			V	TTL
Output load				50	pF	HCMOS up to <50 MHz
				30	pF	HCMOS 50 to <70 MHz
				15	pF	HCMOS 70 to 106.25 MHz
				10	TTL	TTL
Duty cycle	1.544 to 80 MHz	45		55	%	-40 to +85°C measured 50%VDD
	>80 to 106.25 MHz	45		55	%	-10 to +70°C measured 50%VDD
		40		60	%	-40 to +85°C measured 50%VDD
	1.544 to 106.25 MHz	40		60	%	-40 to +85°C measured 1.5V
Rise and fall time	1.544 up to <50 MHz			8	ns	measured 20/80% of waveform
	50 to <70 MHz			5	ns	
	70 to 106.25 MHz			3	ns	
	1.544 to <70 MHz			5	ns	measured 0.4V to 2.4V
	70 to 106.25 MHz			2	ns	

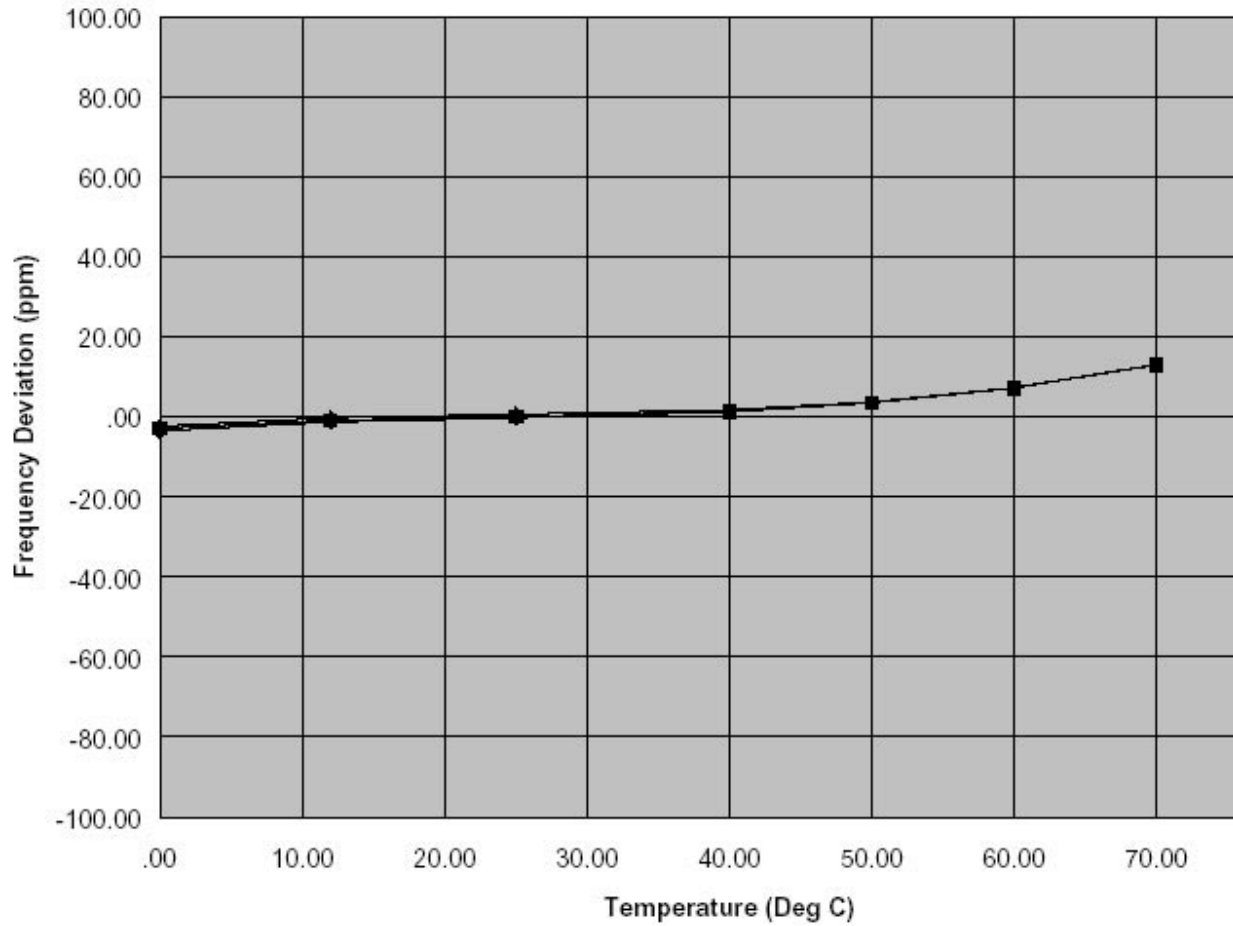
Notes:

- As specified. Stability includes all combinations of operating temperature, load changes, rated input (supply) voltage changes, initial calibration tolerance (25°C), aging (1 year at 25°C average effective ambient temperature), shock and vibration.

Output Enable / Disable Function

Parameter	Min.	Typ.	Max.	Units	Notes
Input Voltage (pin 1), Output Enable	2.2			V	or open
Input voltage (pin 1), Output Disable (low power standby)			0.8	V	Output is Hi-Z
Internal pullup resistance	50			kΩ	
Output disable delay			100	ns	
Output enable delay			100	ns	

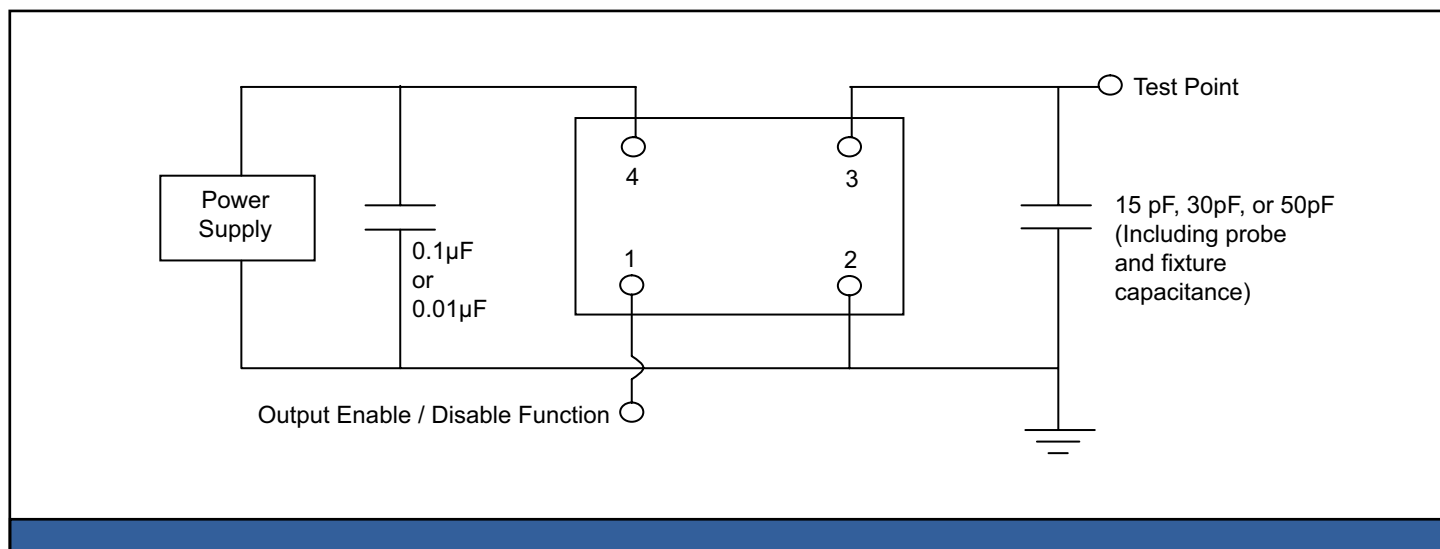
Typical Frequency Stability



Absolute Maximum Ratings

Parameter	Min.	Typ.	Max.	Units	Notes
Storage temperature	-55		+125	°C	

Test Circuit

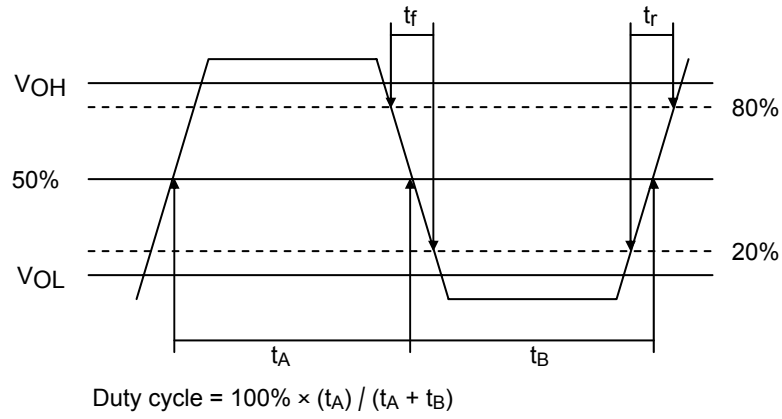


Reliability Test Ratings

This product is rated to meet the following test conditions:

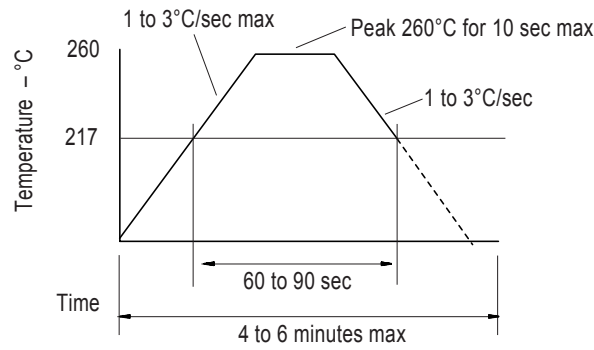
Type	Parameter	Test Condition
Mechanical	Shock	MIL-STD-883, Method 2002, Condition B
Mechanical	Solderability	JESD22-B102-D Method 2 (Preconditioning E)
Mechanical	Terminal strength	MIL-STD-883, Method 2004, Condition D
Mechanical	Gross leak	MIL-STD-883, Method 1014, Condition C
Mechanical	Fine leak	MIL-STD-883, Method 1014, Condition A2 ($R_1 = 2 \times 10^{-8}$ atm cc/s)
Mechanical	Solvent resistance	MIL-STD-202, Method 215
Environmental	Thermal shock	MIL-STD-883, Method 1011, Condition A
Environmental	Moisture resistance	MIL-STD-883, Method 1004
Environmental	Vibration	MIL-STD-883, Method 2007, Condition A
Environmental	Resistance to soldering heat	J-STD-020C Table 5-2 Pb-free devices (2 cycles max)

Output Waveform

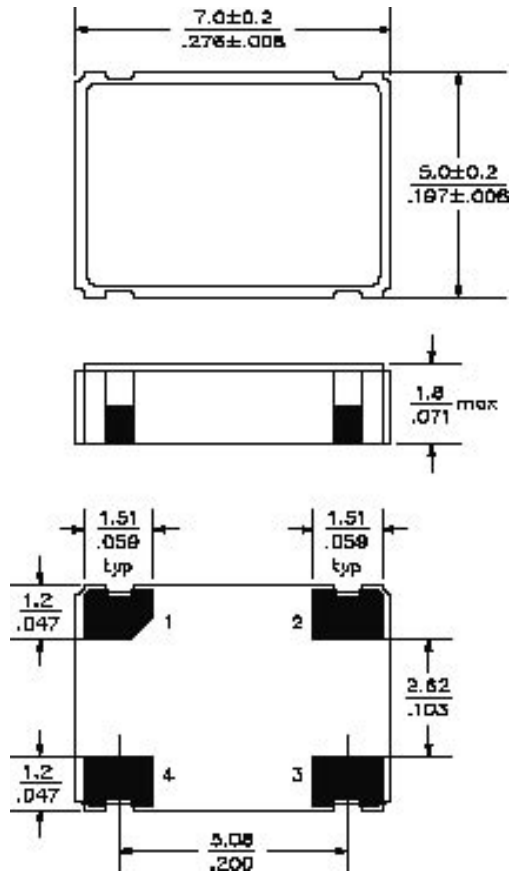


Reflow Soldering Profile

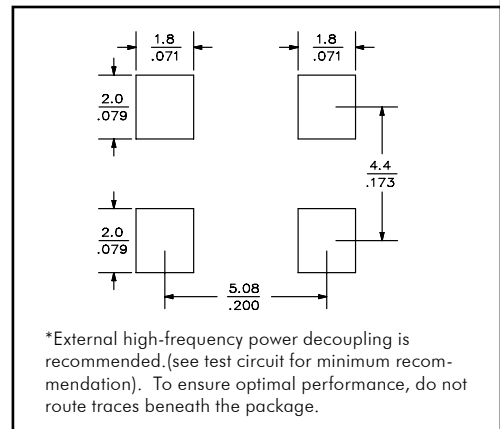
As per IPC/JEDEC J-STD-020C



Mechanical Drawings



Recommended Land Pattern*



Scale: None. Dimensions are in mm/inches.

Marking LINE 1: S K X (SaRonix, Model, Stability code)
 Marking LINE 2: Frequency (Frequency code)
 Marking LINE 3: ● YY WW X (Pin 1, Year, Week, Origin)

**Exact location of markings may vary.