N-Channel 40-V (D-S), 175 °C MOSFET

PRODUCT SUMMARY			
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)[a]	Q_g (Typ.)
40	0.020 at V_{GS} = 10 V	20	11.4 nC
	0.025 at V_{GS} = 4.5 V	20	

FEATURES

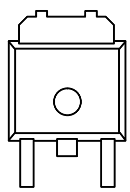
- TrenchFET® Power MOSFET
- 100 % R_g and UIS Tested

RoHS COMPLIANT

APPLICATIONS

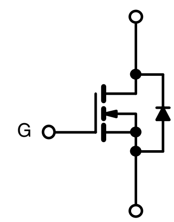
- LCD TV Inverter
- Secondary Synchronous Rectifier

TO-252



Top View

Ordering Information: SUD50N04-25P-E3 (Lead (Pb)-free)



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T_A = 25 °C, unless otherwise noted

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	40	V
Gate-Source Voltage		V_{GS}	± 16	
Continuous Drain Current (T_J = 150 °C)	T_C = 25 °C	I_D	20[a]	A
	T_C = 100 °C		18.9	
	T_A = 25 °C		8.5[b]	
	T_A = 100 °C		4.9[b]	
Pulsed Drain Current		I_{DM}	50	
Continuous Source-Drain Diode Current	T_C = 25 °C	I_S	20[a]	
	T_A = 25 °C		2.3[b]	
Single Pulse Avalanche Current	L = 0.1 mH	I_{AS}	20	
Avalanche Energy		E_{AS}	20	mJ
Maximum Power Dissipation	T_C = 25 °C	P_D	28.8	W
	T_C = 100 °C		14.4	
	T_A = 25 °C		2.8[b]	
	T_A = 100 °C		1.4[b]	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 175	°C

THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient[b]	Steady State	R_{thJA}	43	52	°C/W
Maximum Junction-to-Case	Steady State	R_{thJC}	4.3	5.2	

Notes:
a. Package limited.
b. Surface mounted on 1" x 1" FR4 board.

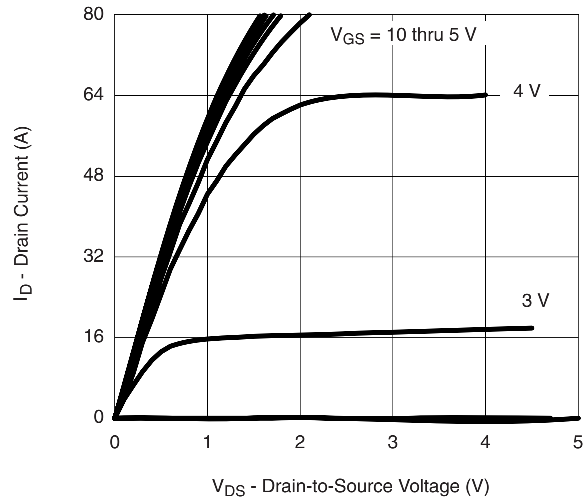
SPECIFICATIONS T_J = 25 °C, unless otherwise noted						
Parameter	**Symbol**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA	40			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	I_D = 250 µA		37		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			5.3		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 250 µA	1.0		2.6	V
Gate-Source Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 16 V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 40 V, V_{GS} = 0 V			1	µA
		V_{DS} = 40 V, V_{GS} = 0 V, T_J = 100 °C			20	
On-State Drain Current[a]	$I_{D(on)}$	$V_{DS} \geq$ 5 V, V_{GS} = 10 V	30			A
Drain-Source On-State Resistance[a]	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 15 A		0.016	0.020	Ω
		V_{GS} = 4.5 V, I_D = 10 A		0.020	0.025	
Forward Transconductance[a]	g_{fs}	V_{DS} = 15 V, I_D = 15 A		42		S
Dynamic[b]						
Input Capacitance	C_{iss}	V_{DS} = 20 V, V_{GS} = 0 V, f = 1 MHz		1195		pF
Output Capacitance	C_{oss}			150		
Reverse Transfer Capacitance	C_{rss}			80		
Total Gate Charge	Q_g	V_{DS} = 20 V, V_{GS} = 10 V, I_D = 30 A		25	38	nC
		V_{DS} = 20 V, V_{GS} = 4.5 V, I_D = 30 A		11.4	18	
Gate-Source Charge	Q_{gs}			3.2		
Gate-Drain Charge	Q_{gd}			4.2		
Gate Resistance	R_g	f = 1 MHz		1.6	2.5	Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 20 V, R_L = 0.66 Ω $I_D \cong$ 30 A, V_{GEN} = 4.5 V, R_g = 1 Ω		13	20	ns
Rise Time	t_r			14	21	
Turn-Off Delay Time	$t_{d(off)}$			16	25	
Fall Time	t_f			7	14	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 20 V, R_L = 0.66 Ω $I_D \cong$ 30 A, V_{GEN} = 10 V, R_g = 1 Ω		6	12	
Rise Time	t_r			9	18	
Turn-Off Delay Time	$t_{d(off)}$			24	36	
Fall Time	t_f			7	14	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	T_C = 25 °C			20	A
Pulse Diode Forward Current[a]	I_{SM}				50	
Body Diode Voltage	V_{SD}	I_S = 10 A		0.87	1.2	V
Body Diode Reverse Recovery Time	t_{rr}	I_F = 20 A, dI/dt = 100 A/µs, T_J = 25 °C		25	38	ns
Body Diode Reverse Recovery Charge	Q_{rr}			22	33	nC
Reverse Recovery Fall Time	t_a			17		ns
Reverse Recovery Rise Time	t_b			8		

Notes:
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.

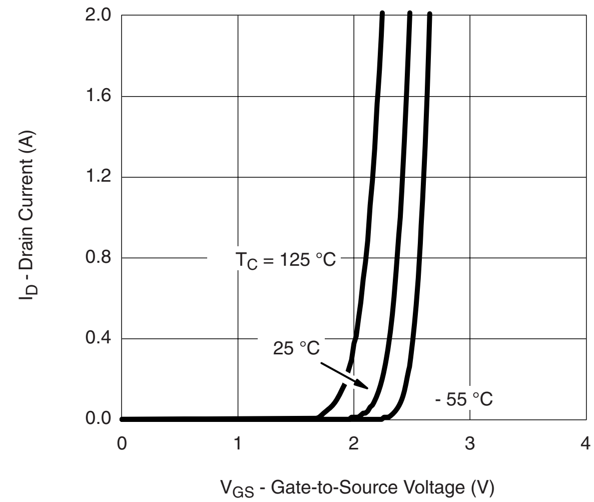
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Document Number: 74415
S-81956-Rev. B, 25-Aug-08

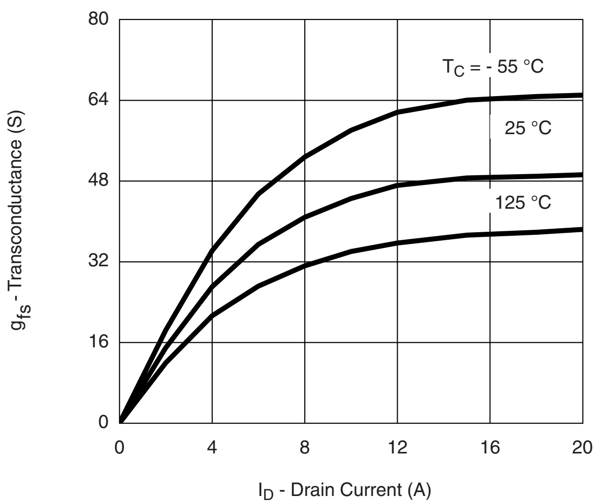
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



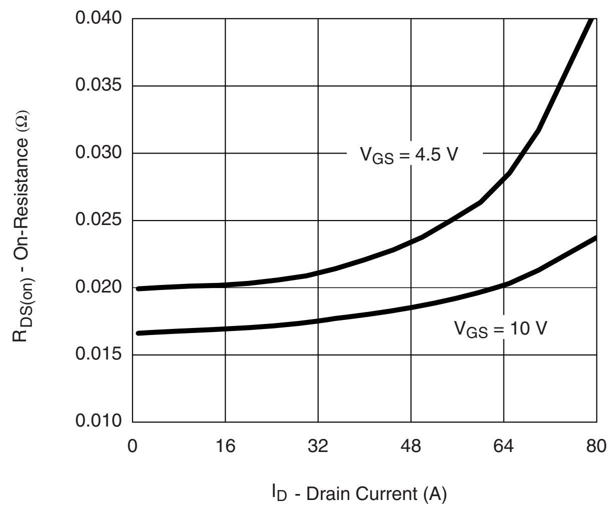
Output Characteristics



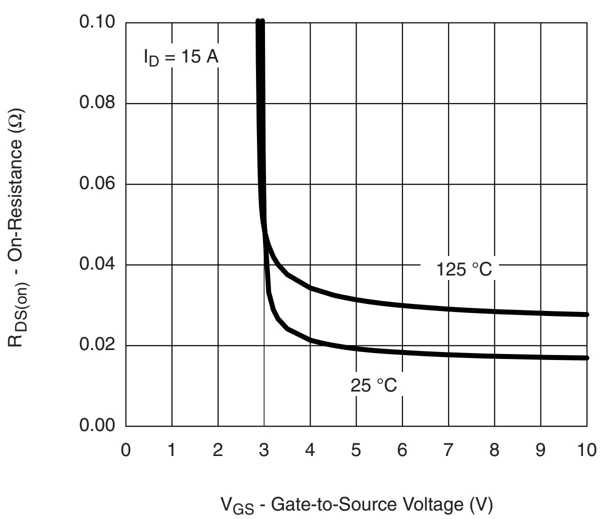
Transfer Characteristics



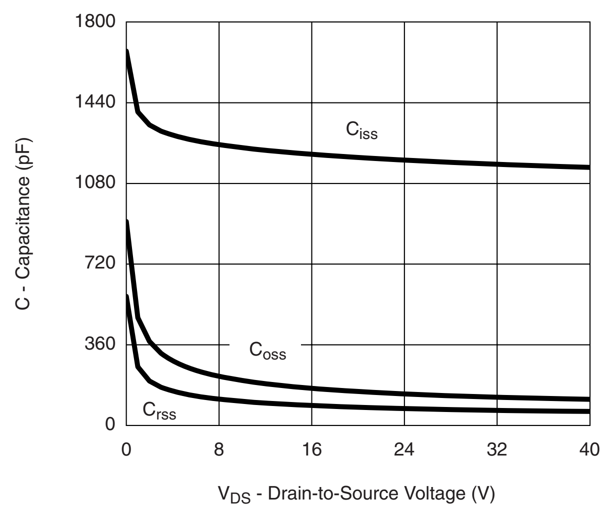
Transconductance



On-Resistance vs. Drain Current

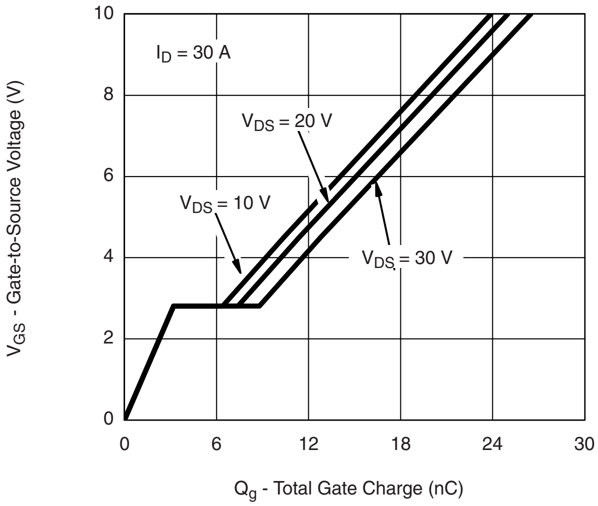


On-Resistance vs. Gate-to-Source Voltage

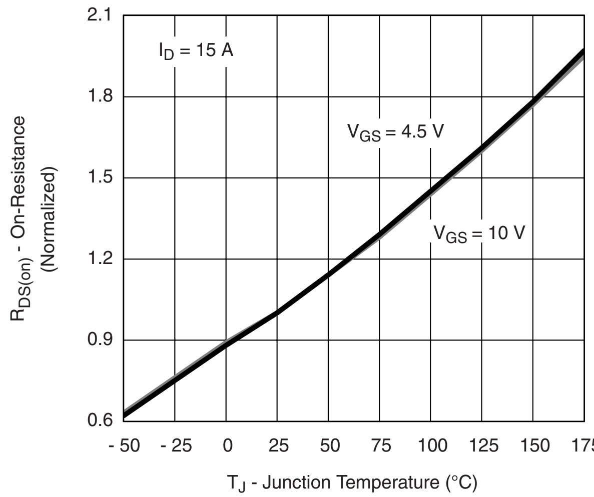


Capacitance

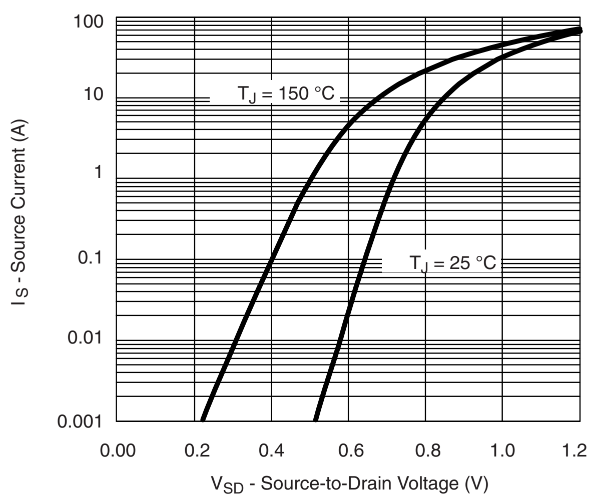
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



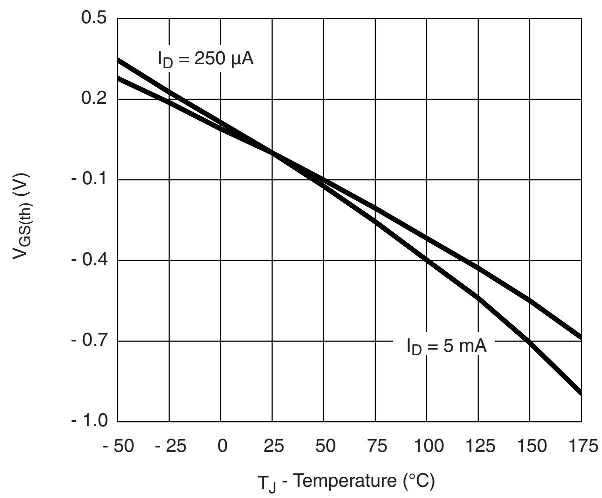
Gate Charge



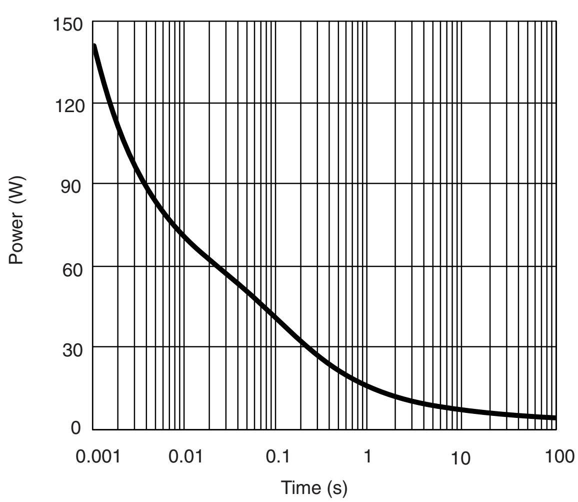
On-Resistance vs. Junction Temperature



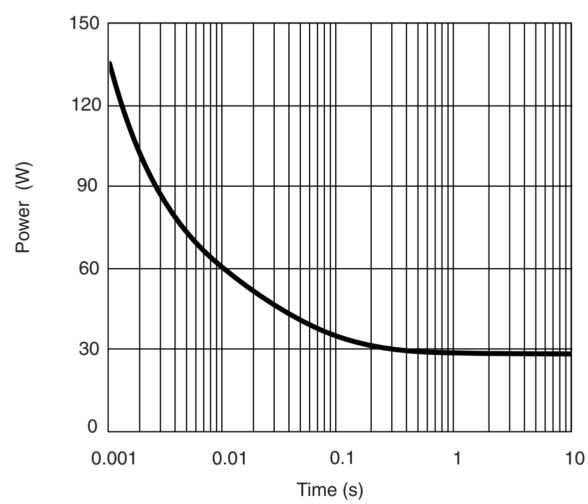
Source-Drain Diode Forward Voltage



Threshold Voltage

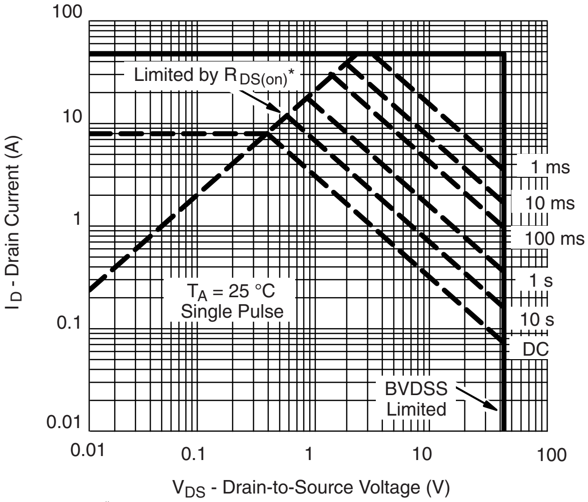


Single Pulse Power, Junction-to-Ambient



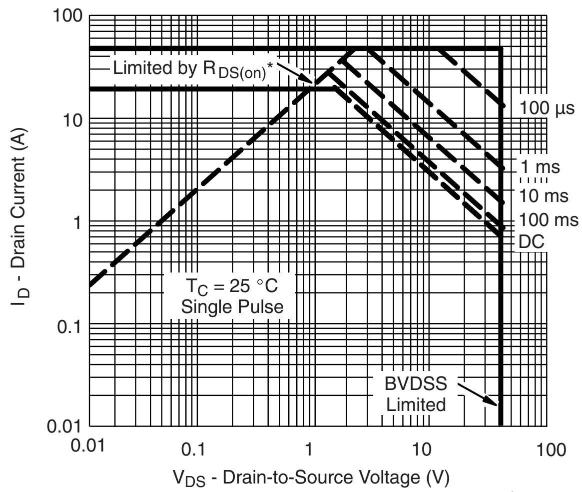
Single Pulse Power, Junction-to-Case

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



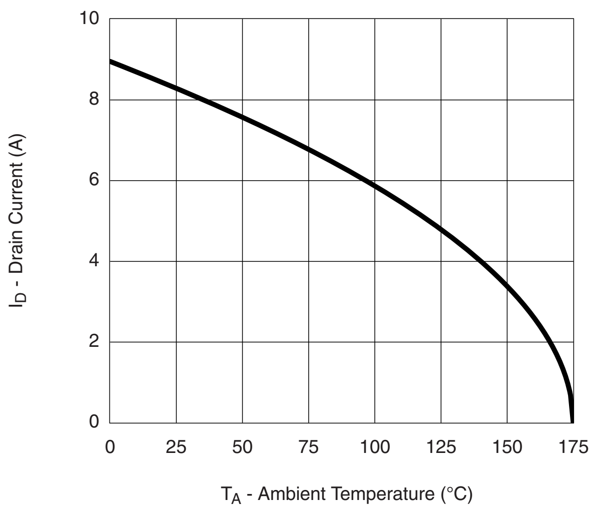
* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient

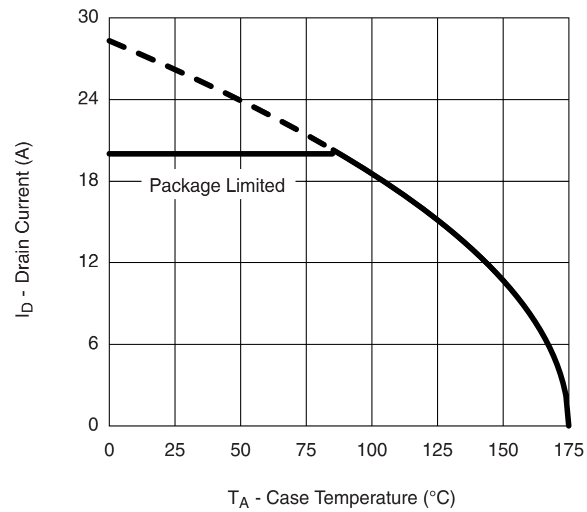


* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Case



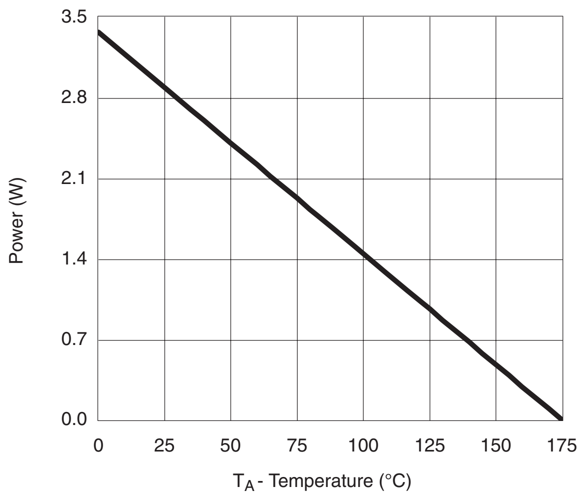
Current Derating, Junction-to-Ambient**



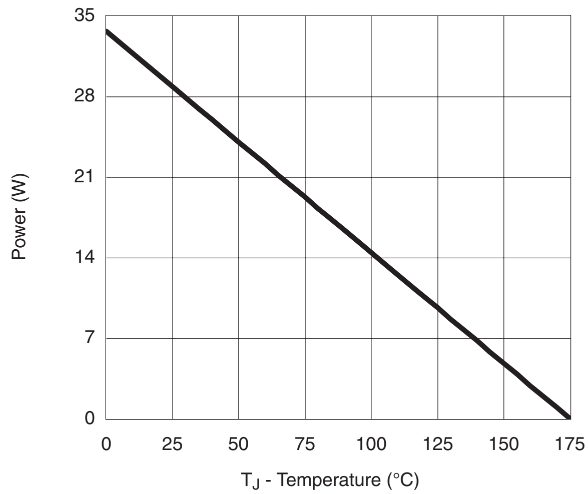
Current Derating, Junction-to-Case**

** The power dissipation P_D is based on $T_{J(max)}$ = 175 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



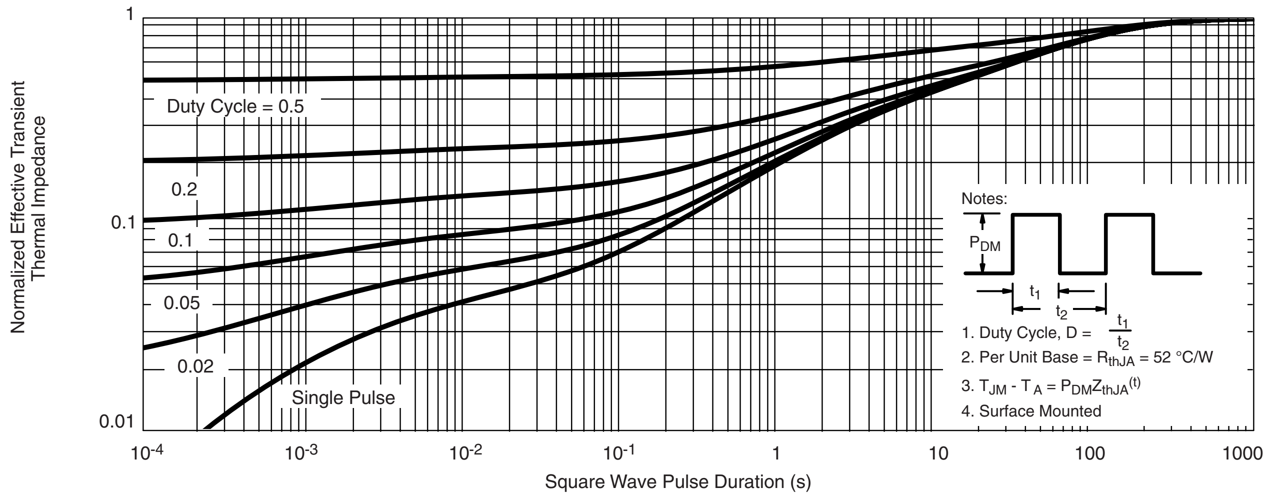
Power Derating*, Junction-to-Ambient



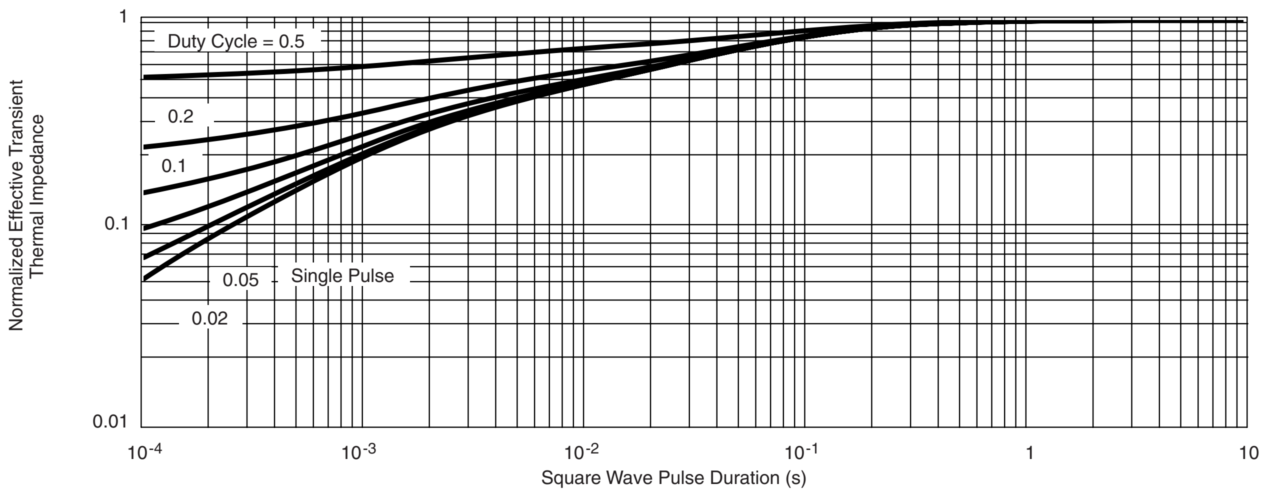
Power Derating*, Junction-to-Case

* The power dissipation P_D is based on $T_{J(max)}$ = 175 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see http://www.vishay.com/ppg?74415.

Disclaimer

All product specifications and data are subject to change without notice.

Vishay Intertechnology, Inc., its affiliates, agents, and employees, and all persons acting on its or their behalf (collectively, “Vishay”), disclaim any and all liability for any errors, inaccuracies or incompleteness contained herein or in any other disclosure relating to any product.

Vishay disclaims any and all liability arising out of the use or application of any product described herein or of any information provided herein to the maximum extent permitted by law. The product specifications do not expand or otherwise modify Vishay’s terms and conditions of purchase, including but not limited to the warranty expressed therein, which apply to these products.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document or by any conduct of Vishay.

The products shown herein are not designed for use in medical, life-saving, or life-sustaining applications unless otherwise expressly indicated. Customers using or selling Vishay products not expressly indicated for use in such applications do so entirely at their own risk and agree to fully indemnify Vishay for any damages arising or resulting from such use or sale. Please contact authorized Vishay personnel to obtain written terms and conditions regarding products designed for such applications.

Product names and markings noted herein may be trademarks of their respective owners.