TOSHIBA PHOTOCOUPLER GaAłAs IRED & PHOTO-IC

# TLP715F

## Isolated Bus Drivers High Speed Line Receivers Microprocessor System Interfaces

The Toshiba TLP715F consists of a GaAtAs light-emitting diode and an integrated high-gain, high-speed photodetector. This unit is a 6-pin SDIP. The TLP715F is 50% smaller than the 8-PIN DIP and meets the reinforced insulation class requirements of international safety standards. Therefore the mounting area can be reduced in equipment requiring safety standard certification.

The detector has a totem pole output stage to provide both source and sink driving. The detector IC has an internal shield that provides a guaranteed common-mode transient immunity of 10 kV/ $\mu$ s.

The TLP715F is buffer logic type. For inverter logic type, the TLP718F is in line-up.

Absolute maximum ratings and electrical characteristics are the same as in the TLP715 technical data sheets.

- Buffer logic output (totem pole output)
- Guaranteed performance over temperature : -40 to 100°C
- Power supply voltage : 4.5 to 20 V
- Input current: I<sub>FLH</sub> = 3mA (Max.)
- Switching time ( t<sub>pLH</sub> / t<sub>pHL</sub>) : 250 ns (Max.)
- Common-mode transient immunity : ±10 kV/µs (Min)
- Isolation voltage : 5000 Vrms (Min)
- UL recognized UL1577, File No.E67349
- c-UL recognized CSA Component Acceptance Service No. 5A, File No.E67349
- Option (D4)

TÜV recognized / VDE under application : DIN EN60747-5-2Maximum Operating Insulation Voltage : $1140V_{PK}$ Highest Permissible Over Voltage : $8000V_{PK}$ 

(Note) : When a EN60747-5-2 approved type is needed, Please designate "Option(D4)"

• Construction Mechanical Rating

	7.62 mm pitch standard type	10.16 mm pitch TLPXXXF type
Creepage Distance	7.0 mm (Min)	8.0 mm (Min)
Clearance	7.0 mm (Min)	8.0 mm (Min)
Insulation Thickness	0.4 mm (Min)	0.4 mm (Min)

#### **Truth Table**

Input	LED	Tr1	Tr2	Output
Н	ON	ON	OFF	Н
L	OFF	OFF	ON	L

Weight:0.26 g(typ.)

TOSHIBA

0.4±0.1

4.58±0.25

Η

25

6.8±0.

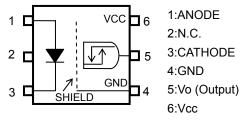
.65 +0.15

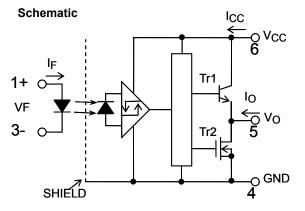
1.27±0.2

65

 $25\pm +0.0$ 

### Pin Configuration (Top View)





 $0.1 \ \mu\text{F}$  bypass capacitor must be connected between pins 6 and 4.



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11-5J101

7.62±0.25

11.7±0.3

11-5J101

0.75±0.25

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