ADVANCE INFORMATION SPECIFICATION

T-49-19-07

Z86C50

CMOS Z8® CCP™ ICE IN-CIRCUIT EMULATOR

FEATURES

- 8-bit CMOS Z8 CCP base In-Circuit Emulation chip
- 124-pin PGA package
- Full Z8 CCP family instruction set
- 3.0 to 5.5 volt operation range
- Clock speed 20 MHz
- 236-byte general-purpose register
- Low EMI mode programmable
- Internal register read bus and write bus interface
- Register file bank pointer and register file address bus interface for accessing the Expanded Register File (ERF) externally.
- Expanded Register control signals (/REGRD, /REGWR and /CE_ERF) interface
- All internal control signals interface (i.e., /SYNC, /IACK, /MAS, /MDS, etc.)
- Disable Timers control signal
- Hold internal clock control signal
- Wait control signal
- STOP and HALT modes signal status outputs
- Two on-board analog comparators
- Two programmable 8-bit Counter/Timers, each with a 6-bit programmable prescaler
- Six vectored, priority interrupts from six different sources
- Internal program memory size select interface

GENERAL DESCRIPTION

The Z86C50 CCP In-Circuit Emulation (ICE) chip introduces a new level of sophistication to ICE architecture. The Z86C50 not only provides all the control signal interfaces, but also the internal register bus interface. The Expanded Register File (ERF) can be external and interface with the internal register bus and ERF control signals.

The Z86C50 allows users to prototype a system with an actual hardware device and to develop the code. Also, this device is very useful in emulator applications.

Figure 1 is the functional block diagram of Z86C50. This device is housed in a 124-pin PGA package (Figure 2). Table 1 is the pin identification of the Z86C50.

Note: All Signals with a preceding front slash, "/", are active Low, e.g.: B/W (WORD is active Low); /B/W (BYTE is active Low, only).

GENERAL DESCRIPTION (Continued)

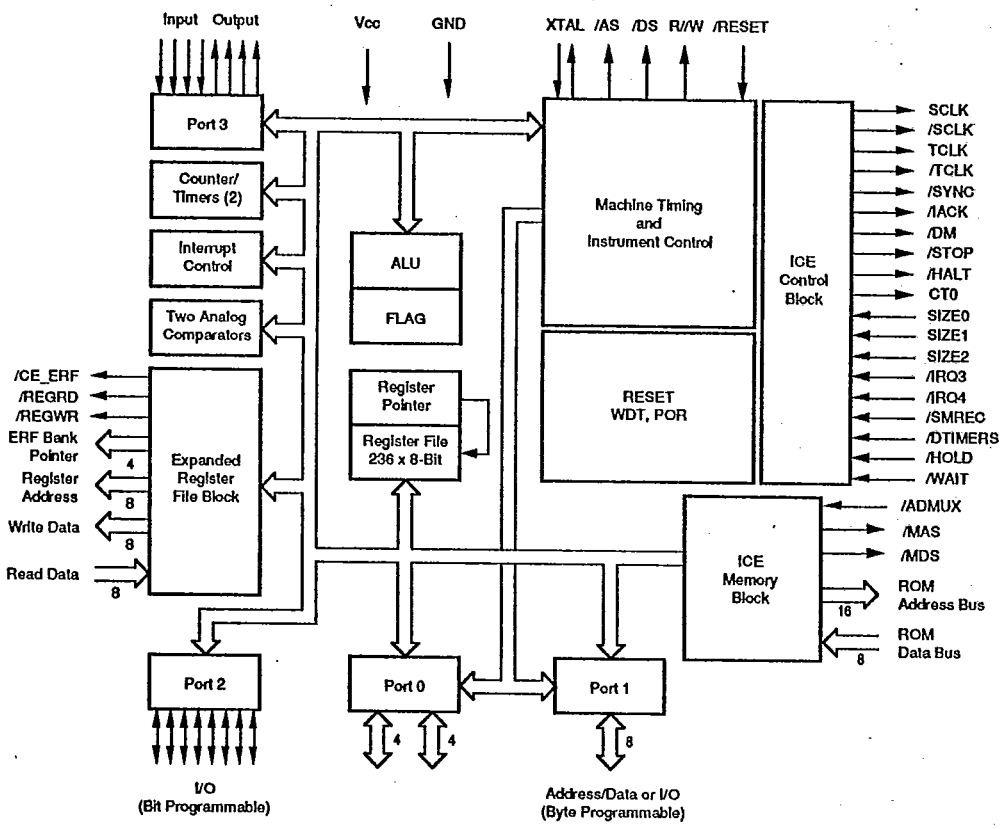


Figure 1. Functional Block Diagram

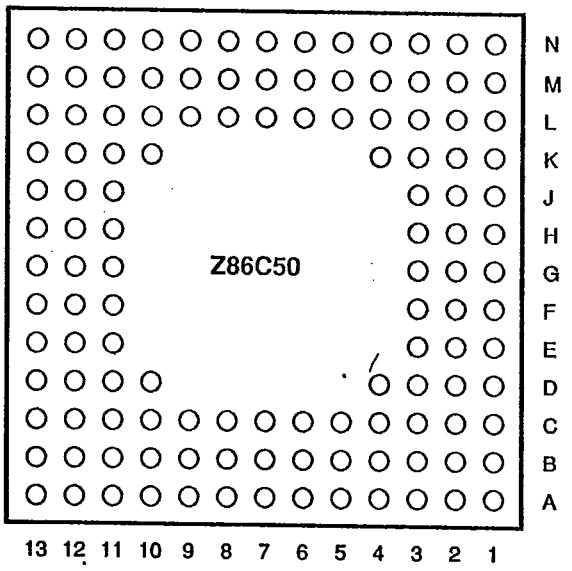


Figure 2. 124-Pin Grid Array Pin Assignments (Top View)

PIN DESCRIPTION

T-49-19-07

Table 1. Pin Identification

Pin #	Symbol	Function	Direction
C3	P30	Port 3 pin 0	Input
B2	P31	Port 3 pin 1	Input
B1	P32	Port 3 pin 2	Input
D3	P33	Port 3 pin 3	Input
C2	P34	Port 3 pin 4	Output
C1	P35	Port 3 pin 5	Output
D2	P36	Port 3 pin 6	Output
E3	V_{cc}	Power Supply	Input
D1	P37	Port 3 pin 7	Output
E2	P10	Port 1 pin 0	In/Output
E1	P11	Port 1 pin 1	In/Output
F3	P12	Port 1 pin 2	In/Output
F2	P13	Port 1 pin 3	In/Output
F1	GND	Ground, V_{ss}	Input
G2	P14	Port 1 pin 4	In/Output
G3	P15	Port 1 pin 5	In/Output
G1	P16	Port 1 pin 6	In/Output
H1	P17	Port 1 pin 7	In/Output
H2	/DM	Data Memory Strobe	Output
H3	GND	Ground	Input
J1	/RESET	Reset	Input
J2	/DTIMERS	Disable Timers	Input
K1	/HOLD	Hold Control	Input
J3	R//W	Read/Write	Output
K2	/DS	Data Strobe	Output
L1	/AS	Address Strobe	Output
M1	SCLK	System Clock	Output
K3	/SYNC	Instruction Sync. Signal	Output
L2	/IACK	Interrupt Acknowledge	Output
N1	/MAS	Interrupt Memory Address strobe	Output
K4	/WAIT	Wait Control	Input
L3	/MDS	Interrupt Memory Data Strobe	Output
M2	A15	Internal Address Line 15	Output
N2	A14	Internal Address Line 14	Output
L4	A13	Internal Address Line 13	Output
M3	A12	Internal Address Line 12	Output
N3	A11	Internal Address Line 11	Output
M4	A10	Internal Address Line 10	Output
L5	/SMR	Stop mode recovery	Input
N4	A9	Internal Address Line 9	Output
M5	A8	Internal Address Line 8	Output
N5	A7	Internal Address Line 7	Output
L6	A6	Internal Address Line 6	Output
M6	A5	Internal Address Line 5	Output
N6	A4	Internal Address Line 4	Output
M7	A3	Internal Address Line 3	Output

Pin #	Symbol	Function	Direction
L7	A2	Internal Address Line 2	Output
N7	GND	Ground, V_{ss}	Input
N8	A	Internal Address Line 1	Output
M8	A0	Internal Address Line 0	Output
L8	/ADMUX	Address/Data Bus Multiplex	Input
N9	GND	Ground	Input
M9	XTAL2	Oscillator Output	Output
N10	V_{cc}	Power Supply	Input
L9	/IRQ4	Interrupt Request 4	Input
M10	/IRQ3	Interrupt Request 3	Input
N11	XTAL1	Oscillator Input	Input
N12	RBP0	Reg. Bank Pointer bit 0	Output
L10	RBP1	Reg. Bank Pointer bit 1	Output
M11	RBP2	Reg. Bank Pointer bit 2	Output
N13	RBP3	Reg. Bank Pointer bit 3	Output
K10	/SCLK	System Clock (inverted)	Output
L11	IWD0	Internal Reg. Write Bus D0	Output
M12	IWD1	Internal Reg. Write Bus D1	Output
M13	IWD2	Internal Reg. Write Bus D2	Output
L12	IWD4	Internal Reg. Write Bus D4	Output
L13	IWD5	Internal Reg. Write Bus D5	Output
K12	IWD6	Internal Reg. Write Bus D6	Output
J11	IWD7	Internal Reg. Write Bus D7	Output
K13	/REGWR	Register Write	Output
J12	/REGRD	Register Read	Output
J13	GND	Ground, V_{ss}	Input
H11	RA0	Register Address Line 0	Output
H12	RA1	Register Address Line 1	Output
H13	RA2	Register Address Line 2	Output
G12	RA3	Register Address Line 3	Output
G11	RA4	Register Address Line 4	Output
G13	RA5	Register Address Line 5	Output
F13	RA6	Register Address Line 6	Output
F12	RA7	Register Address Line 7	Output
F11	CT0	Counter/Timer 0 Output	Output
E13	IRD0	Internal Reg. Read Bus D0	Input
E12	IRD1	Internal Reg. Read Bus D1	Input
D13	V_{cc}	Power Supply	Input
E11	IRD2	Internal Reg. Read Bus D2	Input
D12	IRD3	Internal Reg. Read Bus D3	Input
C13	IRD4	Internal Reg. Read Bus D4	Input
B13	IRD5	Internal Reg. Read Bus D5	Input
D11	IRD6	Internal Reg. Read Bus D6	Input
C12	IRD7	Internal Reg. Read Bus D7	Input
A13	TCLK	Timer Clock Output	Output
D10	/STOP	STOP Signal	Output
C11	/CE_ERF	ERF Chip Select	Output
B12	D0	Internal Memory Data Line 0	In/Output

Table 1. Pin Identification (Continued)

Pin #	Symbol	Function	Direction
A12	D1	Internal Memory Data Line 1	In/Output
C10	D2	Internal Memory Data Line 2	In/Output
B11	D3	Internal Memory Data Line 3	In/Output
A11	D4	Internal Memory Data Line 4	In/Output
B10	D5	Internal Memory Data Line 5	In/Output
C9	D6	Internal Memory Data Line 6	In/Output
A10	D7	Internal Memory Data Line 7	In/Output
B9	SIZE0	Size Select 0	Input
A9	SIZE1	Size Select 1	Input
C8	SIZE2	Size Select 2	Input
B8	P00	Port 0 Pin 0	In/Output
A8	P0	Port 0 Pin 1	In/Output
B7	P0	Port 0 Pin 2	In/Output
C7	P0	Port 0 Pin 3	In/Output
A7	GND	Ground, V_{ss}	Input
A6	P0	Port 0 Pin 4	In/Output
B6	P0	Port 0 Pin 5	In/Output
C6	P0	Port 0 Pin 6	In/Output
B5	P2	Port 2 Pin 0	In/Output
A4	V_{cc}	Power Supply	Input
C5	P2	Port 2 Pin 1	In/Output
B4	P2	Port 2 Pin 2	In/Output
A3	P2	Port 2 Pin 3	In/Output
A2	P2	Port 2 Pin 4	In/Output
C4	P2	Port 2 Pin 5	In/Output
B3	P2	Port 2 Pin 6	In/Output
A1	P2	Port 2 Pin 7	In/Output
D4	/HALT	HALT Signal	Output

PIN FUNCTIONS

P00-P07. Port 0, nibble programmable. Port 0 can be configured as input, output or address lines.

P10-P17. Port 1, byte programmable. Port 1 can be configured as input, output or multiplexed address/data lines.

P20-P27. Port 2, bit programmable. Port 2 can be configured as input or output lines.

P30-P33. Port 3 input lines, P31-P33 can be configured as analog input.

P34-P37. Port 3 output lines.

A0-A15. *Internal Memory Address Bus* (Output). The internal memory can address up to 32 Kbyte.

/ADMUX. *Address/Data Bus Multiplexed* (Input). When this pin is low, A7-A0 is address and data bus multiplexing (AD7-AD0). When this pin is high, A15-A0 outputs the address only. This pin has an internal pull-up resistor.

D7-D0 *(In/Output).* Internal Memory Data Bus.

R/W. Read/Write Signal output line.

SIZE0-SIZE2. *Internal Memory Size* (Input). These three pins select the internal memory size (Table 2).

Table 2. Memory Size Table

SIZE2	SIZE1	SIZE0	Memory Size
0	0	0	0 Kbyte
0	0	1	2 Kbytes
0	1	0	4 Kbytes
0	1	1	8 Kbytes
1	0	0	16 Kbytes
1	0	1	32 Kbytes

RBP0-RBP3. *Register Bank Pointer* (Output). The RBP points to the current register bank. The ERF is located in bank %1 to bank %F.

RA7-RA0. *Register Address Bus* (Output). This bus is used to access each of 256 byte registers of the current register bank.

IWD7-IWD0. *Register Write Bus* (Output). This bus is used to write the data to the register.

/REGWR. *Register Write signal* (Output). This pin goes low during each register write cycle.

IRD7-IRD0. *Register Read Bus* (Input). This bus is used to read the data from the register.

/REGRD. *Register Read signal* (Output). This pin goes low during each register read cycle.

/CE_ERF. *ERF Chip Enable* (Output). This pin goes active when the ERF is accessed and inactive when the on-board register file is accessed.

/DM. *Data Memory Strobe* (Output). This pin goes low during data memory access.

/MDS. *Internal Memory Data Strobe* (Output). This pin goes low during each internal memory fetch cycle.

/MAS. *Internal Memory Address Strobe* (Output). This pin goes low during each T1 cycle.

/DS. *Data Strobe* (Output). This pin goes low during each external memory fetch cycle.

/AS. *Address Strobe* (Output). This pin goes low during each T1 cycle.

PIN FUNCTIONS (Continued)

T-49-19-07

SCLK. System Clock output pin.

/SCLK. Inverse System Clock output pin.

/SYNC. *Instruction Sync Signal* (Output). This signal indicates the last clock of the current executing instruction.

/IACK. *Interrupt Acknowledge* (Output). This pin goes low during an interrupt cycle.

/IRQ3. Interrupt Request 3 input line.

/IRQ4. Interrupt Request 4 input line.

/DTIMERS. *Disable Timers* (Input). All timers (including the WDT) are stopped by the low level at this pin. This pin has an internal pull-up resistor.

/HOLD. *Hold* (Input). The internal clock is stopped by the low level at this pin. The on-board oscillator keeps on oscillating. This pin has an internal pull-up resistor.

/WAIT. *Wait* (Input). The code execution is stopped after completion of the currently executing instruction by the low level at this pin. The address of the fetching byte is latched. /AS goes high and /DS goes low. The high level at this pin releases from WAIT. This pin has an internal pull-up resistor.

/HALT. *HALT Mode Indication* (Output). The low level of this pin indicates the ICE chip in HALT mode.

/STOP. *STOP Mode Indication* (Output). The low level of this pin indicates the ICE chip in STOP mode.

/SMR. *STOP Mode Recovery* (Input). Low level at this pin wakes up the ICE chip from STOP mode.

TCLK. *Timer Clock Output lines.* The frequency of TCLK is the same as SCLK. TCLK drives the timer and interrupt logic.

CT0. Counter/Timer 0 output line.

TIMING DIAGRAMS

Figure 3 shows the configuration of ICE Control Register (ICECON) which selects the access timing of the Expanded Register File.

Figures 4 through 9 are the preliminary access timing diagrams of the register file.

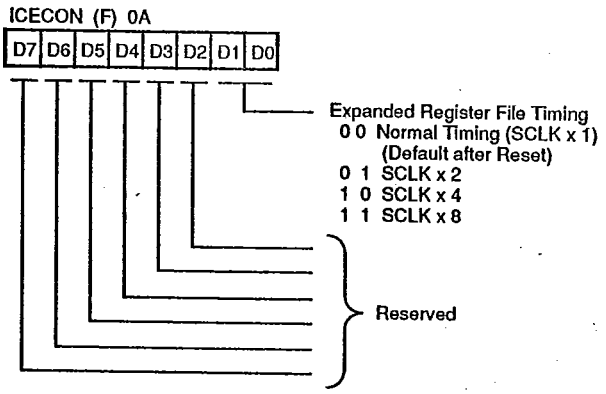


Figure 3. ICE Control Register

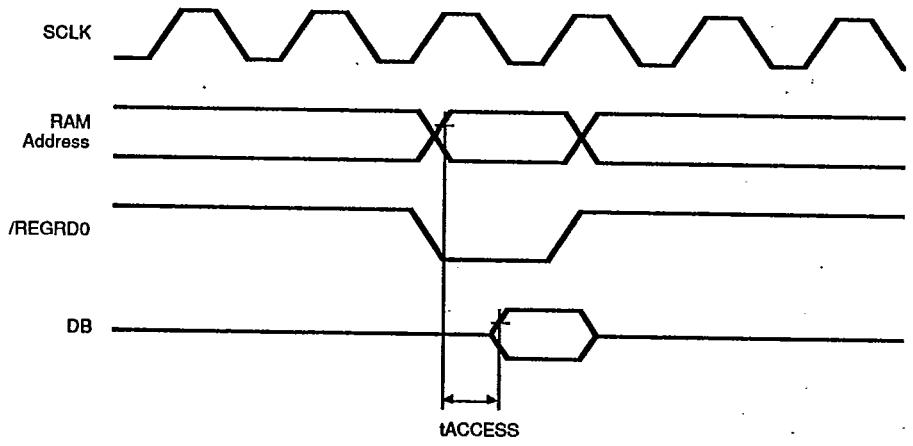


Figure 4. Internal Register File Read Cycle For Indirect Addressing

TIMING DIAGRAMS (Continued)

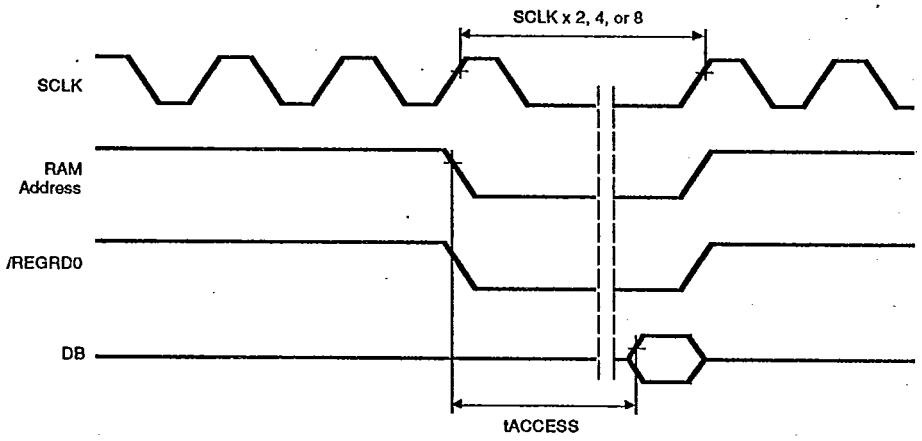


Figure 5. Internal Register File Read Cycle For Indirect Addressing (Extended Timing)

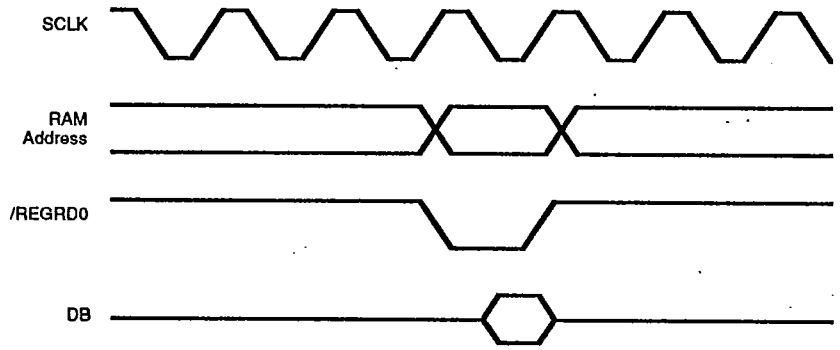


Figure 6. Internal Register File Write Cycle

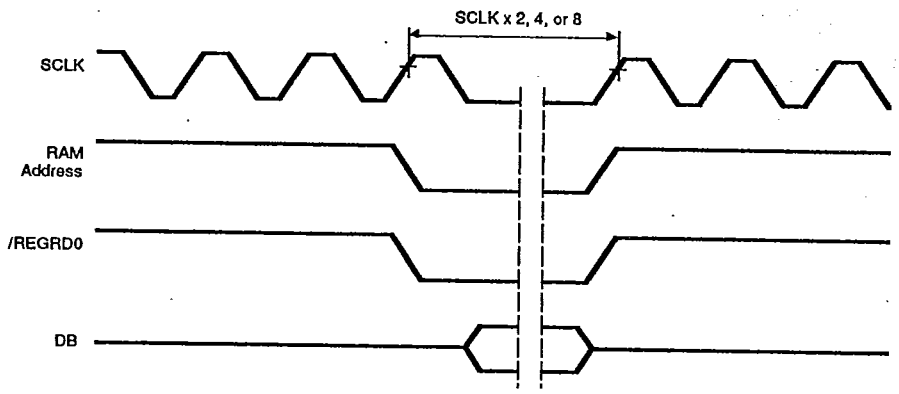


Figure 7. Internal Register File Write Cycle (Extended Timing)

TIMING DIAGRAMS (Continued)

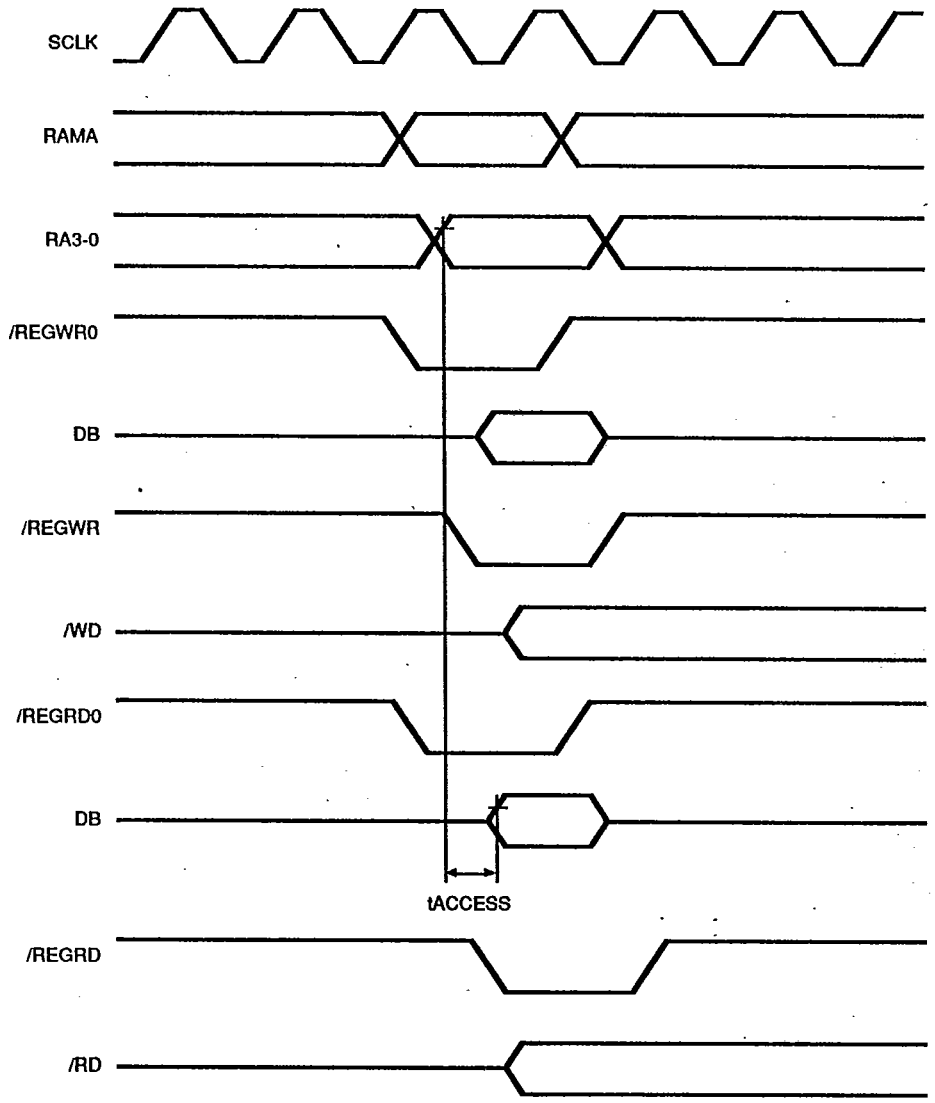


Figure 8. External Read And Write Timing (Normal Timing)

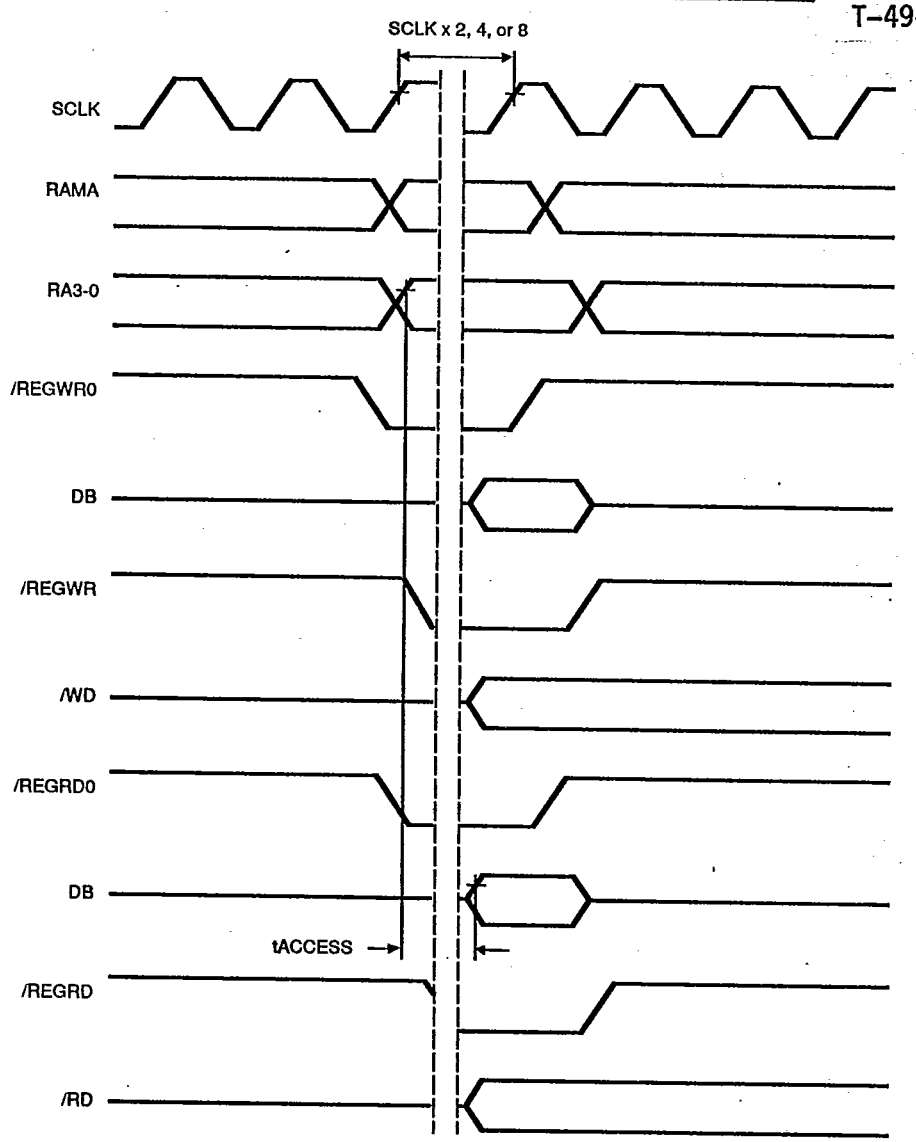
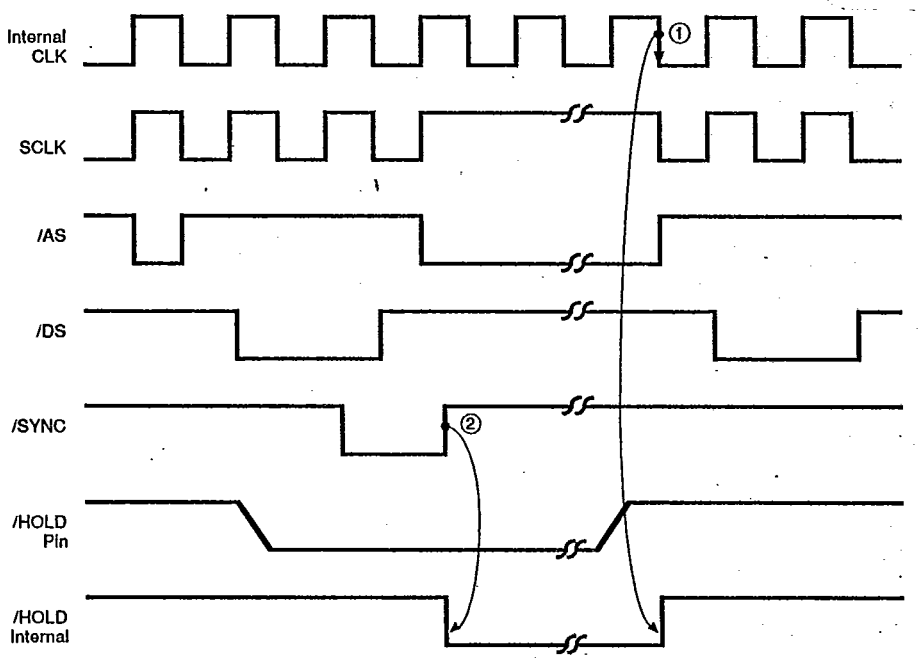
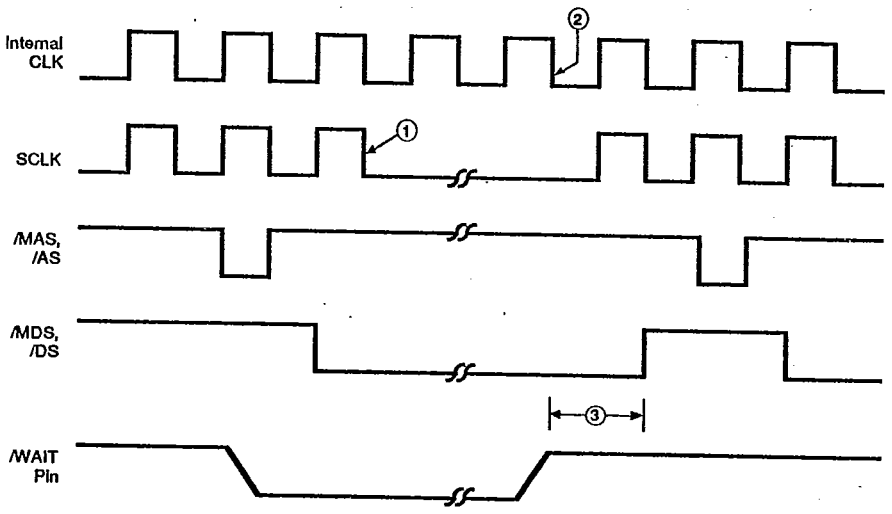


Figure 9. External Read And Write Timing (Extended Timing)



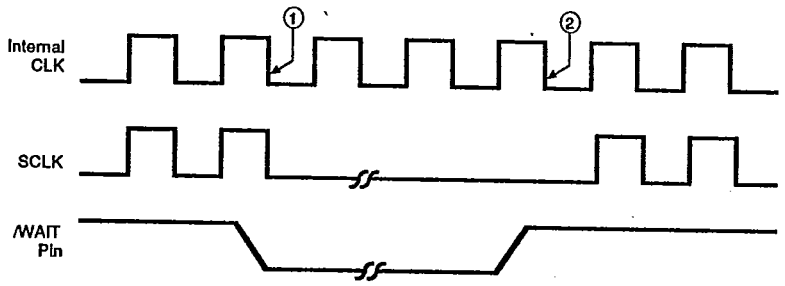
Notes:
1. SCLK, TCLK go HIGH
2. /AS, /MAS go LOW

Figure 10. HOLD Timing Diagram



Notes:
1. WAIT Pin sampled during /MDS, /DS Low
2. WAIT Released
3. Remainder of /DS
TCLK not affected by /WAIT function

Figure 11. WAIT Timing Diagram



Notes:
1. /DTIMERS Pin Samples
2. /DTIMERS Released

Figure 12. DTIMERS Timing Diagram