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# MOS FIELD EFFECT TRANSISTOR 2SK3642

# SWITCHING N-CHANNEL POWER MOS FET

#### **DESCRIPTION**

The 2SK3642 is N-channel MOS FET device that features a low on-state resistance and excellent switching characteristics, and designed for low voltage high current applications such as DC/DC converter with synchronous rectifier.

#### **ORDERING INFORMATION**

| PART NUMBER | PACKAGE         |
|-------------|-----------------|
| 2SK3642-ZK  | TO-252 (MP-3ZK) |

#### **FEATURES**

· Low on-state resistance

 $R_{DS(on)1}$  = 9.5 m $\Omega$  MAX. (Vgs = 10 V, ID = 32 A)  $R_{DS(on)2}$  = 16 m $\Omega$  MAX. (Vgs = 4.5 V, ID = 18 A)

- Low Ciss: Ciss = 1100 pF TYP.
- · Built-in gate protection diode

(TO-252)



#### ABSOLUTE MAXIMUM RATINGS (TA = 25°C)

| Drain to Source Voltage (VGS = 0 V) | VDSS                  | 30           | V  |
|-------------------------------------|-----------------------|--------------|----|
| Gate to Source Voltage (VDS = 0 V)  | Vgss                  | ±20          | V  |
| Drain Current (DC) (Tc = 25°C)      | ID(DC)                | ±64          | Α  |
| Drain Current (pulse) Note1         | I <sub>D(pulse)</sub> | ±190         | Α  |
| Total Power Dissipation (Tc = 25°C) | P <sub>T1</sub>       | 36           | W  |
| Total Power Dissipation             | P <sub>T2</sub>       | 1.0          | W  |
| Channel Temperature                 | Tch                   | 150          | °C |
| Storage Temperature                 | Tstg                  | -55 to + 150 | °C |
| Single Avalanche Current Note2      | las                   | 25           | Α  |
| Single Avalanche Energy Note2       | Eas                   | 62           | mJ |

**Notes 1.** PW  $\leq$  10  $\mu$ s, Duty Cycle  $\leq$  1%

2. Starting T<sub>ch</sub> = 25°C, V<sub>DD</sub> = 15 V, R<sub>G</sub> = 25  $\Omega$ , L = 100  $\mu$ H, V<sub>GS</sub> = 20  $\rightarrow$  0 V

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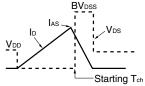
#### **ELECTRICAL CHARACTERISTICS (TA = 25°C)**

| CHARACTERISTICS                          | SYMBOL               | TEST CONDITIONS                                | MIN. | TYP. | MAX. | UNIT |
|--|----------------------|--|------|------|------|------|
| Zero Gate Voltage Drain Current          | IDSS                 | V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V  |      |      | 10   | μΑ   |
| Gate Leakage Current                     | Igss                 | V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0 V |      |      | ±10  | μΑ   |
| Gate Cut-off Voltage                     | V <sub>GS(off)</sub> | V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA  | 1.5  |      | 2.5  | V    |
| Forward Transfer Admittance Note         | <b>y</b> fs          | V <sub>DS</sub> = 10 V, I <sub>D</sub> = 32 A  | 13   | 26   |      | S    |
| Drain to Source On-state Resistance Note | RDS(on)1             | V <sub>GS</sub> = 10 V, I <sub>D</sub> = 32 A  |      | 7.6  | 9.5  | mΩ   |
|  | RDS(on)2             | V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 18 A |      | 10.8 | 16   | mΩ   |
| Input Capacitance                        | Ciss                 | V <sub>DS</sub> = 10 V                         |      | 1100 |      | pF   |
| Output Capacitance                       | Coss                 | V <sub>GS</sub> = 0 V                          |      | 410  |      | pF   |
| Reverse Transfer Capacitance             | Crss                 | f = 1 MHz                                      |      | 150  |      | pF   |
| Turn-on Delay Time                       | t <sub>d(on)</sub>   | V <sub>DD</sub> = 15 V, I <sub>D</sub> = 32 A  |      | 9.6  |      | ns   |
| Rise Time                                | tr                   | V <sub>GS</sub> = 10 V                         |      | 5.1  |      | ns   |
| Turn-off Delay Time                      | t <sub>d(off)</sub>  | $R_G = 10 \Omega$                              |      | 38   |      | ns   |
| Fall Time                                | tr                   |  |      | 10   |      | ns   |
| Total Gate Charge                        | Q <sub>G</sub>       | V <sub>DD</sub> = 24 V                         |      | 23   |      | nC   |
| Gate to Source Charge                    | Qgs                  | V <sub>GS</sub> = 10 V                         |      | 4.3  |      | nC   |
| Gate to Drain Charge                     | Q <sub>GD</sub>      | I <sub>D</sub> = 64 A                          |      | 6    |      | nC   |
| Body Diode Forward Voltage Note          | V <sub>F(S-D)</sub>  | I <sub>F</sub> = 64 A, V <sub>GS</sub> = 0 V   |      | 1.0  |      | V    |
| Reverse Recovery Time                    | trr                  | I <sub>F</sub> = 64 A, V <sub>GS</sub> = 0 V   |      | 31   |      | ns   |
| Reverse Recovery Charge                  | Qrr                  | di/dt = 100 A/μs                               |      | 25   |      | nC   |

**Note** Pulsed: PW  $\leq$  350  $\mu$ s, Duty Cycle  $\leq$  2%

#### **TEST CIRCUIT 1 AVALANCHE CAPABILITY**

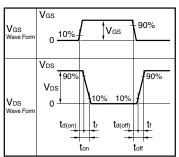
# $V_{GS} = 20 \rightarrow 0 \text{ V}$ $PG. \bigcirc V_{M}$ $V_{DD}$ $PG. \bigcirc V_{M}$ $V_{DD}$ $PG. \bigcirc V_{M}$ $PG. \bigcirc V_{M}$



# PG. Ru Nob

**TEST CIRCUIT 2 SWITCHING TIME** 





#### **TEST CIRCUIT 3 GATE CHARGE**

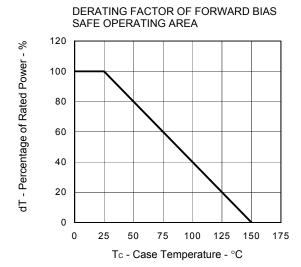
$$\begin{array}{c|c} D.U.T. \\ I_G = 2 \text{ mA} \\ \hline \end{array}$$

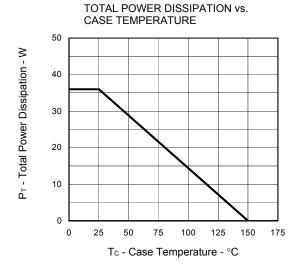
$$\begin{array}{c|c} PG. & \begin{array}{c} \\ \\ \\ \end{array} \end{array} \begin{array}{c} SD.U.T. \\ \hline \end{array}$$

$$\begin{array}{c|c} \\ \\ \end{array} \begin{array}{c} \\$$

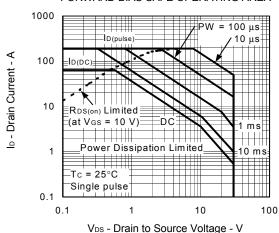


#### TYPICAL CHARACTERISTICS (TA = 25°C)

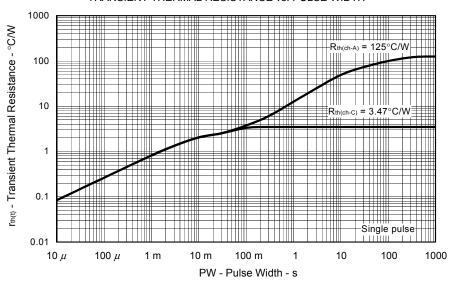




#### FORWARD BIAS SAFE OPERATING AREA

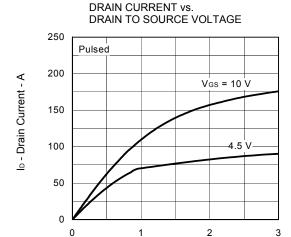


#### TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



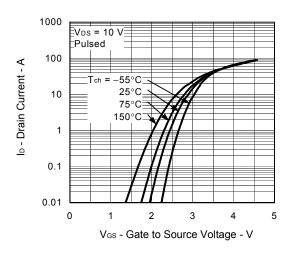
3

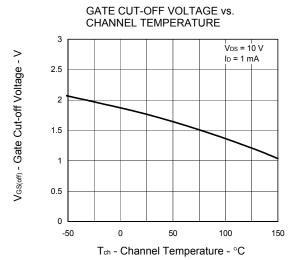




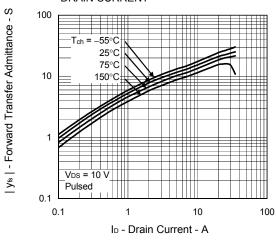
VDS - Drain to Source Voltage - V

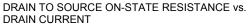
#### FORWARD TRANSFER CHARACTERISTICS

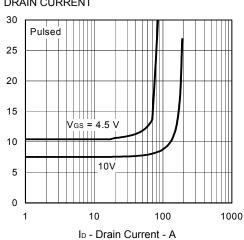




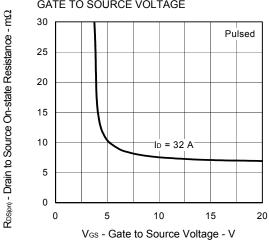
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT





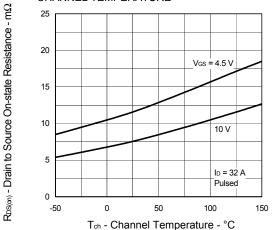


DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

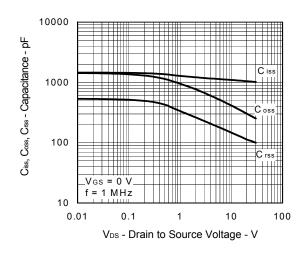


R<sub>DS(on)</sub> - Drain to Source On-state Resistance - mΩ

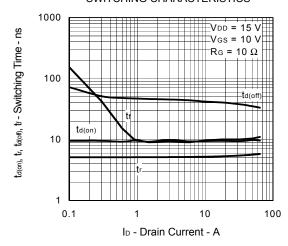
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



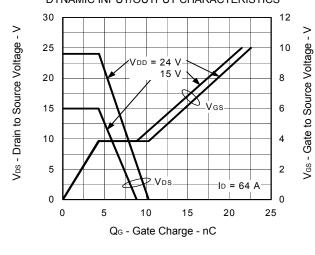
#### CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



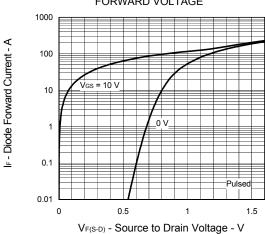
#### SWITCHING CHARACTERISTICS



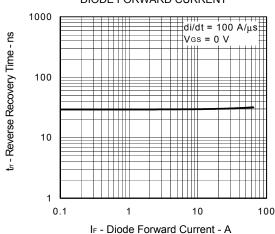
#### DYNAMIC INPUT/OUTPUT CHARACTERISTICS



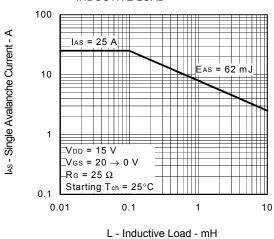
### SOURCE TO DRAIN DIODE FORWARD VOLTAGE



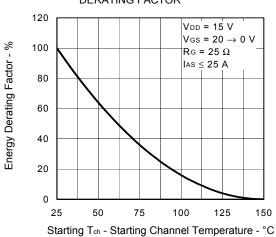
# REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT



## SINGLE AVALANCHE CURRENT vs. INDUCTIVE LOAD



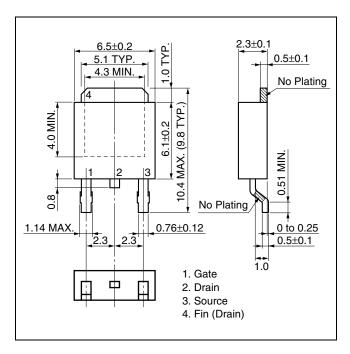
## SINGLE AVALANCHE ENERGY DERATING FACTOR



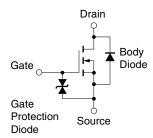


#### **★ PACKAGE DRAWING (Unit: mm)**

#### TO-252 (MP-3ZK)



#### **EQUIVALENT CIRCUIT**



**Remark** The diode connected between the gate and source of the transistor serves as a protector against ESD.

When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

Data Sheet D15970EJ4V0DS 7

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