DATA SHEET

74F543
Octal registered transceiver, non-inverting (3-State)

74F544
Octal registered transceiver, inverting (3-State)

Product specification

1994 Dec 5

IC15 Data Handbook

PHILIPS

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Octal registered transceivers 74F543, 74F544

74F543 Octal registered transceiver, non-inverting (3-State)
74F544 Octal registered transceiver, inverting 93-State)

FEATURES

- Combines74F245 and 74F373 type functions in one chip
- 8-bit octal transceiver with D-type latch
- 74F543 Non-inverting
  74F544 Inverting
- Back-to-back registers for storage
- Separate controls for data flow in each direction
- A outputs sink 20mA and source 3mA
- B outputs sink 64mA and source 15mA
- 3-State outputs for bus-oriented applications
- 74F543 available in SSOP Type II package

DESCRIPTION

The 74F543 and 74F544 Octal Registered Transceivers contain two sets of D-type latches for temporary storage of data flowing in either direction. Separate Latch Enable ($\overline{LEAB}$, $\overline{LEBA}$) and Output Enable ($\overline{OEAB}$, $\overline{OEBA}$) inputs are provided for each register to permit independent control of inputting and outputting in either direction of data flow. While the 74F543 has non-inverting data path, the 74F544 inverts data in both directions. The A outputs are guaranteed to sink 24mA, while the B outputs are rated for 64mA.

FUNCTIONAL DESCRIPTION

The 74F543 and 74F544 contain two sets of eight D-type latches, with separate input and controls for each set. For data flow from A to B, for example, the A-to-B Enable ($\overline{EAB}$) input must be Low in order to enter data from A0 - A7 or take data from B0 - B7, as indicated in the Function Table. With $\overline{EAB}$ Low, a Low signal on the A-to-B Latch Enable ($\overline{LEAB}$) input makes the A-to-B latches transparent; a subsequent Low-to-High transition for the $\overline{LEAB}$ signal puts the A latches in the storage mode and their outputs no longer change with the A inputs. With $\overline{EAB}$ and $\overline{OEAB}$ both Low, the 3-State B output buffers are active and display the data present at the outputs of the A latches. Control of data flow from B to A is similar, but using the $\overline{EBA}$, $\overline{LEBA}$, and $\overline{OEBA}$ inputs.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F543	6.0ns	80mA
74F544	6.5ns	95mA

ORDERING INFORMATION

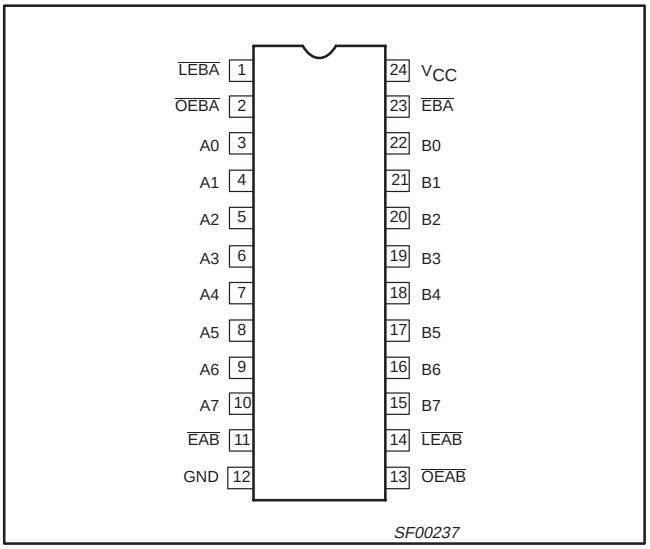
DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_A = 0°C to +70°C	DRAWING NUMBER
24-pin plastic skinny DIP (300mil)	N74F543N, N74F544N	SOT222–1
24-pin plastic SOL	N74F543D, N74F544D	SOT137-1
24-pin plastic SSOP Type II	74F543DB	SOT340-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

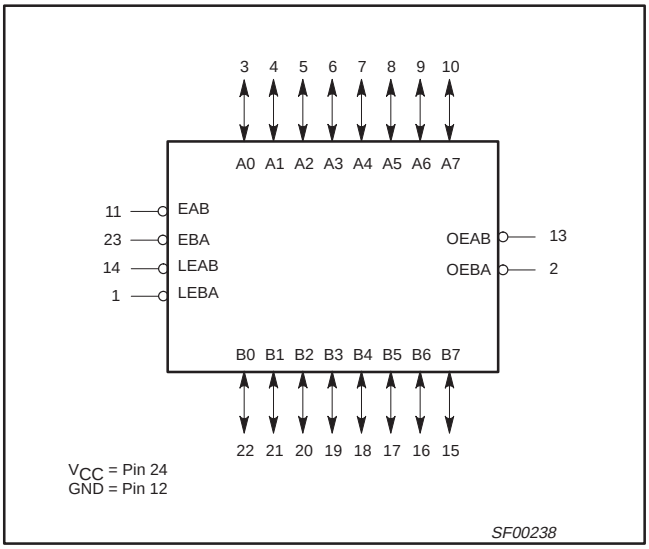
PINS		DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
74F543 74F544	A0 - A7	Port A, 3-State inputs	3.5/1.0	70µA/0.6mA
	B0 - B7	Port B, 3-State inputs	3.5/1.0	70µA/0.6mA
	$\overline{OEAB}$	A-to-B Output Enable input (Active Low)	1.0/1.0	20µA/0.6mA
	$\overline{OEBA}$	B-to-A Output Enable input (Active Low)	1.0/1.0	20µA/0.6mA
	$\overline{EAB}$	A-to-B Enable input (Active Low)	1.0/2.0	20µA/1.2mA
	$\overline{EBA}$	B-to-A Enable input (Active Low)	1.0/2.0	20µA/1.2mA
	$\overline{LEAB}$	A-to-B Latch Enable input (Active Low)	1.0/1.0	20µA/0.6mA
	$\overline{LEBA}$	B-to-A Latch Enable input (Active Low)	1.0/1.0	20µA/0.6mA
74F543	A0 - A7	Port A, 3-State outputs	150/40	3.0mA/24mA
	B0 - B7	Port B, 3-State outputs	750/106.7	15mA/64mA
74F544	$\overline{A}$0 - $\overline{A}$7	Port $\overline{A}$, 3-State outputs	150/40	3.0mA/24mA
	$\overline{B}$0 - $\overline{B}$7	Port $\overline{B}$, 3-State outputs	750/106.7	15mA/64mA

NOTE: One (1.0) FAST Unit Load is defined as: 20µA in the High State and 0.6mA in the Low state.

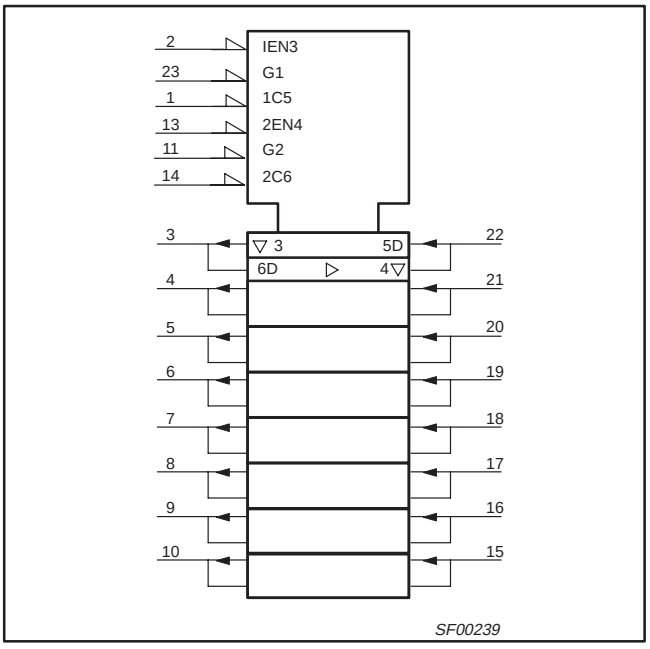
PIN CONFIGURATION – 74F543



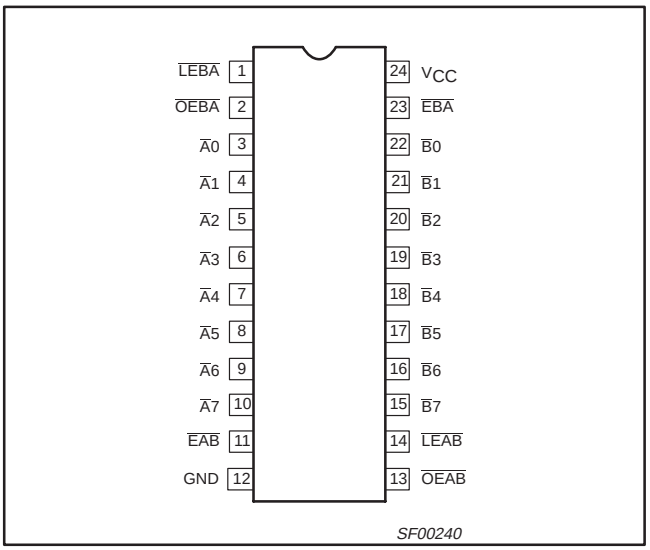
LOGIC SYMBOL – 74F543



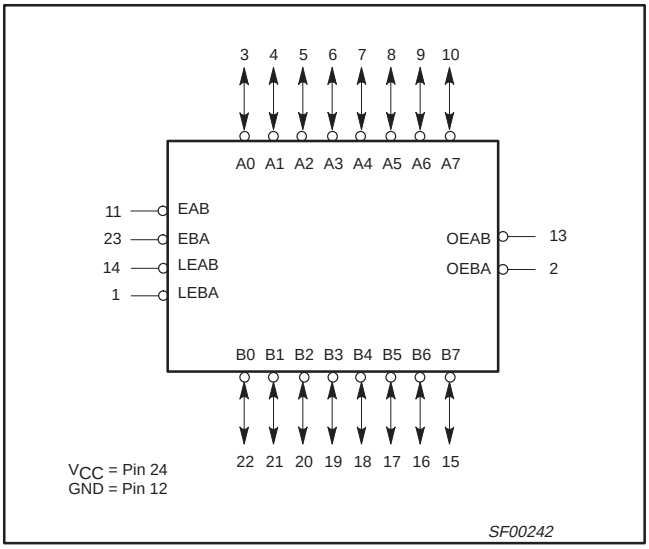
LOGIC SYMBOL (IEEE/IEC) – 74F543



PIN CONFIGURATION – 74F544



LOGIC SYMBOL – 74F544



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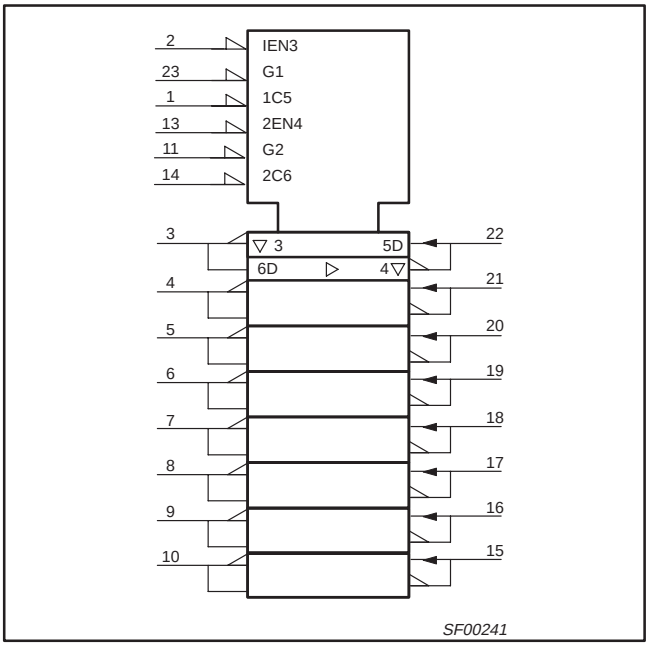
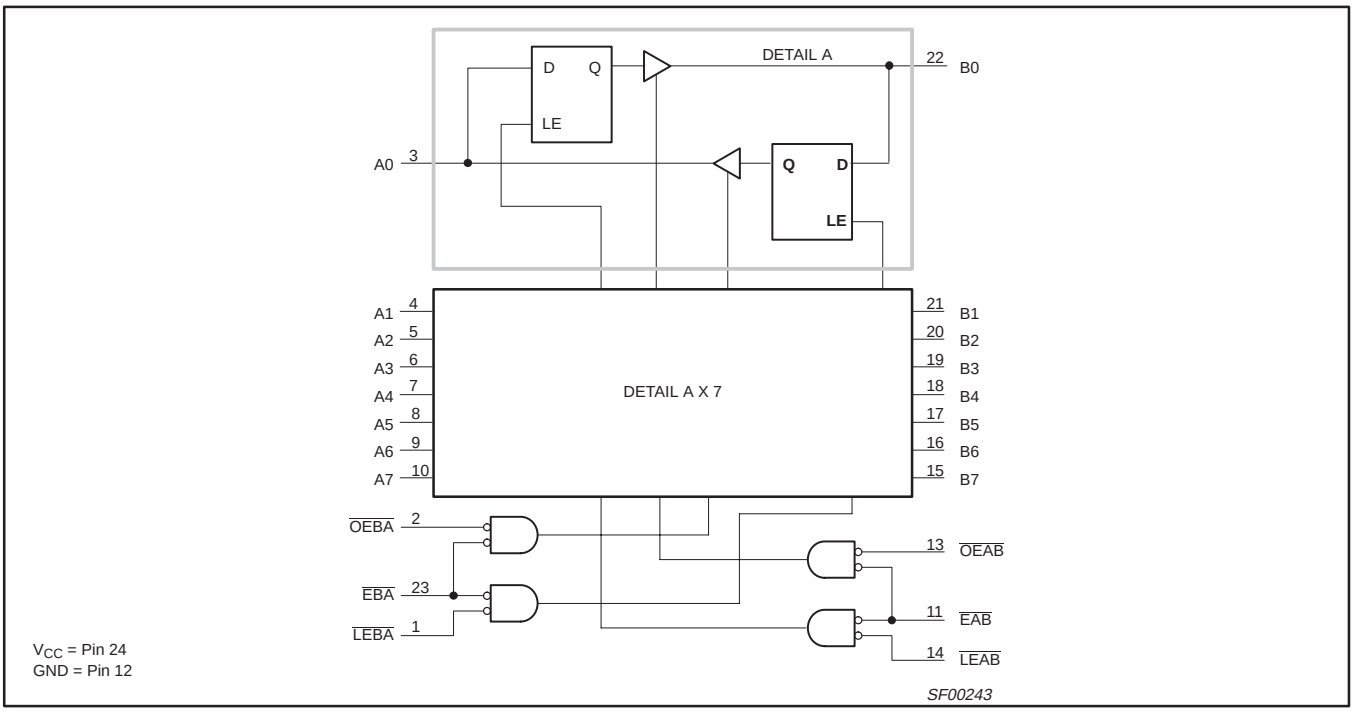


FUNCTION TABLE for 74F543 and 74F544

INPUTS				OUTPUTS		STATUS
$\overline{OEXX}$	$\overline{EXX}$	$\overline{LEXX}$	DATA	74F543	74F544	
H	X	X	X	Z	Z	Disabled
X	H	X	X	Z	Z	Disabled
L	↑	L	h	Z	Z	Disable + Latch
L	↑	L	l	Z	Z	
L	L	↑	h	H	L	Latch + Display
L	L	↑	l	L	H	
L	L	L	H	H	L	Transparent
L	L	L	L	L	H	
L	L	H	X	NC	NC	Hold

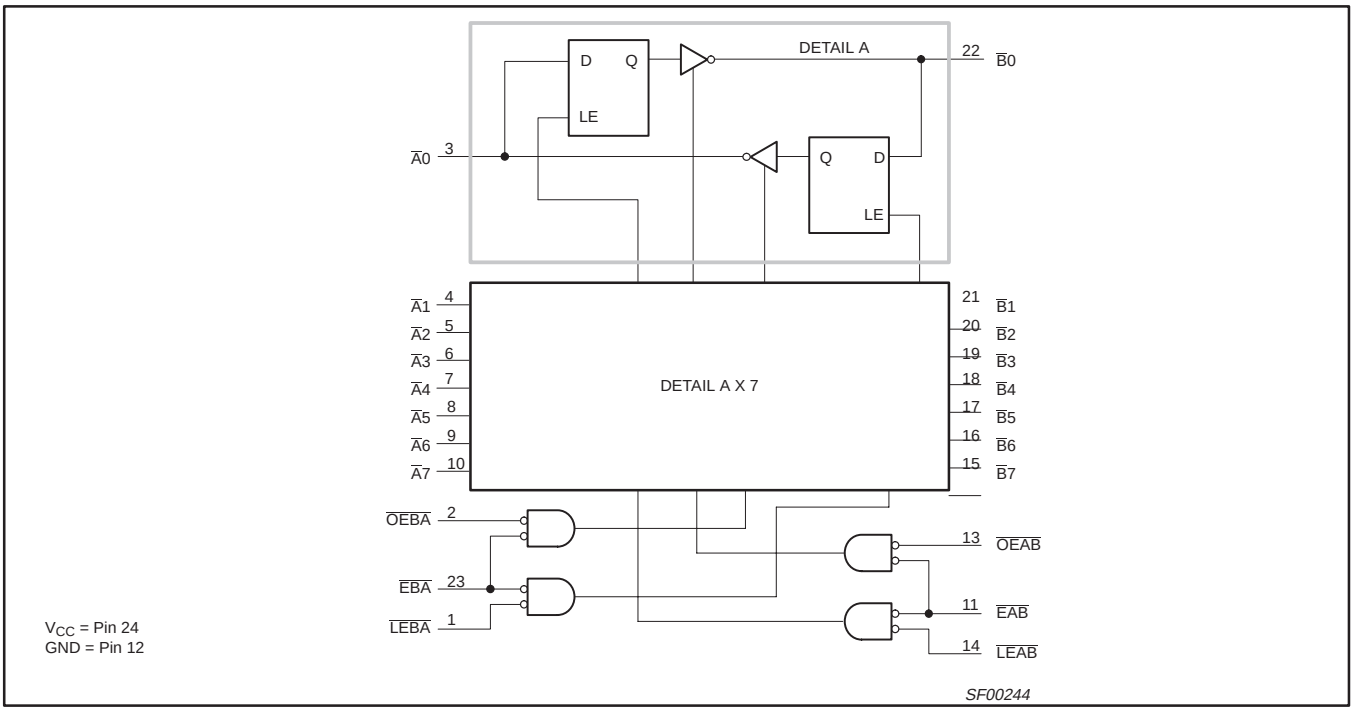
H = High voltage level
L = Low voltage level
h = High state must be present one setup time before the Low-to-High transition of $\overline{LEXX}$ or $\overline{EXX}$ (XX=AB or BA)
l = Low state must be present one setup time before the Low-to-High transition of $\overline{LEXX}$ or $\overline{EXX}$ (XX=AB or BA)
↑ = Low-to-High transition of $\overline{LEXX}$ or $\overline{EXX}$ XX = AB or BA
X = Don't care
NC = No change
Z = High impedance "off" state

LOGIC DIAGRAM FOR 74F543



V_{CC} = Pin 24
GND = Pin 12

LOGIC DIAGRAM FOR 74F544



V_{CC} = Pin 24
GND = Pin 12

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	A0 - A7, $\overline{A}0$ - $\overline{A}7$	48	mA
		B0 - B7, $\overline{B}0$ - $\overline{B}7$	128	mA
T_{amb}	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	A0 - A7, $\overline{A}0$ - $\overline{A}7$			-3	mA
		B0 - B7, $\overline{B}0$ - $\overline{B}7$			-15	mA
I_{OL}	Low-level output current	A0 - A7, $\overline{A}0$ - $\overline{A}7$			24	mA
		B0 - B7, $\overline{B}0$ - $\overline{B}7$			64	mA
T_{amb}	Operating free-air temperature range		-0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]			LIMITS			UNIT
							MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		A0 - A7, $\overline{A0}$ - $\overline{A7}$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = -3mA	±10%V_{CC}	2.4			V
						±5%V_{CC}	2.7	3.4		V
			B0 - B7, $\overline{B0}$ - $\overline{B7}$		I_{OH} = -15mA	±10%V_{CC}	2.0			V
						±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage		A0 - A7, $\overline{A0}$ - $\overline{A7}$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 24mA	±10%V_{CC}		0.35	0.50	V
						±5%V_{CC}		0.35	0.50	V
			B0 - B7, $\overline{B0}$ - $\overline{B7}$		I_{OL} = 64mA	±10%V_{CC}			0.55	V
						±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, I_I = I_{IK}				–0.73	–1.2	V
I_I	Input current at maximum input voltage		$\overline{OEAB}$, $\overline{OEBA}$, $\overline{EAB}$	V_{CC} = MAX, V_I = 7.0 V					100	µA
			Others	V_{CC} = 5.5, V_I = 5.5V					1	mA
I_{IH}	High-level input current			V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		Others	V_{CC} = MAX, V_I = 0.5V					–0.6	mA
			$\overline{EAB}$, $\overline{EBA}$						–1.2	mA
I_{OZH} + I_{IH}	Off-state output current, high-level voltage applied			V_{CC}= MAX, V_O = 2.7V					70	µA
I_{OZH} + I_{IL}	Off-state output current, Low-level voltage applied			V_{CC}= MAX, V_O = 0. 5V					–600	µA
I_{OS}	Short-circuit output current[3]		A0 - A7, $\overline{A0}$ - $\overline{A7}$	V_{CC} = MAX			–60		–150	mA
			B0 - B7, $\overline{B0}$ - $\overline{B7}$				–100		–225	mA
I_{CC}	Supply current (total)	74F543	I_{CCH}	V_{CC} = MAX				70	105	mA
			I_{CCL}					95	135	mA
			I_{CCZ}					95	135	mA
		74F544	I_{CCH}	V_{CC} = MAX				80	110	mA
			I_{CCL}					105	140	mA
			I_{CCZ}					100	135	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under the recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS FOR 74F543

SYMBOL	PARAMETER	TEST CONDITIONS	74F543 LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = 5.0V C_L = 50pF R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = 5.0V ± 10% C_L = 50pF R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n	Waveform 2	3.5 3.0	5.5 5.0	8.5 8.0	3.0 2.5	9.0 8.5	ns
t_{PLH} t_{PHL}	Propagation delay B_n to A_n	Waveform 2	2.5 2.5	4.0 4.5	7.0 7.5	2.5 2.5	7.5 8.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{LEBA}$ to A_n	Waveform NO TAG, 2	5.0 4.0	7.0 6.0	10.0 9.0	4.5 4.0	11.0 9.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{LEAB}$ to B_n	Waveform NO TAG, 2	6.0 4.5	8.5 6.5	11.5 9.5	5.5 4.0	12.5 10.0	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OEBA}$ to A_n or $\overline{OEAB}$ to B_n	Waveform 4 Waveform 5	2.0 3.5	4.0 5.0	7.5 8.5	1.5 3.0	8.0 9.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OEBA}$ to A_n or $\overline{OEAB}$ to B_n	Waveform 4 Waveform 5	1.0 1.5	3.0 4.0	6.5 7.5	1.0 1.0	7.5 8.5	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{EBA}$ to A_n or $\overline{EAB}$ to B_n	Waveform 4 Waveform 5	4.5 5.0	7.0 7.0	10.5 10.5	4.0 4.5	11.5 11.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{EBA}$ to A_n or $\overline{EAB}$ to B_n	Waveform 4 Waveform 5	2.5 4.5	5.0 7.0	8.5 11.0	2.0 3.0	9.5 12.0	ns

AC SETUP REQUIREMENTS FOR 74F543

SYMBOL	PARAMETER	TEST CONDITIONS	74F543 LIMITS				UNIT
			T_{amb} = +25°C V_{CC} = 5.0V C_L = 50pF R_L = 500Ω		T_{amb} = 0°C to +70°C V_{CC} = 5.0V ± 10% C_L = 50pF R_L = 500Ω		
			MIN	TYP	MIN	MAX	
t_s(H) t_s(L)	Setup time, High or Low A_n to $\overline{LEAB}$ or B_n to $\overline{LEBA}$	Waveform 3	0.0 2.5		0.0 3.0		ns
t_h(H) t_h(L)	Hold time, High or Low A_n to $\overline{LEAB}$ or B_n to $\overline{LEBA}$	Waveform 3	0.0 1.5		0.0 2.0		ns
t_s(H) t_s(L)	Setup time, High or Low A_n to $\overline{EAB}$ or B_n to $\overline{EBA}$	Waveform 3	1.0 2.5		1.5 3.0		ns
t_h(H) t_h(L)	Hold time, High or Low A_n to $\overline{EAB}$ or B_n to $\overline{EBA}$	Waveform 3	0.0 1.5		0.0 2.0		ns
t_w(L)	Latch enable pulse width, Low	Waveform 3	4.0		4.5		ns

AC ELECTRICAL CHARACTERISTICS FOR 74F544

SYMBOL	PARAMETER	TEST CONDITIONS	74F544 LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = 5.0V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C, V_{CC} = 5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ to $\overline{B}_n$ or $\overline{B}_n$ to $\overline{A}_n$	Waveform NO TAG	3.0 3.0	6.5 5.0	9.5 8.0	3.0 3.0	10.5 8.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{LEBA}$ to $\overline{A}_n$	Waveform NO TAG, 2	4.0 4.0	7.0 7.0	9.5 9.5	4.0 4.0	10.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{LEAB}$ to $\overline{B}_n$	Waveform NO TAG, 2	5.0 4.0	8.0 7.5	11.5 9.5	4.0 4.0	12.5 10.5	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OEBA}$ to $\overline{A}_n$ or $\overline{OEAB}$ to $\overline{B}_n$	Waveform 4 Waveform 5	2.0 3.5	4.0 5.5	7.0 8.5	1.5 3.0	7.5 9.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OEBA}$ to $\overline{A}_n$ or $\overline{OEAB}$ to $\overline{B}_n$	Waveform 4 Waveform 5	1.0 1.5	4.0 4.0	6.5 6.5	1.0 1.5	7.0 7.5	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{EBA}$ to $\overline{A}_n$ or $\overline{EAB}$ to $\overline{B}_n$	Waveform 4 Waveform 5	4.0 4.5	7.0 8.0	9.5 11.0	3.5 4.5	10.0 12.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{EBA}$ to $\overline{A}_n$ or $\overline{EAB}$ to $\overline{B}_n$	Waveform 4 Waveform 5	2.5 4.5	5.0 8.5	8.0 11.5	2.5 4.0	9.0 11.5	ns

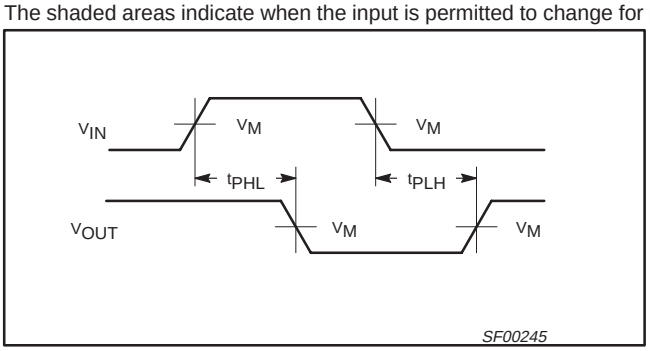
AC SETUP REQUIREMENTS FOR 74F544

SYMBOL	PARAMETER	TEST CONDITIONS	74F544 LIMITS				UNIT
			T_{amb} = +25°C, V_{CC} = 5.0V, C_L = 50pF, R_L = 500Ω		T_{amb} = 0°C to +70°C, V_{CC} = 5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MIN	MAX	
t_s(H) t_s(L)	Setup time, High or Low $\overline{A}_n$ to $\overline{LEAB}$ or $\overline{B}_n$ to $\overline{LEBA}$	Waveform 3	1.5 1.5		2.0 2.5		ns
t_h(H) t_h(L)	Hold time, High or Low $\overline{A}_n$ to $\overline{LEAB}$ or B_n to $\overline{LEBA}$	Waveform 3	1.5 2.0		2.5 2.5		ns
t_s(H) t_s(L)	Setup time, High or Low A_n to $\overline{EAB}$ or B_n to $\overline{EBA}$	Waveform 3	1.5 1.5		2.5 2.5		ns
t_h(H) t_h(L)	Hold time, High or Low $\overline{A}_n$ to $\overline{EAB}$ or $\overline{B}_n$ to $\overline{EBA}$	Waveform 3	1.5 2.0		2.0 2.0		ns
t_w(L)	Latch enable pulse width, Low	Waveform 3	4.0		4.5		ns

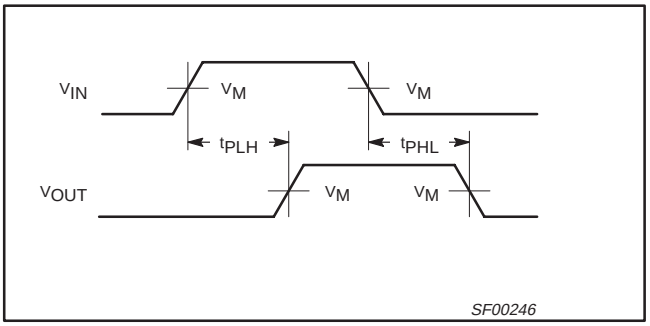
AC WAVEFORMS

V_M = 1.5V

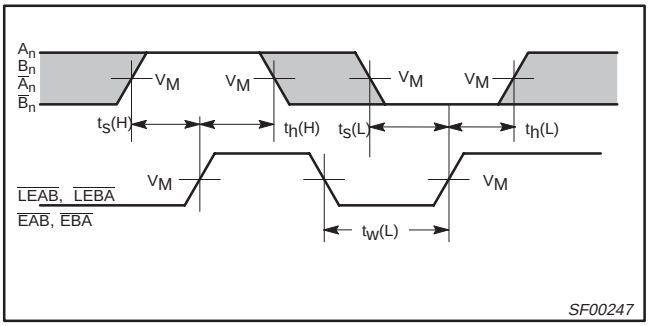
The shaded areas indicate when the input is permitted to change for predictable output performance.



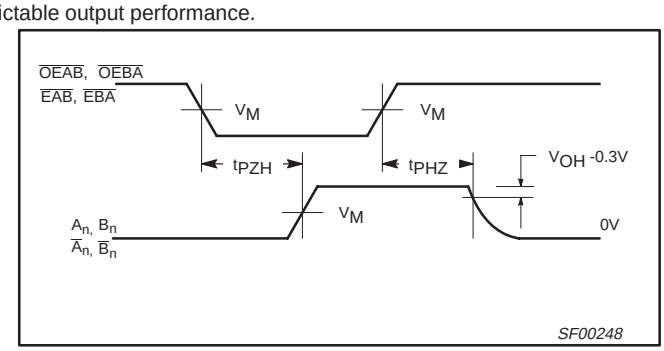
Waveform 1. Propagation Delay for Inverting Outputs



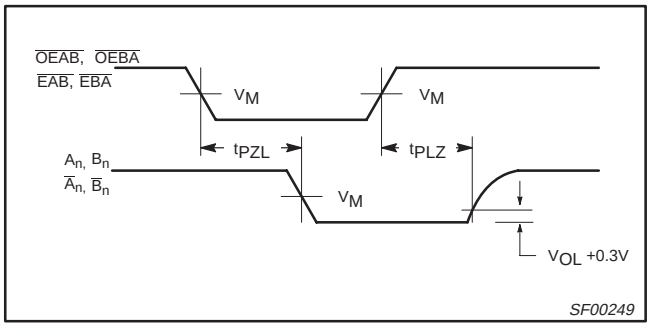
Waveform 2. Propagation Delay for Non-Inverting Outputs



Waveform 3. Data Setup Time and Hold Times, and Latch Enable Pulse Width

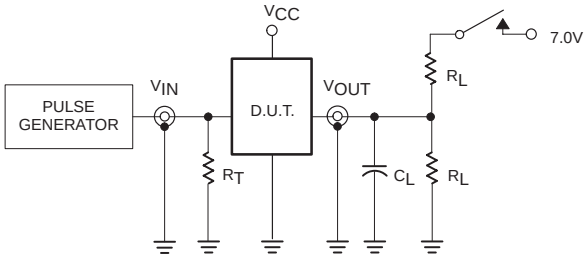


Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time from High Level

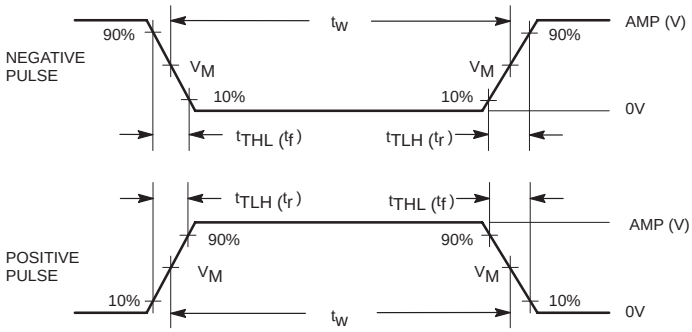


Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Open Collector Outputs



Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

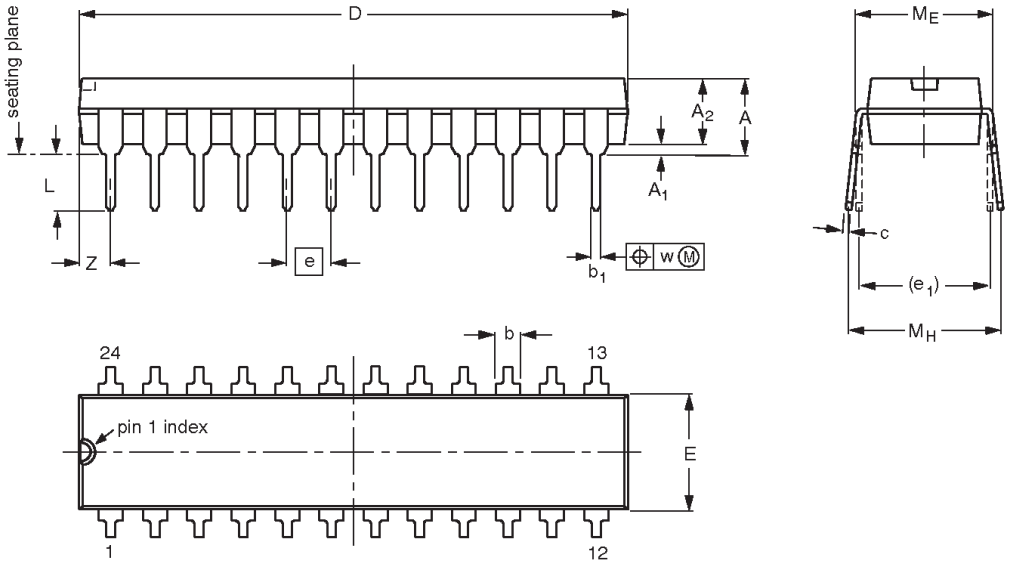
C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

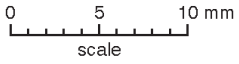
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00128

DIP24: plastic dual in-line package; 24 leads (300 mil) SOT222-1





DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

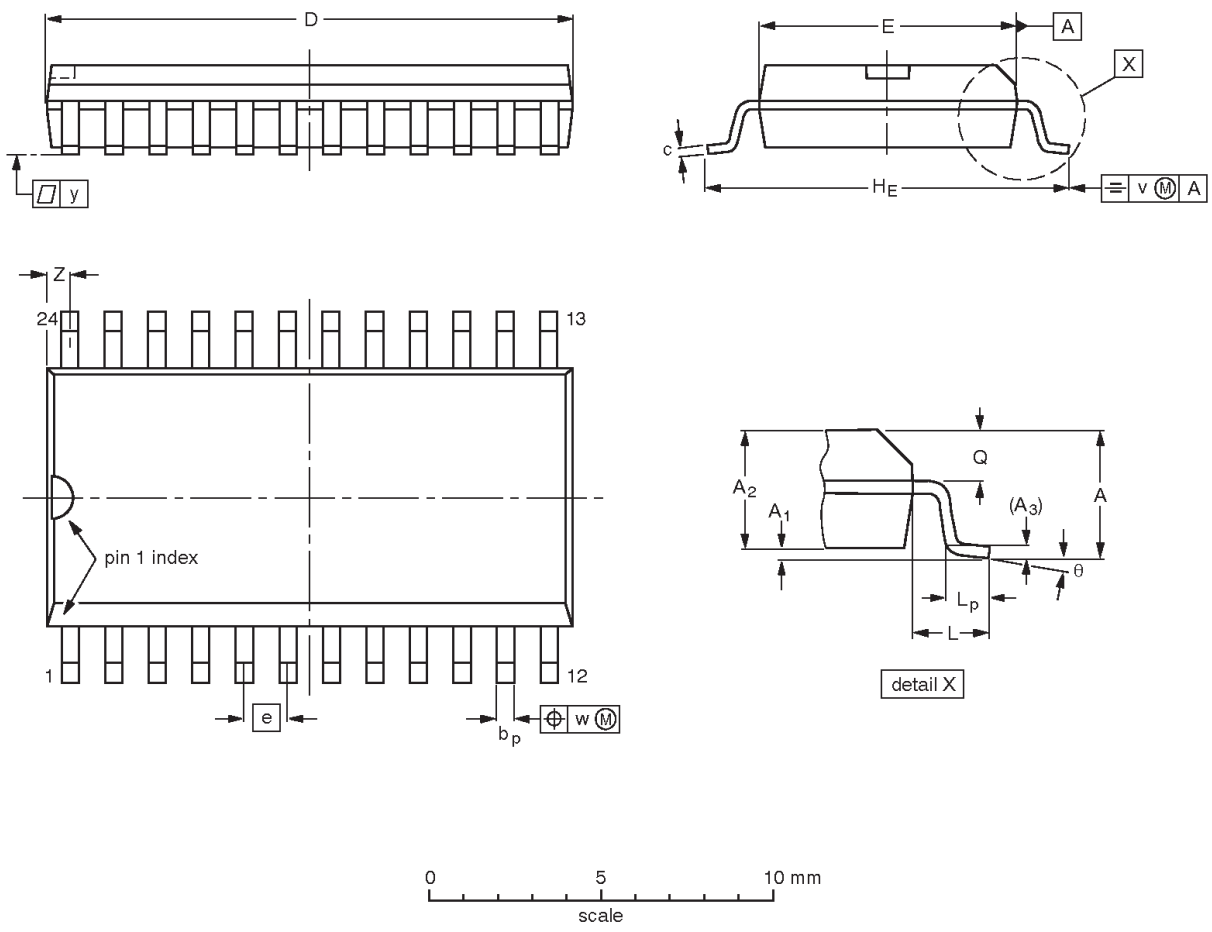
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.70	0.38	3.94	1.63 1.14	0.56 0.43	0.36 0.25	31.9 31.5	6.73 6.48	2.54	7.62	3.51 3.05	8.13 7.62	10.03 7.62	0.25	2.05
inches	0.185	0.015	0.155	0.064 0.045	0.022 0.017	0.014 0.010	1.256 1.240	0.265 0.255	0.100	0.300	0.138 0.120	0.32 0.30	0.395 0.300	0.01	0.081

Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT222-1		MS-001AF				95-03-11

SO24: plastic small outline package; 24 leads; body width 7.5 mm SOT137-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

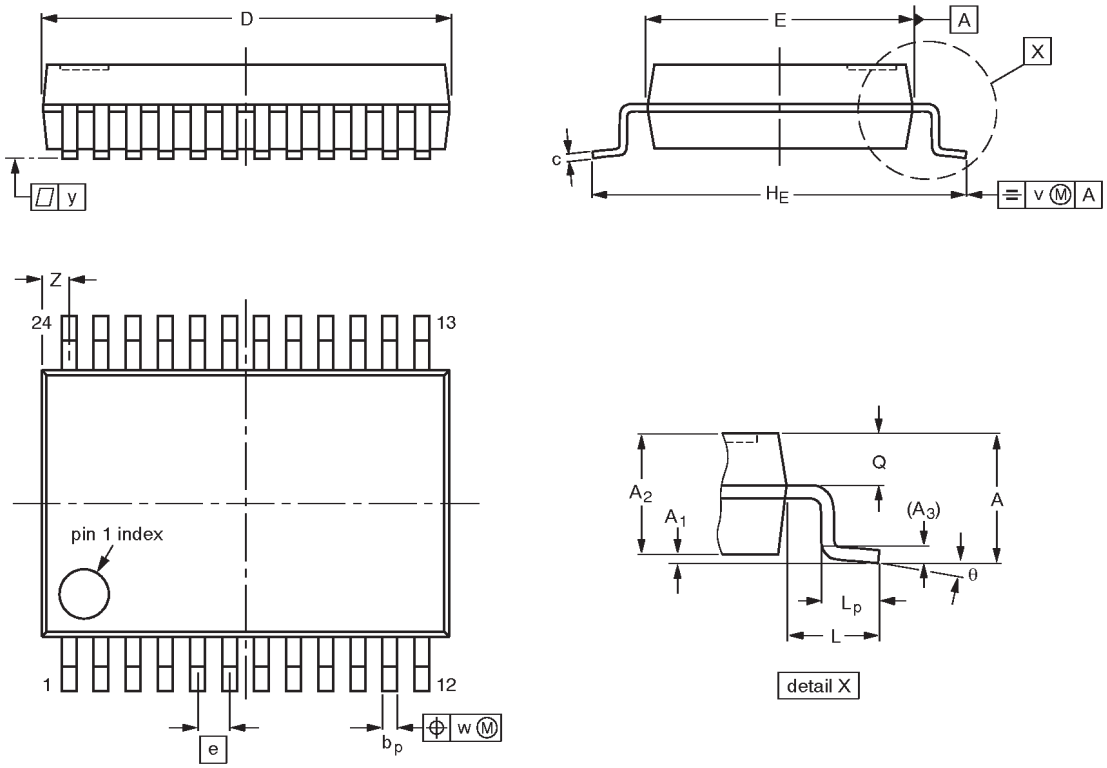
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT137-1	075E05	MS-013AD				~~95-01-24~~ 97-05-22

SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm **SOT340-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	8.4 8.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.8 0.4	8° 0°

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT340-1		MO-150AG				~~93-09-08~~ 95-02-04

NOTES

DEFINITIONS

Data Sheet Identification	Product Status	Definition
Objective Specification	Formative or in Design	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	Preproduction Product	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	Full Production	This data sheet contains Final Specifications. Philips Semiconductors reserves the right to make changes at any time without notice, in order to improve design and supply the best possible product.

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