

Compatible with Eu Directive
2002/EC - RoHS

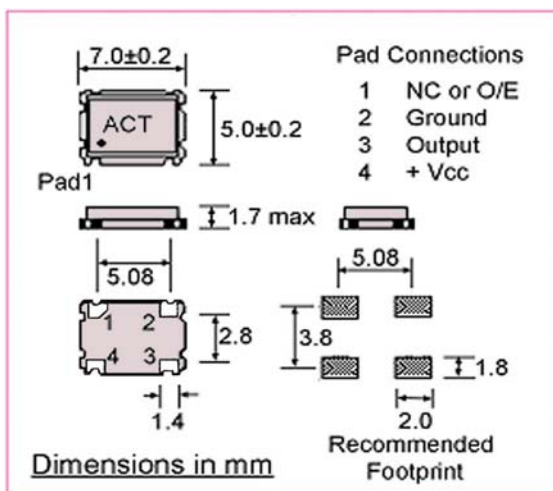
ACT9200

The ACT9200 family is a miniature, low profile SMD package, with a ceramic base utilising a seam welded metal lid for high reliability and better long-term stability. The metal lid is grounded through the package to assist with EMI emission reductions. This 7x5mm device is available as the ACT9200 in both 3V3 and 5V0. 1V8 and 2V5 versions are available as ACT9200L (See ACT9200L data sheet). A 32.768kHz version is available as the 9200WC (See 9200WC data sheet). Taped and reeled packaging (1k reels) and loose quantities are available for purchase, to suit high and low volume production.



Specification

Parameter	Symb.	Specification		Condition
Supply Voltage	V _{dd}	3.3V _{DC} ± 10%	5.0V _{DC} ± 10%	Please specify
Frequency Range	f _o	1.000 ~ 200.00 MHz	1.000 ~ 106.25 MHz	Please specify
Frequency Stability	Δf/f _o	±15ppm ~ ±100ppm		Please specify
Temp Operating Range	T _{opr}	0 ~ +70°C standard to -40 ~ +85°C		Please specify
Temp Storage Range	T _{stg}	-55 to +125°C		
Supply Current (max)	I _{op}	16mA (1.000 ~ 34.999 MHz)	25mA (1.0000 ~ 34.999 MHz)	
		25mA (35.000 ~ 60.00 MHz)	40mA (35.00 ~ 60.00 MHz)	
		40mA (60.001 ~ 99.999 MHz)	60mA (60.001 ~ 99.999 MHz)	
		50mA (100.00 ~ 155.00 MHz)	80mA (100.00 ~ 106.25 MHz)	
		60mA (155.01 ~ 200.00 MHz)		
Duty Cycle	T _{w/t}	40/60% (Std) & 45/55% available		Please specify
Output Level '0'	V _{OL}	0.4V _{DC} max (TTL)	10% V _{DD} max (HCMOS)	
Output Level '1'	V _{OH}	2.4V _{DC} min (TTL)	90% V _{DD} min (HCMOS)	
Rise & Fall Time (max)	T _{rTf}	10nS (1.000 ~ 34.999 MHz)	10nS (1.00 ~ 49.999 MHz)	
		5nS (35.00 ~ 99.999 MHz)	5nS (50.00MHz ~ 99.90 MHz)	
		2.5nS (100.00 ~ 200.00 MHz)	3nS (100.00 ~ 106.25 MHz)	
Output Load	N/CL	10TTL / 15pF (30pF available)		
Start-up Time	T _{osc}	10mS max		
Tri-state Input Voltage	No Connection	Enable output		
	V _{IH} : ≥90% of V _{DD}	Enable output		
	V _{IL} : ≤10% of V _{DD}	Disable output : High Impedance		
Ageing	F _a	±5ppm ±3ppm option	first year max @25°C	
Period Jitter (Absolute)	T _j	100pS max @ 1.0MHz	Other frequencies - see Note 2 below	
Period Jitter (one sigma)	T _j	25pS max @ 1.0MHz	Other frequencies - see Note 2 below	



Pad surface Material
Au

APPLICATIONS

- Microprocessor clock
- PDA / notebook
- Wireless applications
- Audio
- Gigabit ethernet
- Fibre channel
- Instrumentation

NOTE 1: To reduce HF power supply noise, an external bypass capacitor of 0.01μF close to ground and V_{dd} is recommended.

NOTE 2: Typical (max) Jitter values in pS:

	RMS(1 sigma)	Absolute (PK-PK)
25MHz:	6.3 (10)	17.8 (28)
33MHz:	5.2 (10)	14.7 (28)
60MHz:	3.7 (5.0)	10.5 (14.0)
100MHz	1.0 (3.0)	2.8 (8.4)

Please note that all parameters can not necessarily be specified in the same device

Customer to Specify : Frequency, Frequency Stability, Operating Temperature Range, Output Type, Output enable, Voltage, Duty Cycle

In line with our ongoing policy of product evolution and improvement, the above specification is subject to change without notice

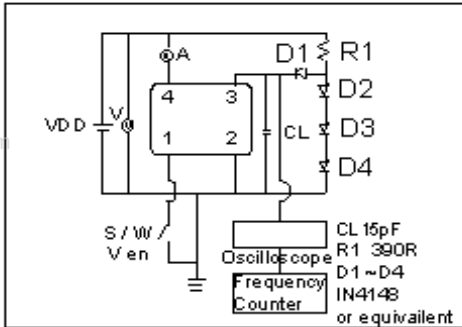
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For quotations or further information please contact us at:
 3 The Business Centre, Molly Millars Lane, Wokingham, Berks, RG41 2EY, UK
<http://www.actcrystals.com>

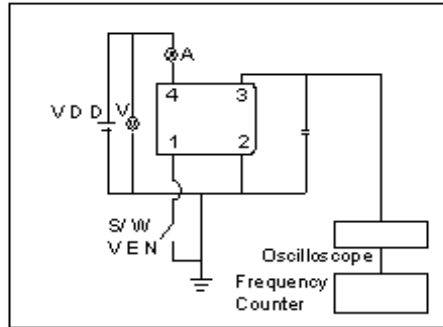
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ACT9200 CIRCUIT DRAWINGS

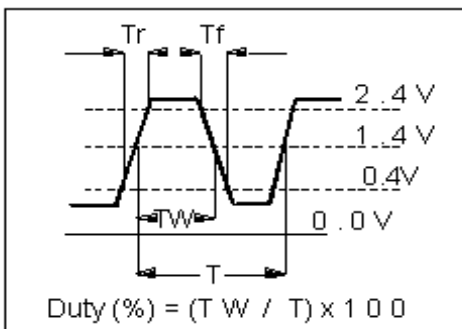
TTL Test Circuit



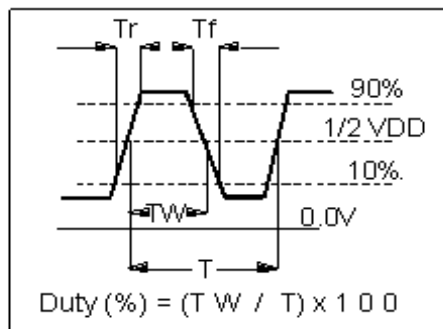
CMOS Test Circuit



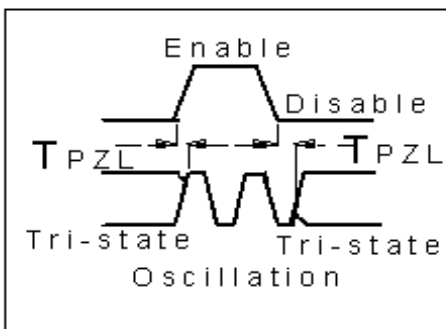
TTL Waveform



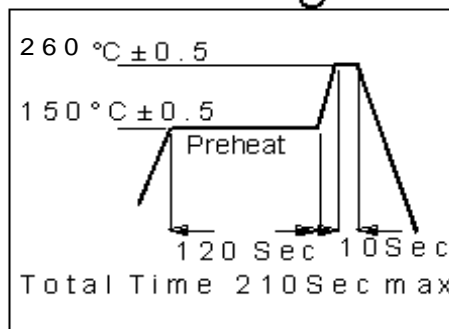
CMOS Waveform



Tristate Function



Reflow Diagram



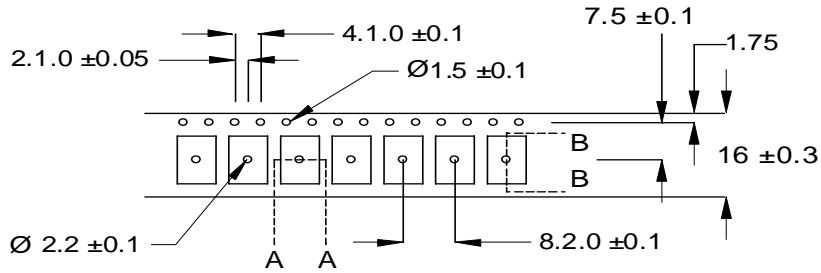
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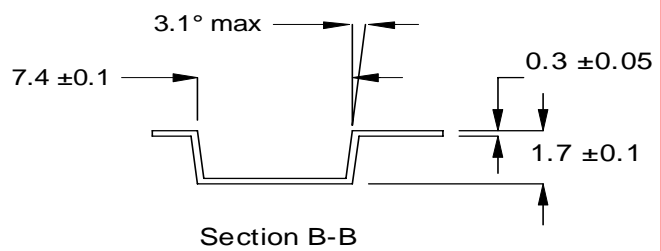
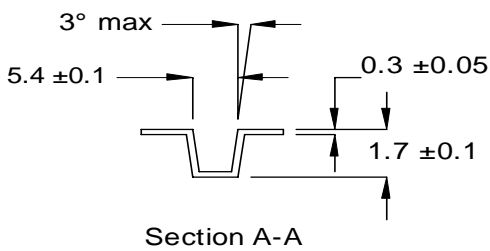
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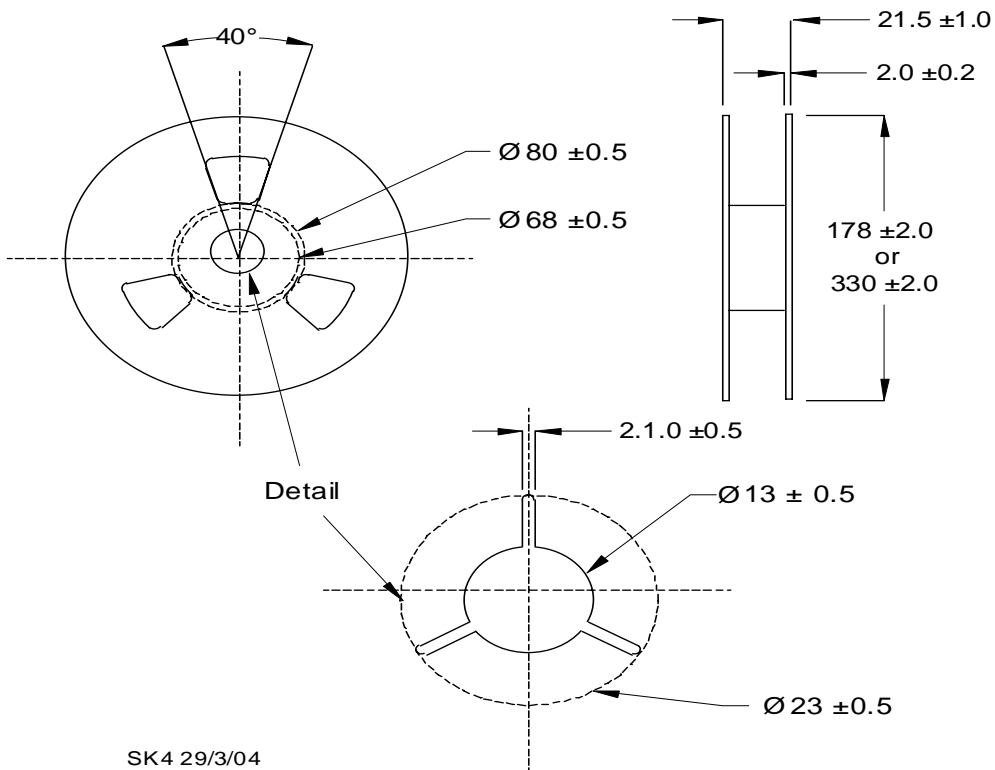
ACT9200 TAPE & REEL SPECIFICATIONS (1K Reels)



www.DataSheet4U.com



Dimensions in mm



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