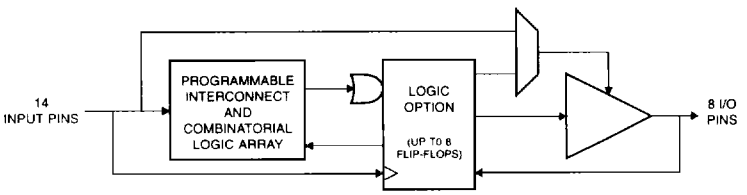
Features

- Edge-Controlled Power Down Pin
- Zero Power Equivalent of ATF20V8B
- Edge-Sensing Zero Standby Power (10 µA Typical)
- Industry Standard Architecture
  - Emulates Many 24-Pin PALs®
  - Low Cost Easy-to-Use Software Tools
- High Speed Electrically Erasable Programmable Logic Devices
  - 10 ns Maximum Pin-to-Pin Delay
- CMOS and TTL Compatible Inputs and Outputs
  - Latch Feature Hold Outputs to Previous Logic States
- Advanced Flash Technology
  - Reprogrammable
  - 100% Tested
- High Reliability CMOS Process
  - 20 Year Data Retention
  - 100 Erase/Write Cycles
  - 2,000 V ESD Protection
  - 200 mA Latchup Immunity
- Commercial, and Industrial Temperature Ranges
- Dual-in-Line and Surface Mount Packages in Standard Pinouts

High Performance Flash PLD

Advance Information

Block Diagram



Description

The ATF20V8CZ is a high performance CMOS (Electrically Erasable) Programmable Logic Device (PLD) which utilize Atmel's proven electrically erasable Flash memory technology. Speeds down to 10 ns and power dissipation as low as 10 µA are offered. All speed ranges are specified over the full 5 V ± 10% range for industrial temperature ranges, and 5 V ± 5% range for commercial ranges.

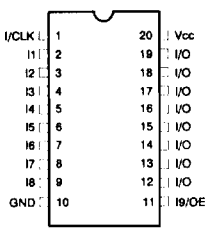
The ATF20V8CZ provides the zero power CMOS PLD solution, with "zero" standby power (10 µA typical). The ATF20V8CZ powers down automatically though Atmel's patented Input

(continued)

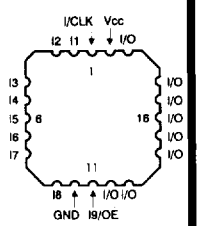
Pin Configurations

Pin Name	Function
CLK	Clock
IN	Logic Inputs
I/O	Bidirectional Buffers
$\overline{OE}$	Output Enable
•	No Internal Connection
VCC	+5 V Supply

DIP



PLCC



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Description (Continued)

Transition Detection (ITD) circuitry to the "zero" standby power mode when all inputs are idle. Pin "keeper" circuits on input and output pins reduce static power consumed by pull-ups.

The ATF20V8CZ incorporates a superset of the generic architectures, which allows direct replacement of the 20R8 family and most 24-pin combinatorial PLDs. Eight outputs are each allocated eight product terms. Three different modes of operation, configured automatically with software, allowing highly complex logic functions to be realized.

D.C. and A.C. Operating Conditions

	Commercial	Industrial
Operating Temperature (Case)	0°C - 70°C	-40°C - 85°C
V_{CC} Power Supply	5 V ± 5%	5 V ± 10%

Functional Description

The ATF20V8CZ macrocell can be configured in one of three different modes. Each mode makes the ATF20V8CZ look like a different device. The ATF20V8CZ can be a registered output, combinatorial I/O, combinatorial output, or dedicated input. Most PLD compilers can choose the right mode automatically. The user can also force the selection by supplying the compiler with a mode selection. The determining factors would be the usage of register versus combinatorial outputs and dedicated outputs versus output with output enable control.

The ATF20V8CZ powers down automatically through the ITD circuitry down to a "zero" standby power (10 µA typical) when all inputs are idle. This feature allows the user flexibility to reduce total system power, enhance reliability all without sacrificing speed. Static power loss due to pull-up resistors is reduced through input and output pin "keeper" circuits which holds pins to their previous logic levels when idle.

The universal architecture of the ATF20V8CZ can be programmed to emulate many 24-pin PAL devices. The user can download the subset device JEDEC programming file to the PLD programmer, and the ATF20V8CZ can be configured to act like the chosen device.

Unused product terms are automatically disabled by the compiler to further decrease power consumption. A Security Fuse, when programmed, protects the contents the ATF20V8CZ. Eight bytes (64 fuses) of User Signature are accessible to the user for purposes such as storing project name, part number, revision or date. The User Signature is accessible regardless of the state of the Security Fuse.

Compiler Mode Selection

	Registered	Complex	Simple	Auto Select
ABEL, Atmel-ABEL	P20V8R	P20V8C	P20V8AS	P20V8
CUPL	G20V8MS	G20V8MA	G20V8AS	G20V8
LOG/iC	GAL20V8_R [1]	GAL20V8_C7 [1]	GAL20V8_C8 [1]	GAL20V8
OrCAD-PLD	"Registered"	"Complex"	"Simple"	GAL20V8A
PLDesigner	P20V8R	P20V8C	P20V8C	P20V8A
Tango-PLD	G20V8R	G20V8C	G20V8AS	G20V8

Note: 1. Only applicable for version 3.4 or lower.