# Triacs high noise immunity

# BT139X series H

## GENERAL DESCRIPTION

Glass passivated triacs in a full pack, plastic envelope, intended for use in applications requiring high noise immunity in addition to high, bidirectional blocking voltage capability and thermal cycling performance. Typical applications include motor control, industrial lighting, heating and static switching.

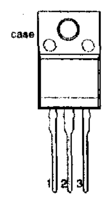
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | MAX. | MAX. | UNIT |
|---|---|---|---|---|---|
| | BT139X- | 500H | 600H | 800H | |
| $V_{DRM}$ | Repetitive peak off-state voltages | 500 | 600 | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | 16 | 16 | 16 | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | 140 | 140 | 140 | A |

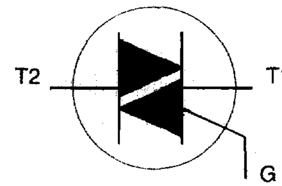
## PINNING - SOT186A

| PIN | DESCRIPTION |
|---|---|
| 1 | main terminal 1 |
| 2 | main terminal 2 |
| 3 | gate |
| case | isolated |

## PIN CONFIGURATION




## SYMBOL




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | -500 | -600 | -800 | |
| $V_{DRM}$ | Repetitive peak off-state voltages | | - | 500[1] | 600[1] | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{hs} \leq 38$ ˚C | - | 16 | | | A |
| $I_{TSM}$ | Non-repetitive peak on-state current | full sine wave; $T_j = 25$ ˚C prior to surge | | | | | |
| | | t = 20 ms | - | 140 | | | A |
| | | t = 16.7 ms | - | 150 | | | A |
| $I^2t$ | $I^2t$ for fusing | t = 10 ms | - | 98 | | | $A^2s$ |
| $dI_T/dt$ | Repetitive rate of rise of on-state current after triggering | $I_{TM} = 20$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs | | | | | |
| | | T2+ G+ | - | 50 | | | A/µs |
| | | T2+ G- | - | 50 | | | A/µs |
| | | T2- G- | - | 50 | | | A/µs |
| | | T2- G+ | - | 10 | | | A/µs |
| $I_{GM}$ | Peak gate current | | - | 2 | | | A |
| $V_{GM}$ | Peak gate voltage | | - | 5 | | | V |
| $P_{GM}$ | Peak gate power | | - | 5 | | | W |
| $P_{G(AV)}$ | Average gate power | over any 20 ms period | - | 0.5 | | | W |
| $T_{stg}$ | Storage temperature | | -40 | 150 | | | ˚C |
| $T_j$ | Operating junction temperature | | - | 125 | | | ˚C |

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

## ISOLATION LIMITING VALUE & CHARACTERISTIC

$T_{hs}$ = 25 ˚C unless otherwise specified

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $V_{isol}$ | R.M.S. isolation voltage from all three terminals to external heatsink | f = 50-60 Hz; sinusoidal waveform; R.H. ≤ 65% ; clean and dustfree | - | | 2500 | V |
| $C_{isol}$ | Capacitance from T2 to external heatsink | f = 1 MHz | - | 10 | - | pF |

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $R_{th\ j-hs}$ | Thermal resistance junction to heatsink | full or half cycle<br>with heatsink compound<br>without heatsink compound | -<br>- | -<br>- | 4.0<br>5.5 | K/W<br>K/W |
| $R_{th\ j-a}$ | Thermal resistance junction to ambient | in free air | - | 55 | - | K/W |

## STATIC CHARACTERISTICS

$T_j$ = 25 ˚C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $I_{GT}$ | Gate trigger current | $V_D$ = 12 V; $I_T$ = 0.1 A | | | | |
| | | T2+ G+ | 10 | 14 | 50 | mA |
| | | T2+ G- | 10 | 17 | 50 | mA |
| | | T2- G- | 10 | 18 | 50 | mA |
| | | T2- G+ | 10 | 40 | 100 | mA |
| $I_L$ | Latching current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | | | | |
| | | T2+ G+ | - | 10 | 60 | mA |
| | | T2+ G- | - | 25 | 90 | mA |
| | | T2- G- | - | 12 | 60 | mA |
| | | T2- G+ | - | 14 | 90 | mA |
| $I_H$ | Holding current | $V_D$ = 12 V; $I_{GT}$ = 0.1 A | - | 8 | 60 | mA |
| $V_T$ | On-state voltage | $I_T$ = 20 A | - | 1.2 | 1.6 | V |
| $V_{GT}$ | Gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A | - | 0.7 | 1.5 | V |
| | | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 125 ˚C | 0.25 | 0.4 | - | V |
| $I_D$ | Off-state leakage current | $V_D$ = $V_{DRM(max)}$; $T_j$ = 125 ˚C | - | 0.1 | 0.5 | mA |

## DYNAMIC CHARACTERISTICS

$T_j$ = 25 ˚C unless otherwise stated

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $dV_D/dt$ | Critical rate of rise of off-state voltage | $V_{DM}$ = 67% $V_{DRM(max)}$; $T_j$ = 125 ˚C; exponential waveform; gate open circuit | 200 | 500 | - | V/µs |
| $dV_{com}/dt$ | Critical rate of change of commutating voltage | $V_{DM}$ = 400 V; $T_j$ = 95 ˚C; $I_{T(RMS)}$ = 16 A; $dI_{com}/dt$ = 7.2 A/ms; gate open circuit | 10 | 20 | - | V/µs |
| $t_{gt}$ | Gate controlled turn-on time | $I_{TM}$ = 20 A; $V_D$ = $V_{DRM(max)}$; $I_G$ = 0.1 A; $dI_G/dt$ = 5 A/µs | - | 2 | - | µs |

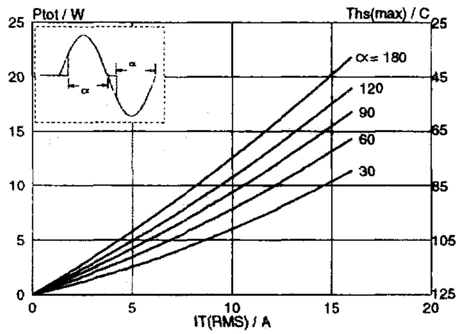



*Fig.1. Maximum on-state dissipation, $P_{tot}$, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.*

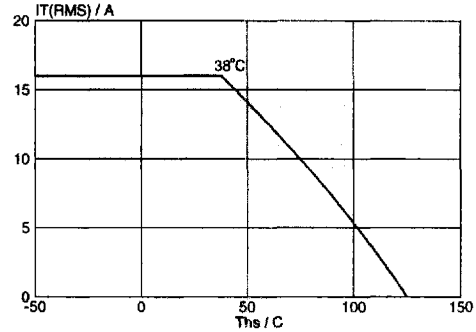



*Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus heatsink temperature $T_{hs}$.*

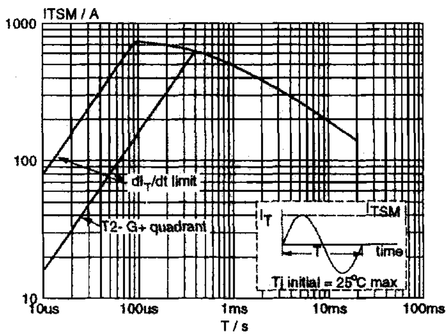



*Fig.2. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus pulse width $t_p$, for sinusoidal currents, $t_p \leq 20ms$.*

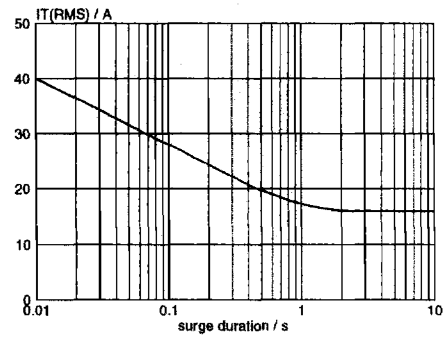



*Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{hs} \leq 38°C$.*

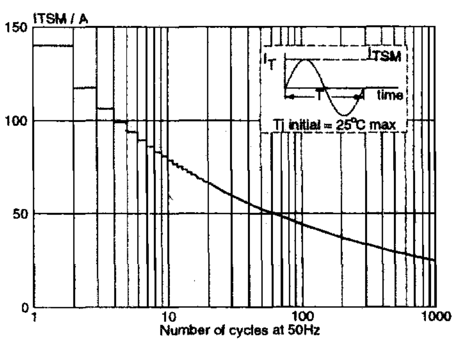



*Fig.3. Maximum permissible non-repetitive peak on-state current $I_{TSM}$, versus number of cycles, for sinusoidal currents, f = 50 Hz.*

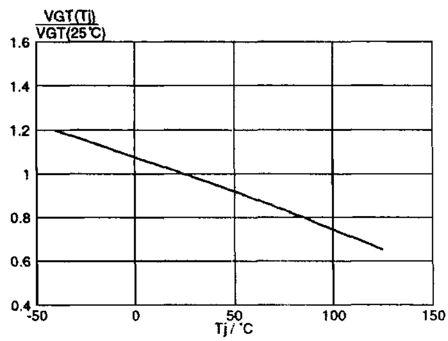



*Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/V_{GT}(25°C)$, versus junction temperature $T_j$.*

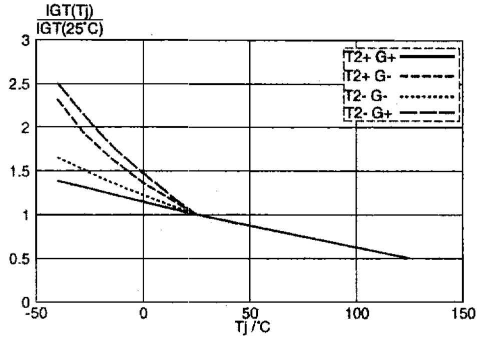



*Fig.7. Normalised gate trigger current $I_{GT}(T_j)/I_{GT}(25˚C)$, versus junction temperature $T_j$.*

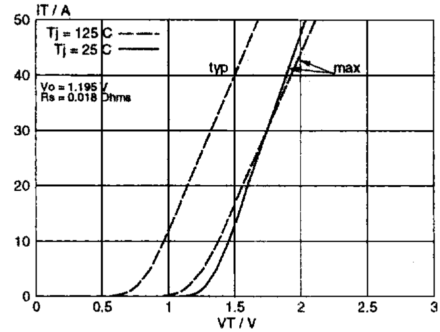



*Fig.10. Typical and maximum on-state characteristic.*

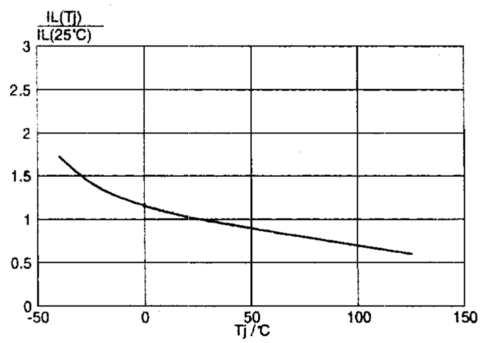



*Fig.8. Normalised latching current $I_L(T_j)/I_L(25˚C)$, versus junction temperature $T_j$.*

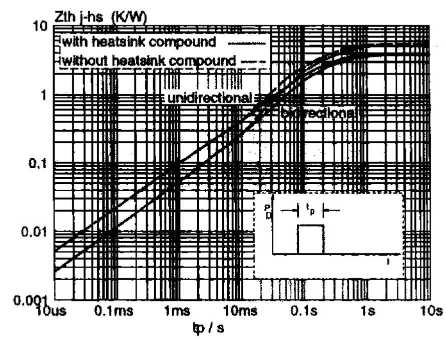



*Fig.11. Transient thermal impedance $Z_{th\,j\text{-}hs}$, versus pulse width $t_p$.*

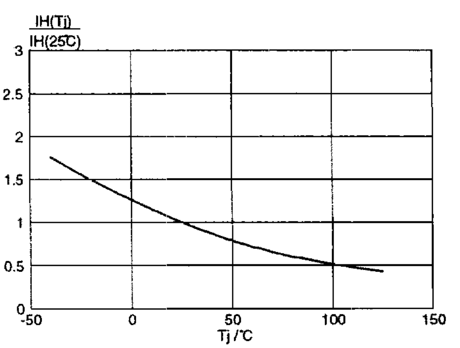



*Fig.9. Normalised holding current $I_H(T_j)/I_H(25˚C)$, versus junction temperature $T_j$.*

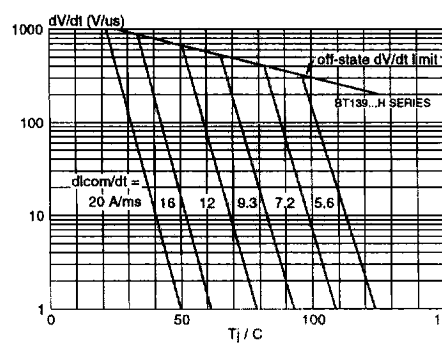



*Fig.12. Typical commutation dV/dt versus junction temperature, parameter commutation $dI_T/dt$. The triac should commutate when the dV/dt is below the value on the appropriate curve for pre-commutation $dI_T/dt$.*