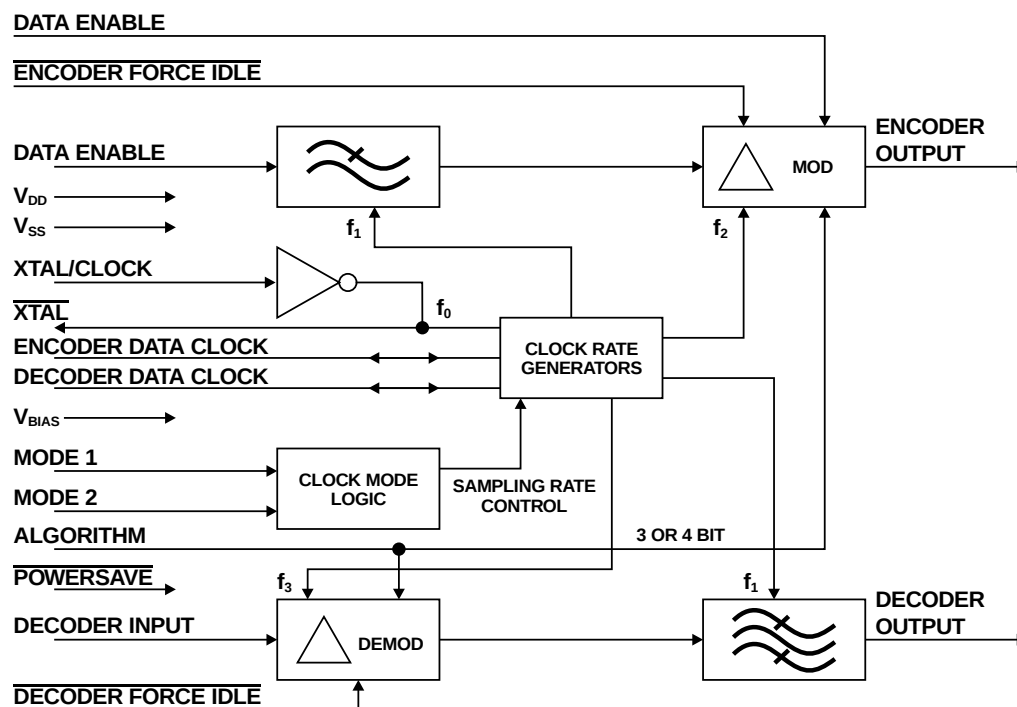


Features

- Meets EUROCOM D1-IA8
- Single Chip Full Duplex CVSD CODEC
- On-chip Input and Output Filters
- Programmable Sampling Clocks
- 3- or 4-bit Companding Algorithm
- Powersave Capabilities
- Low Power, 3.0V - 5.0V Operation

Applications

- Military Communications
- Multiplexers, Switches, & Phones



The CMX619A is a Continuously Variable Slope Delta Modulation (CVSD) Codec designed for use in military communications systems. This device is suitable for applications in military delta multiplexers, switches, and phones. The CMX619A is designed to meet EUROCOM D1-IA8 specifications.

Encoder input and decoder output filters are incorporated on-chip. Sampling clock rates can be programmed to 16, 32, or 64kbps from an internal clock generator or externally injected in the 8 to 64kbps range. The sampling clock frequency is output for the synchronization of external circuits.

The encoder has an enable function for use in multiplexer applications. Encoder and Decoder forced idle capabilities are provided forcing 10101010... pattern in encode and a $V_{DD}/2$ bias in decode. The companding circuit may be operated with an externally selectable 3- or 4-bit algorithm. The device may be placed in standby mode by selecting Powersave. A reference 1.024MHz oscillator uses an external clock or crystal.

The CMX619A operates using a supply voltage from 3.0V to 5.0V and is available in the following packages: 24-pin TSSOP (CMX619AE2), 24-pin PLCC (CMX619AL2), 22-pin Cerdip (CMX619AJ3), and 22-pin PDIP (CMX619AP6).

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MX-COM, Inc. reserves the right to change specifications at any time and without notice.
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1 Block Diagram

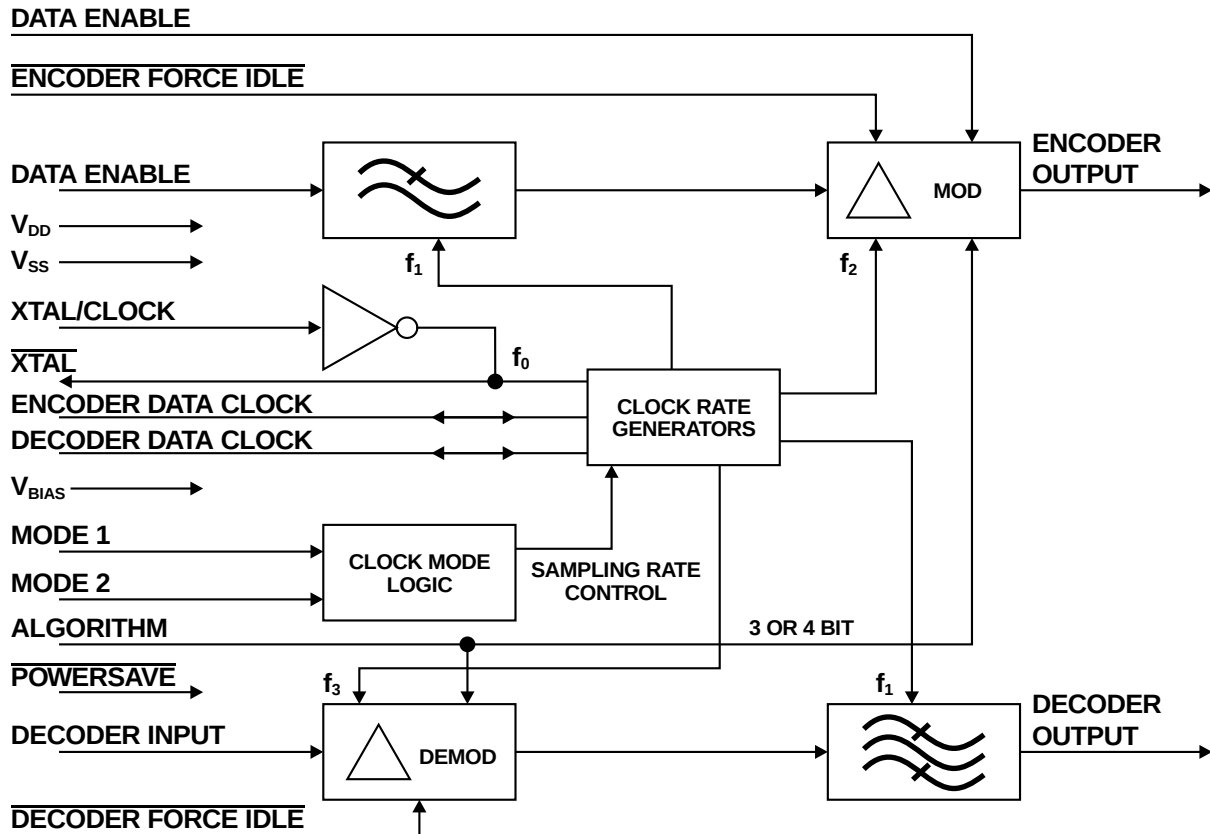


Figure 1: Block Diagram

2 Signal List

J3/P6	E2/L2	Name	Signal	Description
1	1	Xtal/Clock	input	Input to the clock oscillator inverter. A 1.024MHz Xtal input or externally derived clock is injected here. See Clock Mode pins and Figure 2.
	2	N/C		No Connection
2	3	$\overline{\text{Xtal}}$	output	The 1.024 MHz output of the clock oscillator inverter.
3	4	N/C		No Connection
4	5	Encoder Data Clock	input/output	A logic I/O port. External encode clock input or internal data clock output. Clock frequency is dependent upon Clock Mode 1, 2 inputs and Xtal frequency (see Clock Mode pins).
5	6	Encoder Output	output	The encoder digital output. This is a three-state output whose condition is set by the Data Enable and Powersave inputs. See Table 2.
6	7	$\overline{\text{Encoder Force Idle}}$		When this pin is at a logical "0" the encoder is forced to an idle state and the encoder digital output is 0101, a perfect idle pattern. When this pin is a logical "1" the encoder encodes as normal. Internal 1M Ω pull-up.
7	8	Data Enable	input	Data is made available at the encoder output pin by control of this input. See Encoder Output pin. Internal 1 M Ω pull-up.
8	9	N/C		No Connection
9	10	V _{BIAS}		Normally at V _{DD} /2 bias, this pin should be externally decoupled by capacitor C4. Internally pulled to V _{SS} when "Powersave" is a logical "0".
10	11	Encoder Input	input	The analog signal input. Internally biased at V _{DD} /2, this input requires an external coupling capacitor. The source impedance should be less than 100 Ω . Output channel noise levels will improve with an even lower source impedance. See Figure 2.
11	12	V _{SS}	power	Negative Supply
12	13	N/C		No Connection
13	14	Decoder Output	output	The recovered analog signal is output at this pin. It is the buffered output of a lowpass filter and requires external components. During "Powersave" this output is open circuit.
14	15	N/C		No Connection
15	16	$\overline{\text{Powersave}}$		A logic "0" at this pin puts most parts of the codec into a quiescent non-operational state. When at a logical "1", the codec operates normally. Internal 1 M Ω pull-up.
	17	N/C		No Connection
16	18	$\overline{\text{Decoder Force Idle}}$		A logic "0" at this pin gates a 0101... pattern internally to the decoder so that the Decoder Output goes to V _{DD} /2. When this pin is a logical "1" the decoder operates as normal. Internal 1M Ω pull-up.
17	19	Decoder Input		The received digital signal input. Internal 1 M Ω pull-up.
18	20	Decoder Data Clock	input/output	A logic I/O port. External decode clock input or internal data clock output, dependent upon clock mode 1,2 inputs. See Clock Mode pins.
19	21	Algorithm		A logic "1" at this pin sets this device for a 3-bit companding algorithm. A logical "0" sets a 4-bit companding algorithm. Internal 1 M Ω pull-up.

J3/P6	E2/L2	Name	Signal	Description
20	22	Clock Mode 2		Clock rates refer to $f = 1.024\text{MHz}$ Xtal/Clock input. During internal operation the data clock frequencies are available at the ports for external circuit synchronization. Independent or common data rate inputs to Encode and Decode data clock ports may be employed in the External Clocks mode. Internal $1\text{M}\Omega$ pull-ups. See Table 3.
21	23	Clock Mode 1		
22	24	V_{DD}	power	Positive Supply. A single 3.0V - 5.0V supply is required.

Table 1: Signal List

Data Enable	Powersave	Encoder Output
1	1	Enable
0	1	High Z (open circuit)
1	0	V_{SS}

Table 2: Encoder Output

Clock Mode 1	Clock Mode 2	Facility
0	0	External Clocks
0	1	Internal, 64kbps = $f/16$
1	0	Internal, 32kbps = $f/32$
1	1	Internal, 16kbps = $f/64$

Table 3: Clock Mode

3 External Components

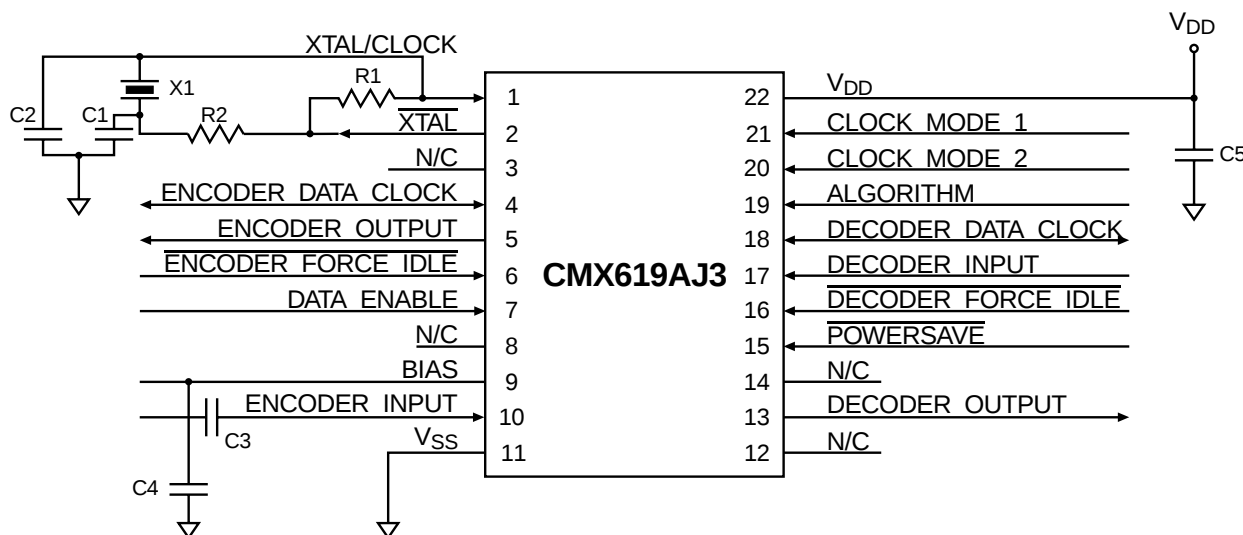


Figure 2: Recommended External Components for Typical Application

R1	Note 1	1M Ω	$\pm 10\%$
R2	Note 2	Selectable	
C1	Note 3	33pF	$\pm 20\%$
C2	Note 3	68pF	$\pm 20\%$

C3	Note 4	1.0 μ F	$\pm 20\%$
C4	Note 5	1.0 μ F	$\pm 20\%$
C5	Note 6	1.0 μ F	$\pm 20\%$
X1	Note 7, 8	1.024MHz	

Table 4: Recommended External Components for Typical Application

Notes:

- Oscillator inverter bias resistor.
- Xtal Drive limiting resistor.
- Xtal circuit load capacitor.
- Encoder input coupling capacitor. The drive source impedance to this input should be less than 100 Ω . Output idle channel noise levels will improve with even lower source impedance.
- Bias decoupling capacitor
- V_{DD} decoupling capacitor
- A 1.024MHz Xtal/Clock input will yield exactly 16/32/64kbps data clock rates. Xtal circuitry shown is in accordance with MX-COM's Xtal Oscillator Application Note.
- For best results, a crystal oscillator design should drive the clock inverter input with signal levels of at least 40% of V_{DD}, peak to peak. Tuning fork crystals generally cannot meet this requirement. To obtain crystal oscillator design assistance, please consult your crystal manufacturer.

4 General Description

The CMX619A is a Continuously Variable Slope Delta Modulation (CVSD) Codec designed for use in military communications systems. This device is suitable for applications in military delta multiplexers, switches and phones. The CMX619A is designed to meet EUROCOM D1-IA8 specifications.

Encoder input and decoder output filters are incorporated on-chip. Sampling clock rates can be programmed to 16, 32, or 64kbps from an internal clock generator or externally injected in the 8 to 64kbps range. The sampling clock frequency is output for the synchronization of external circuits.

The encoder has an enable function for use in multiplexer applications. Encoder and Decoder forced idle capabilities are provided forcing 10101010... pattern in encode and a V_{DD}/2 bias in decode. The companding circuit may be operated with an externally selectable 3- or 4-bit algorithm. The device may be placed in standby mode by selecting Powersave. A reference 1.024MHz oscillator uses an external clock or crystal.

5 Application

Due to the very low levels of signal specified for idle channel noise in military applications, a noisy or badly regulated power supply could cause instability, putting the overall system performance out of specification. Adherence to the points listed below will assist in minimizing this problem.

1. Care should be taken in the design and layout of the printed circuit board.
2. All external components (as recommended in Figure 2) should be kept close to the package.
3. Tracks should be kept short, particularly the Encoder Input capacitor and the V_{BIAS} capacitor.
4. Xtal/Clock tracks should be kept well away from analog inputs and outputs.
5. Inputs and outputs should be screened whenever possible.
6. A 'ground plane' connected to V_{SS} will assist in eliminating external pick-up on the input and output pins.
7. It is recommended that the power supply rails have less than $1mV_{RMS}$ of noise allowed.
8. The source impedance to the Encoder Input pin must be less than 100Ω ; output idle channel, noise levels will improve with even lower source impedance.

5.1 CODEC Integration

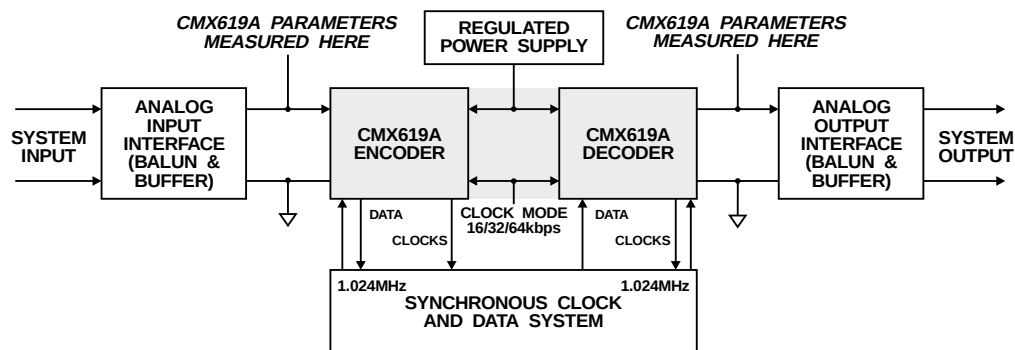


Figure 3: System Configuration using the CMX619A

5.2 Digital to Analog Performance

Test	Sample Rate	Bit Sequence at Decoder Input	MLA Duty Cycle	$V_{DD} = 5.0V$ Output Level (dBmO)	$V_{DD} = 3.0V$ Output Level (dBmO)
a	16kbps	1011 0100 1001 0010 1101 (\$B492D)	0	-41.5dBmO	-46.0dBmO
	32kbps	1011 0110 1010 1001 0010 0100 1001 0101 0110 1101 (\$B6A924956D)	0	-42.0dBmO	-46.5dBmO
b	16kbps	1101 1001 0010 0100 1101 (\$D924D)	0.05	-25.0dBmO	-29.4dBmO
	32kbps	1011 0110 1010 1001 0010 0010 0100 1010 1101 1011 (\$B6A9224ADB)	0.05	-25.0dBmO	-29.4dBmO
c	16kbps	1011 0101 0001 0010 1011 (\$B512B)	0.1	-19.0dBmO	-23.4dBmO
	32kbps	1101 1011 0101 0010 0010 0010 0100 1010 1101 1101 (\$DB52224ADD)	0.1	-18.5dBmO	-23.0dBmO
d	16kbps	1101 1001 0000 1001 1011 (\$D909B)	0.2	-11.0dBmO	-15.4dBmO
	32kbps	1101 1101 1001 0100 0100 0010 0010 0110 1011 1011 (\$DD944226BB)	0.2	-11.5dBmO	-16.0dBmO
e	16kbps	1101 1010 0000 1001 0111 (\$DA097)	0.3	-6.5dBmO	-11.0dBmO
	32kbps	1110 1110 1100 1000 1000 0001 0001 0011 0111 0111 (\$EEC8811377)	0.3	-6.5dBmO	-11.0dBmO
f	16kbps	1101 1010 0000 0100 1111 (\$DA04F)	0.4	-3.0dBmO	-7.5dBmO
	32kbps	1111 0111 0101 0001 0000 0000 1000 1010 1110 1111 (\$F751008AEF)	0.4	-3.0dBmO	-7.5dBmO
g	16kbps	1110 1010 0000 0010 1111 (\$EA02F)	0.5	0dBmO	-4.4dBmO
	32kbps	1111 1011 1010 0010 0000 0000 0100 0101 1101 1111 (\$FBA20045DF)	0.5	0dBmO	-4.4dBmO

Table 5: Bit Sequence Test

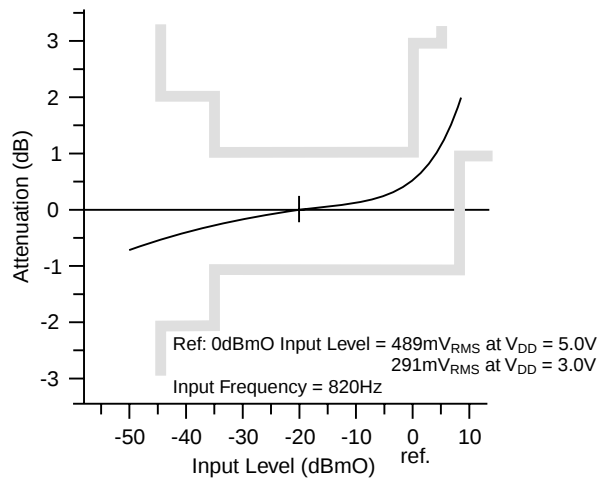


Figure 4: Gain vs. Input Level (16kbps)

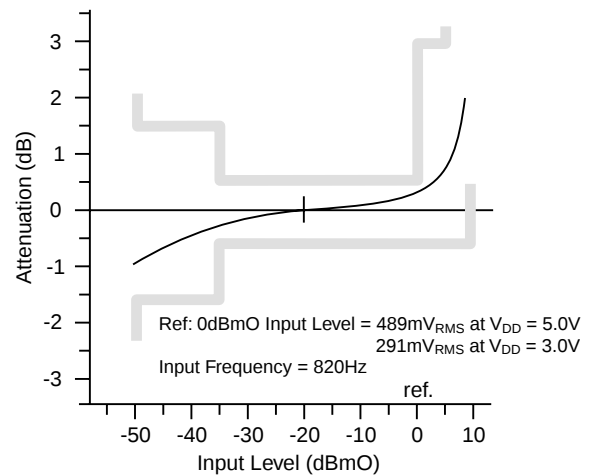


Figure 5: Gain vs. Input Level (32kbps)

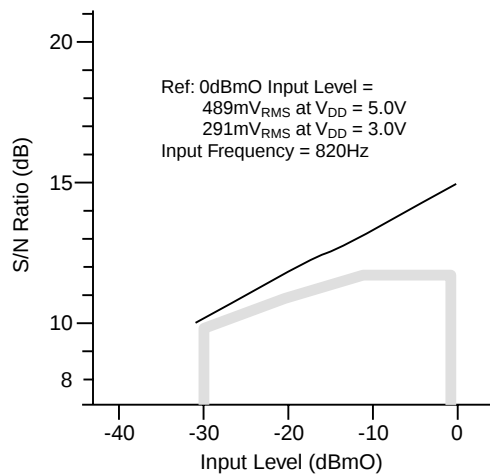


Figure 6: S/N vs. Input Level (16kbps)

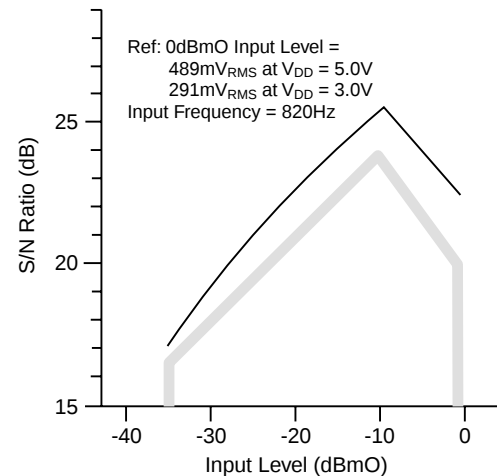


Figure 7: S/N vs. Input Level (32kbps)

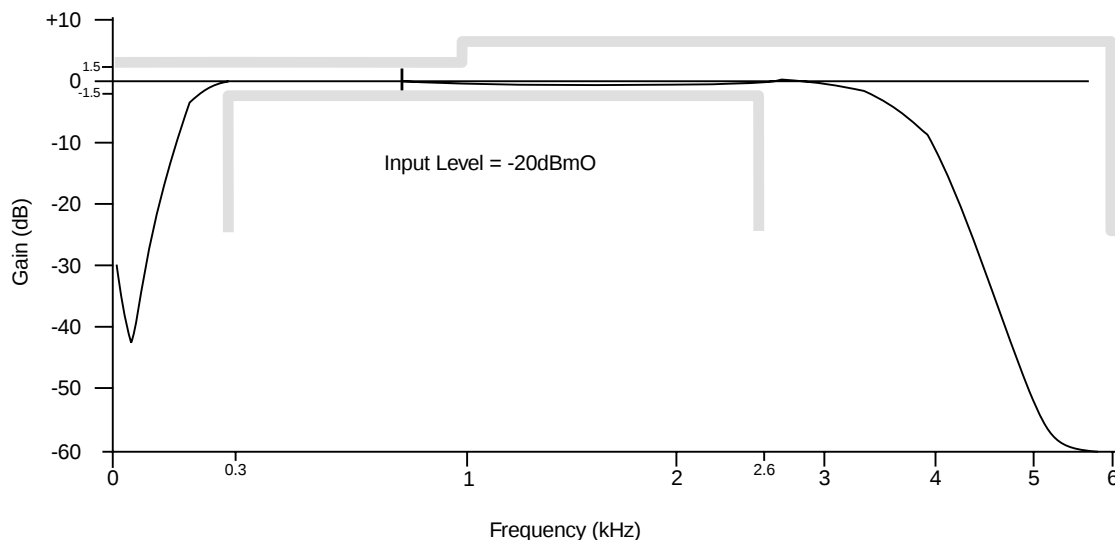


Figure 8: Attenuation Distortion vs. Frequency (16kbps)

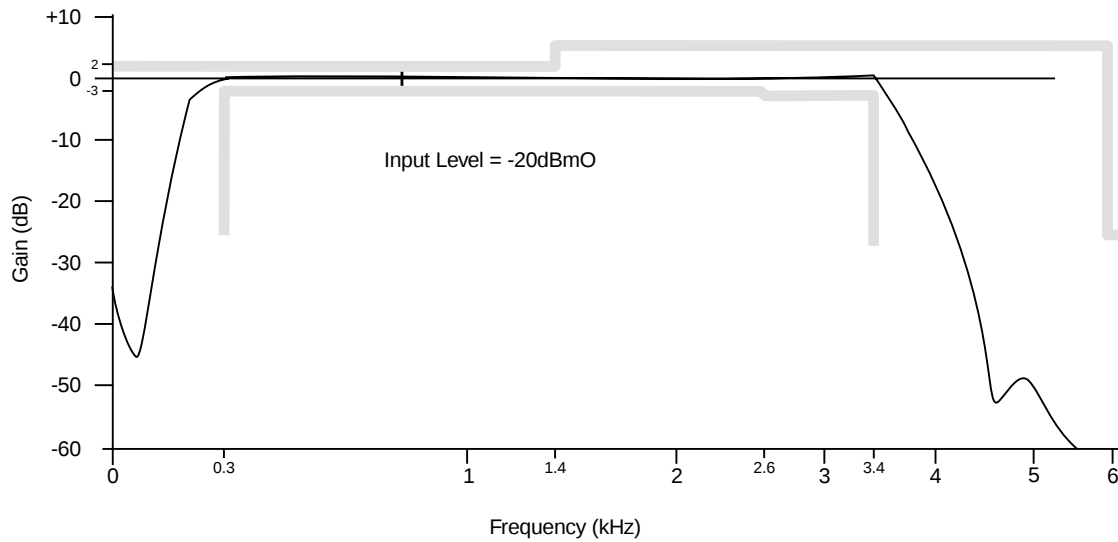


Figure 9: Attenuation Distortion vs. Frequency (32kbps)

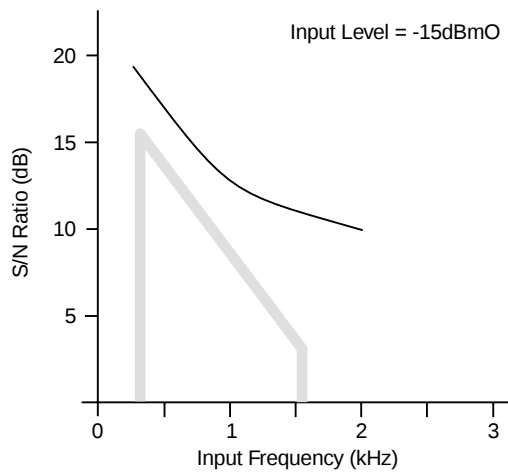


Figure 10: S/N vs. Input Frequency (16kbps)

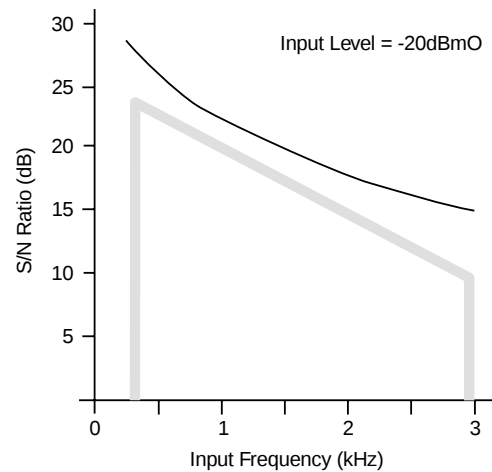


Figure 11: S/N vs. Input Frequency (32kbps)

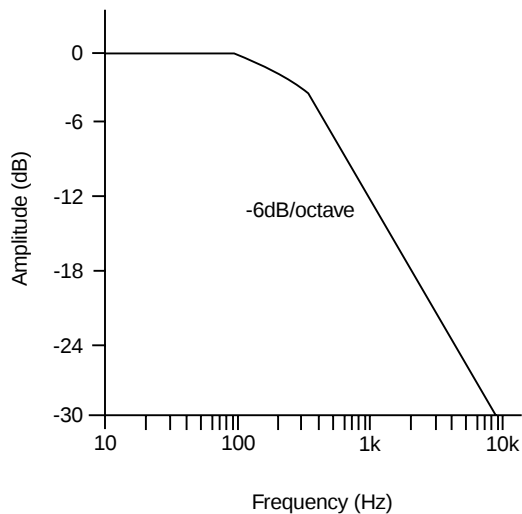


Figure 12: Principal Integrator Response

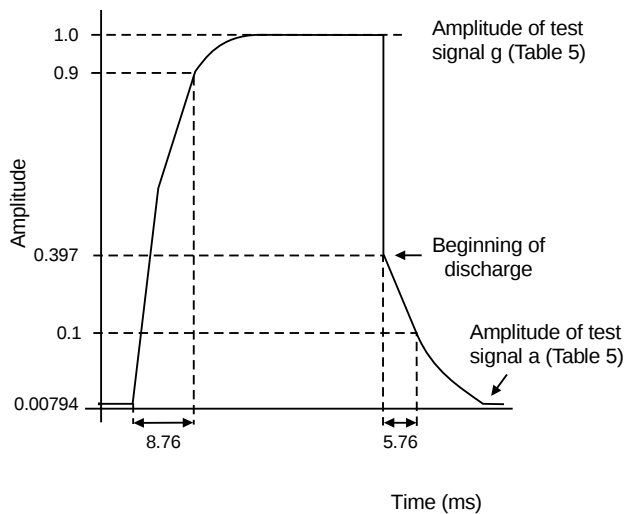


Figure 13: Compand Envelope

6 Performance Specification

6.1 Electrical Performance

6.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

	Min.	Max.	Units
Supply ($V_{DD} - V_{SS}$)	-0.3	7.0	V
Voltage on any pin to V_{SS}	-0.3	$V_{DD} + 0.3$	V
Current			
V_{DD}	-30	30	mA
V_{SS}	-30	30	mA
any other pin	-20	20	mA
E2 Package			
Total Allowable Power Dissipation at $T_{AMB} = 25^{\circ}\text{C}$		550	mW
Derating above 25°C		9	mW/ $^{\circ}\text{C}$ above 25°C
Storage Temperature	-55	125	$^{\circ}\text{C}$
Operating Temperature	-40	85	$^{\circ}\text{C}$
J3 / P6 / L2 Packages			
Total Allowable Power Dissipation at $T_{AMB} = 25^{\circ}\text{C}$		800	mW
Derating above 25°C		10	mW/ $^{\circ}\text{C}$ above 25°C
Storage Temperature	-55	125	$^{\circ}\text{C}$
Operating Temperature	-40	85	$^{\circ}\text{C}$

6.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Min	Typ.	Max.	Units
Supply ($V_{DD} - V_{SS}$)	2.7	3.0 / 5.0	5.5	V
Operating Temperature	-40		85	$^{\circ}\text{C}$
Xtal Frequency	0.5	1.024	1.500	MHz

6.1.3 Operating Characteristics

Details in this section represent target values and are not currently guaranteed.

For the following conditions unless otherwise specified:

$V_{DD} = 5.0V$ at $T_{AMB} = 25^{\circ}C$, Audio Test Frequency = 820Hz Xtal/Clock $f_0 = 1.024MHz$

3-bit Compand Algorithm, Sample Clock Rate = 32kbps, Audio level 0dB ref (0 dBm0) = 489mV_{RMS} measured over a 0-10kHz bandwidth.

	Notes	Min.	Typ.	Max.	Units
Static Values					
Supply Voltage	1	2.7	3.0V / 5.0V	5.5	V
Supply Current					
Enabled at 3.0V			TBD		mA
Enabled at 5.0V			2.75		mA
Powersave at 3.0V			TBD		μA
Powersave at 5.0V			600		μA
Input logic '1'		70% V_{DD}			V
Input Logic '0'				30% V_{DD}	V
Output Logic '1'		80% V_{DD}			V
Output Logic '0'				20% V_{DD}	V
Digital Input Impedance					
Logic I/O pins		1.0	10		MΩ
Logic Input pins, Pull-up Resistor	2	300			kΩ
Digital output impedance			4		kΩ
Analog Input Impedance	4		1		kΩ
Analog Output Impedance				800	Ω
Three State Output Leakage		-4		4	μA
Insertion Loss	3	-2		2	dB
Dynamic Values					
Encoder	1,8				
Analog signal Input levels					
$V_{DD} = 5.0V$	5, 7	-35		6	dBmO
$V_{DD} = 3.0V$	5, 7	-39		2	dBmO
Principal Integrator Frequency			275		Hz
Encoder Passband			3400		Hz
Compand Time Constant			4.0		ms
Decoder					
Analog Signal Output Levels					
$V_{DD} = 5.0V$	5, 7	-35	-14.5	6	dBmO
$V_{DD} = 3.0V$	5, 7	-39		2	dBmO
Decoder Passband		300		3400	Hz

	Notes	Min.	Typ.	Max.	Units
Encoder Decoder (Full Codec)					
Compression Ratio (Cd = 0.5 to Cd = 0.0)		50			
Passband		300		3400	Hz
Stopband		6		10	KHz
Stopband Attenuation			60		dB
Passband Gain			0		dB
Passband Ripple		-3		3	dB
300Hz – 1400Hz		-1		1	dB
1400Hz – 2600Hz		-1		1	dB
2600Hz – 3400Hz		-2		3	dB
Output Noise (Input Short Circuit)	7			-60	dBmO
Perfect Idle Channel Noise					
(Encode Forced)	7		-63		dBmO
Group Delay Distortion	4				
(1000Hz-2600Hz)	6			450	μs
(600Hz-2800Hz)	6			750	μs
(500Hz-3000Hz)	6			1.5	ms
Xtal/clock Frequency			1.024		MHz

Notes:

1. Dynamic characteristics are specified at 5.0V unless otherwise specified.
2. All logic inputs except Encoder and Decoder Data clocks
3. For an Encoder/Decoder combination, Insertion loss contributed by a single component is half this figure.
4. Driven with a source impedance of <100Ω.
5. Recommended values – See Figures 4, 5, 6, and 7.
6. Group Delay Distortion for the full codec is relative to the delay with an 820Hz, -20dB signal at the encoder input.
7. Analog Voltage Levels used:
0dBmO = 489mV_{RMS} = -4dBm = 0dB
-15dBmO = 87mV_{RMS}
-20dBmO = 49mV_{RMS} = -24dBm.

6.1.4 TIMING

Serial Bus Timings (See Figure 14)		Min.	Typ.	Max.	Units
t_{CH}	Clock 1 pulse width	1.0			μs
t_{CL}	Clock 0 pulse width	1.0			μs
t_{IR}	Clock rise time	0	100		ns
t_{IF}	Clock fall time		100		ns
t_{SU}	Data set-up time			450	ns
t_H	Data hold time	600			ns
$t_{SU} + t_H$	Data true time		1.5		μs
t_{PCO}	Clock to output delay time		750		ns
t_{DR}	Data rise time		100		ns
t_{DF}	Data fall time		100		ns
Xtal input frequency = 1.024MHz					

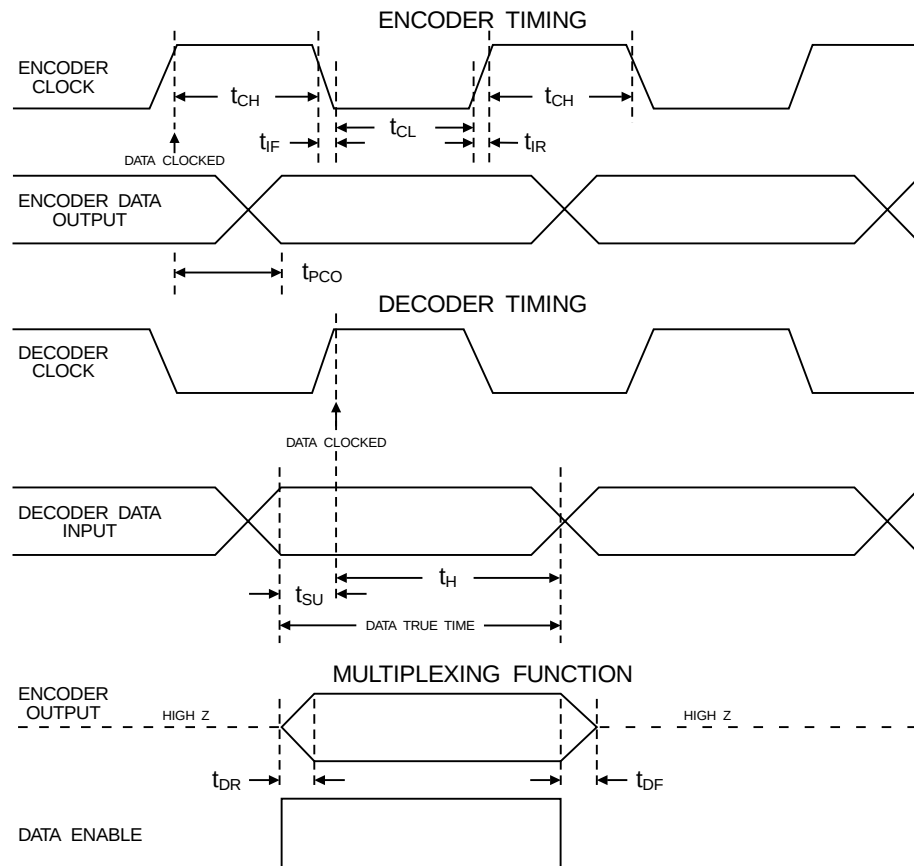


Figure 14: CODEC Timing

6.2 Packaging

For additional packaging options and availability, please contact MX-COM, Inc.

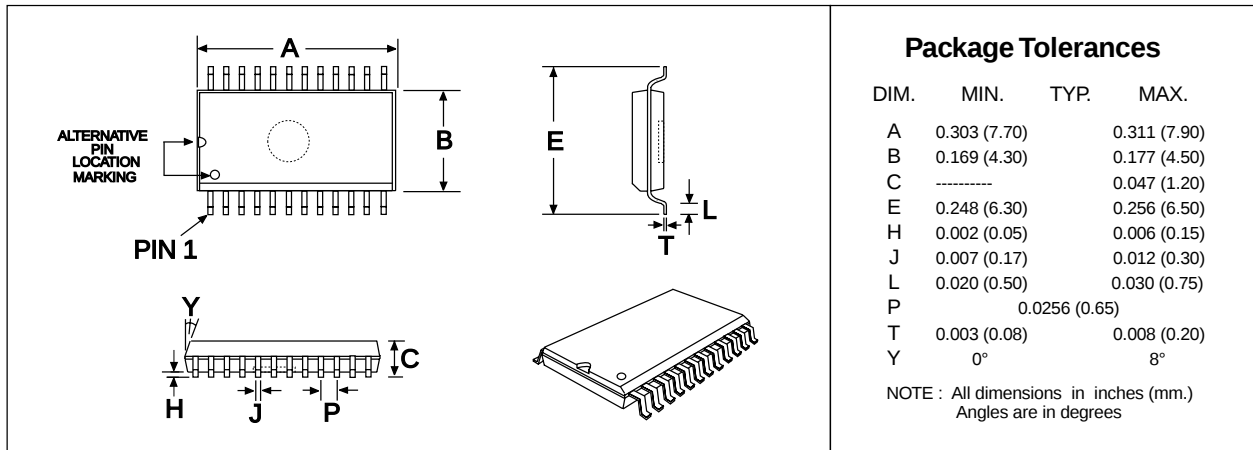


Figure 15: 24-pin TSSOP (E2) Mechanical Outline: *Order as part no. CMX619AE2*

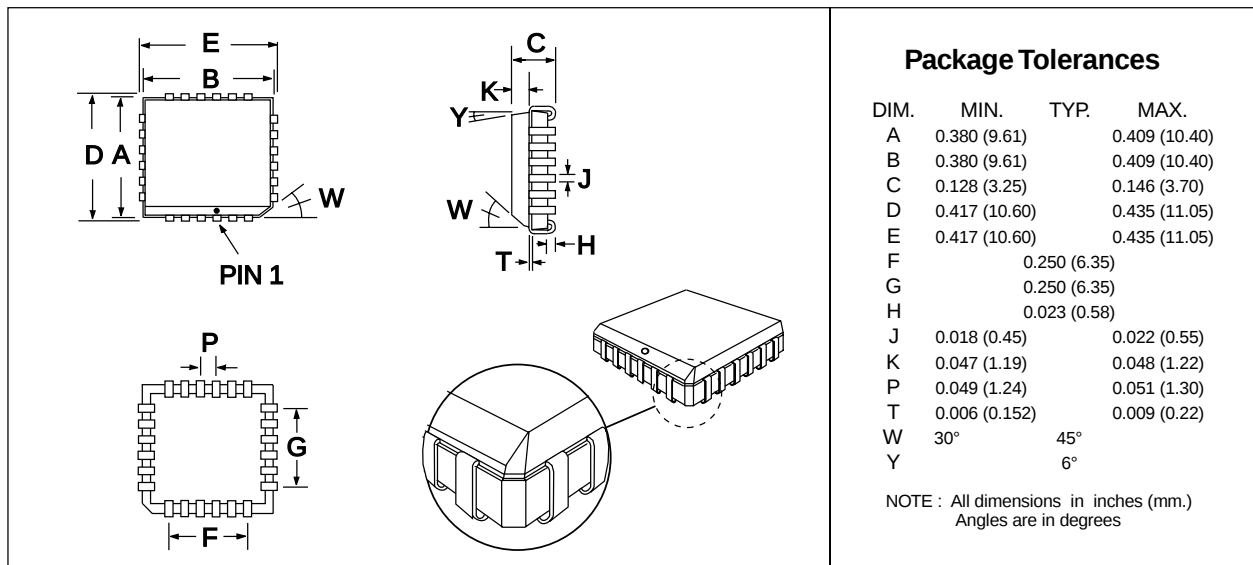


Figure 16: 24-pin PLCC (L2) Mechanical Outline: *Order as part no. CMX619AL2*

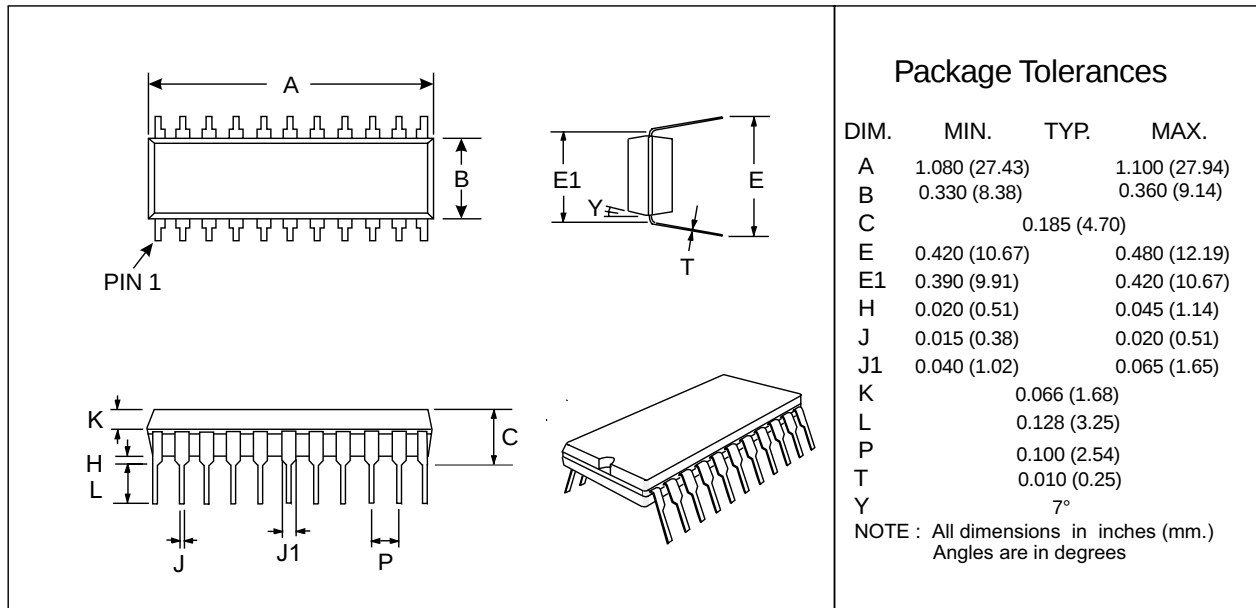


Figure 17: 22-pin PDIP (P6) Mechanical Outline: Order as part no. CMX619AP6

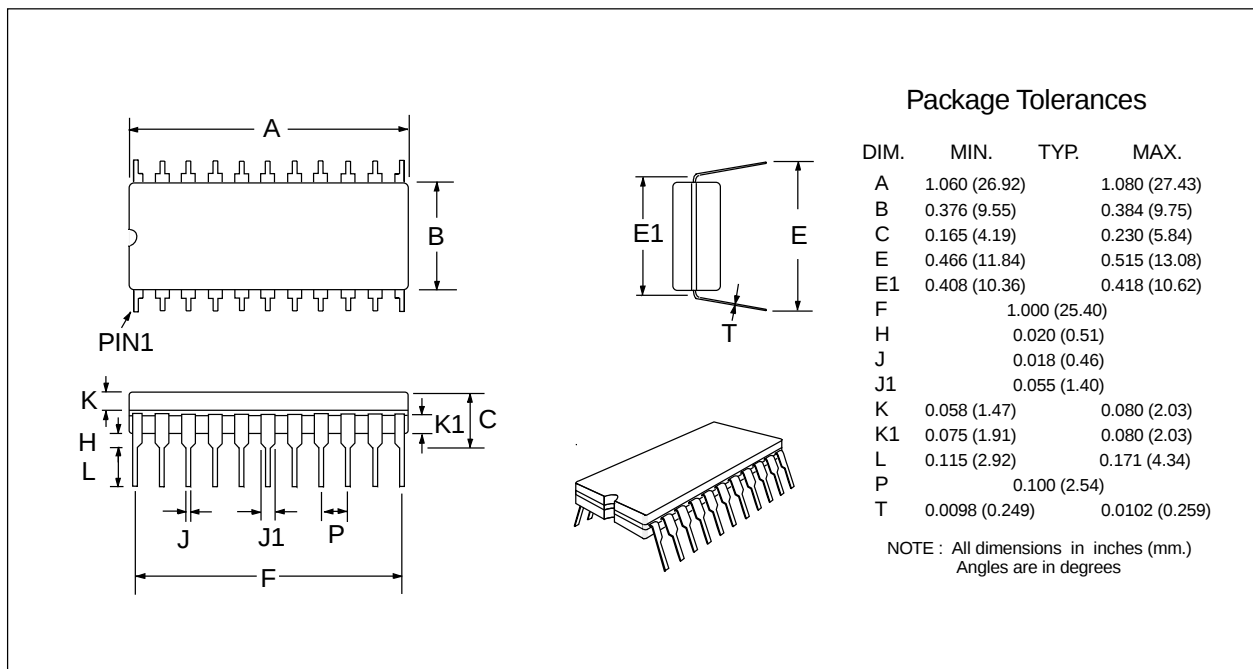


Figure 18: 22-pin Cerdip (J3) Mechanical Outline: Order as part no. CMX619AJ3