FAIRCHILD SEMICONDUCTOR™

September 2001
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FIN1101
LVDS Single Port High Speed Repeater (Preliminary)

General Description

This single port repeater is designed for high speed interconnects utilizing Low Voltage Differential Signaling (LVDS) technology. It accepts and outputs LVDS levels with a typical differential output swing of 350 mV which provides low EMI at ultra low power dissipation even at high frequencies. It can directly accept LVPECL, HSTL, and SSTL-2 for translating directly to LVDS.

Features

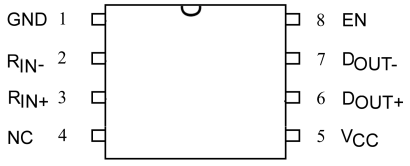
- Greater than 800 Mbps full differential path
- 3.5 ps max random jitter and 135 ps max deterministic jitter
- 3.3V power supply operation
- Wide rail-to-rail common mode range
- Ultra low power consumption
- LVDS receiver inputs accept LVPECL, HSTL, and SSTL-2 directly
- Power off protection
- 6 kV HBM ESD protection
- Meets or exceed the TA/EIA-644-A LVDS standard
- Packaged in 8-pin SOIC and US8 (Preliminary)
- Open circuit, shorted, and terminated fail safe protection

Ordering Code:

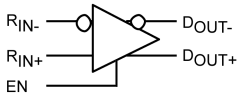
Order Number	Package Number	Package Description
FIN1101M	M08A	8-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
FIN1101K8	MAB08A	8-Lead US8, 0.7mm x 3.1mm x 2.0mm

Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Connection Diagram



Functional Diagram



Pin Descriptions

Pin Name	Description
R_{IN+}	Non-Inverting LVDS Inputs
R_{IN-}	Inverting LVDS Inputs
D_{OUT+}	Non-Inverting Driver Outputs
D_{OUT-}	Inverting Driver Outputs
EN	Driver Enable Pin
V_{CC}	Power Supply
GND	Ground

Function Table

Inputs			Outputs	
EN	**R_{IN+}**	**R_{IN-}**	**D_{OUT+}**	**D_{OUT-}**
H	H	L	H	L
H	L	H	L	H
H	Fail Safe Case		H	L
L or OPEN	X	X	Z	Z

H = HIGH Logic Level
L = LOW Logic Level
X = Don't Care
Z = High Impedance

Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC})	−0.5V to +4.6V
LVDS DC Input Voltage (V_{IN})	−0.5V to +4.6V
LVDS DC Output Voltage (V_{OUT})	−0.5V to +4.6V
Driver Short Circuit Current (I_{OSD})	Continuous 10 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Max Junction Temperature (T_J)	150°C
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C
ESD (Human Body Model)	6000V
ESD (Machine Model)	600V

Recommended Operating Conditions

Supply Voltage (V_{CC})	3.0V to 3.6V
Magnitude of Differential Voltage ($\|V_{ID}\|$)	100 mV to V_{CC}
Operating Temperature (T_A)	−40°C to +85°C

Note 1: The "Absolute Maximum Ratings": are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature and output/input loading variables. Fairchild does not recommend operation of circuits outside databook specification.

DC Electrical Characteristics

Over supply voltage and operating temperature ranges, unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ (Note 2)	Max	Units
V_{TH}	Differential Input Threshold HIGH	See Figure 1			100	mV
V_{TL}	Differential Input Threshold LOW	See Figure 1	−100			mV
V_{IH}	Input High Voltage (EN)		2.0		V_{CC}	V
V_{IL}	Input Low Voltage (EN)		GND		0.8	V
V_{OD}	Output Differential Voltage	R_L = 100 Ω, Driver Enabled, See Figure 2	250	350	450	mV
ΔV_{OD}	V_{OD} Magnitude Change from Differential LOW-to-HIGH				25	mV
V_{OS}	Offset Voltage		1.125	1.25	1.375	V
ΔV_{OS}	Offset Magnitude Change from Differential LOW-to-HIGH				25	mV
I_{OS}	Short Circuit Output Current	D_{OUT+} = 0V & D_{OUT-} = 0V, Driver Enabled			−8	mA
		V_{OD} = 0V, Driver Enabled			±6	mA
I_{IN}	Input Current (EN, D_{INX+}, D_{INX-})	V_{IN} = 0V to V_{CC}, Other Input = V_{CC} or 0V (for Differential Inputs)			±20	µA
I_{OFF}	Power-Off Input or Output Current	V_{CC} = 0V, V_{IN} or V_{OUT} = 0V to 4.6V			±20	µA
I_{CCZ}	Disabled Power Supply Current	Drivers Disabled			5	mA
I_{CC}	Power Supply Current	Drivers Enabled, Any Valid Input Condition			15	mA
$I_{PU/PD}$	Output Power-Up/ Power Leakage Current	V_{CC} = 0V to 1.5V			±20	µA
I_{OZ}	Disabled Output Leakage Current	Driver Disabled, D_{OUT+} = 0V to 4.6V or D_{OUT-} = 0V to 4.6V			±20	µA
V_{IC}	Common Mode Voltage Range		V_{ID}/2		V_{CC}− (V_{ID}/2)	V
C_{IN}	Input Capacitance			3		pF
C_{OUT}	Output Capacitance			4		pF

Note 2: All typical values are at T_A = 25°C and with V_{CC} = 3.3V.

AC Electrical Characteristics

Over supply voltage and operating temperature ranges, unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ (Note 3)	Max	Units
t_{PLHD}	Differential Propagation Delay LOW-to-HIGH	R_L = 100 Ω, C_L = 5 pF, V_{ID} = 100 mV to 1100 mV, V_{IC} = V_{ID}/2 to V_{CC-} (V_{ID}/2), Duty Cycle = 50%, See Figure 3 and Figure 4	0.8		1.8	ns
t_{PHLD}	Differential Propagation Delay HIGH-to-LOW		0.8		1.8	ns
t_{TLHD}	Differential Output Rise Time (20% to 80%)		0.29		0.58	ps
t_{THLD}	Differential Output Fall Time (80% to 20%)		0.29		0.58	ps
$t_{SK(P)}$	Pulse Skew $\lvert t_{PLH} - t_{PHL} \rvert$				0.2	ns
$t_{SK(PP)}$	Part-to-Part Skew (Note 4)				0.5	ns
f_{MAX}	Maximum Frequency (Note 5)		800			Mbps
t_{PZHD}	Differential Output Enable Time from Z to HIGH	R_L = 100 Ω, C_L = 5 pF, See Figure 5 and Figure 6			10	ns
t_{PZLD}	Differential Output Enable Time from Z to LOW				10	ns
t_{PHZD}	Differential Output Disable Time from HIGH to Z				10	ns
t_{PLZD}	Differential Output Disable Time from LOW to Z				10	ns
t_{DJ}	LVDS Data Jitter, Deterministic	V_{ID} = 300 mV, PRBS = 2^{23} – 1, V_{IC} = 1.2V at 800 Mbps		100	135	ps
t_{RJ}	LVDS Clock Jitter, Random (RMS)	V_{ID} = 300 mV V_{IC} = 1.2 V at 400 MHz		2.2	3.5	ps

Note 3: All typical values are at T_A = 25°C and with V_{CC} = 3.3V.

Note 4: $t_{SK(PP)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices switching in the same direction (either LOW-to-HIGH or HIGH-to-LOW) when both devices operate with the same supply voltage, same temperature, and have identical test circuits.

Note 5: Passing criteria for maximum frequency is the output V_{OD} > 250 mV and the duty cycle is better than 45% / 55% with all channels switching.

Required Specifications:

1. When the true and complement LVDS outputs (having a 100Ω connected between outputs) are connected to 3.75kΩ resistors and the common point of those 3.75kΩ resistors are connected to a voltage source that sweeps from 0V to 2.4V, the DC V_{OD} and ΔV_{OD} are still maintained (see Figure 1).
2. When the true and complement LVDS inputs are connected together to a voltage source that sweeps from 0V to 2.4V with respect to the common ground, then the absolute value of the difference in input leakage current is less than 6μA (see Figure 2)
3. Pull-down resistor is required on the enable (EN) input.
4. Human Body Model ESD and Machine Model ESD should be measured using MIL-STD-883C method 3015.7 standard.
5. Latch-up immunity should be tested to the EIA/JEDEC standard number 78 (EIA/JESD78).
6. When the true and complement LVDS outputs are connected with 49.9Ω resistors each to common point, then the common point does not vary by more than 150mV under all process, temperature, and voltage conditions when the outputs switch either from LOW-to-HIGH or from HIGH-to-LOW (see Figure 3, C_L = board + pin stray capacitance)
7. When the LVDS inputs are not driven either in High Impedance, shorted together, or terminated with a resistor, the outputs go the HIGH state (D_{OUT+} = H, D_{OUT-} = L) and the LVDS inputs do not sink or source more than 20μA.

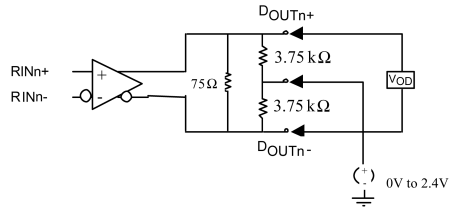


FIGURE 1. Common Mode Supply Test Circuit

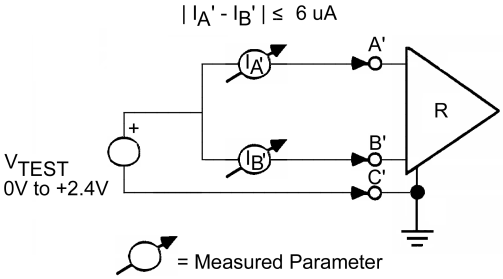


FIGURE 2. Receiver Input Balance Measurements

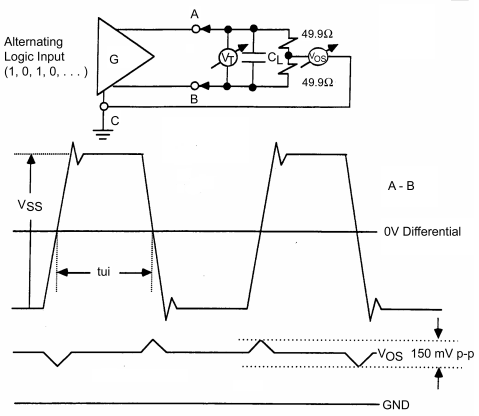


FIGURE 3. Dynamic V_{OS} Test Circuit and Waveforms

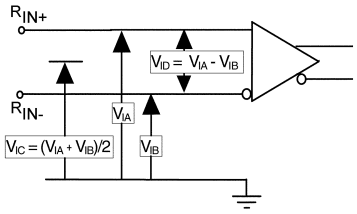


FIGURE 4. Differential Receiver Voltage Definitions and Propagation I and Transition Time Test Circuit

Required Specifications: (Continued)

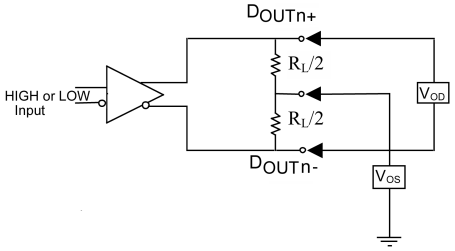
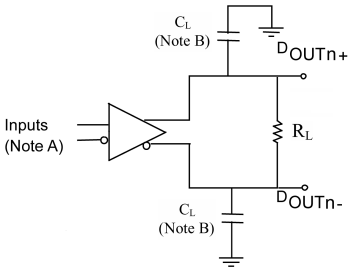


FIGURE 5. Differential Driver DC Test Circuit



Note A: All input pulses have frequency = 10MHz, t_R or t_F < = 1ns

Note B: C_L includes all probe and jig capacitances

FIGURE 6. Differential Driver Propagation Delay and Transition Time Test Circuit

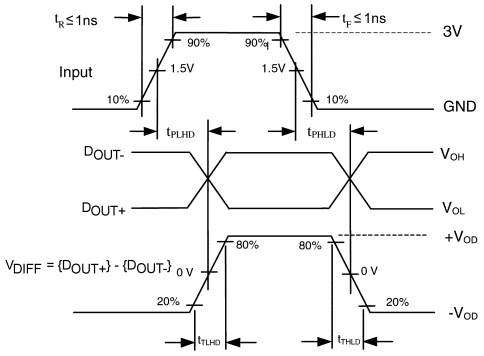
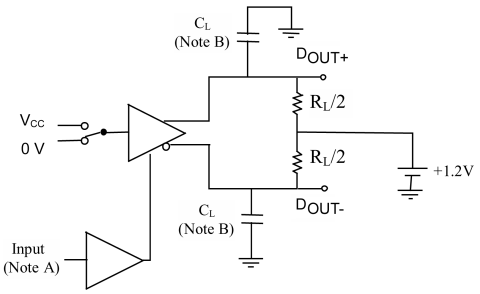


FIGURE 7. AC Waveforms



Note A: All input pulses have frequency = MHz, t_R or t_F < = 2 ns

Note B: C_L includes all probe and jig capacitances

FIGURE 8. Differential Driver Enable and Disable Test Circuit

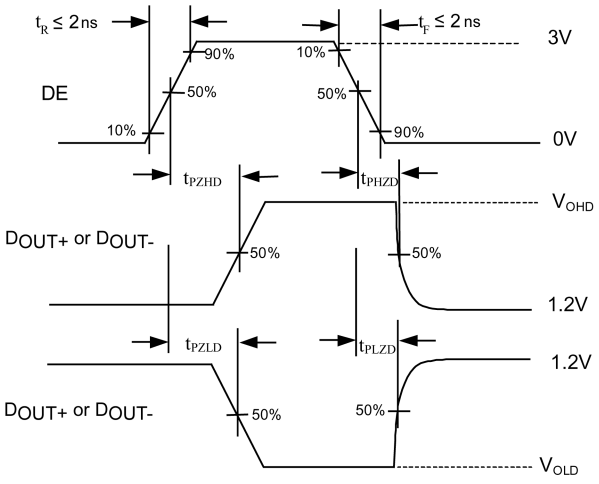
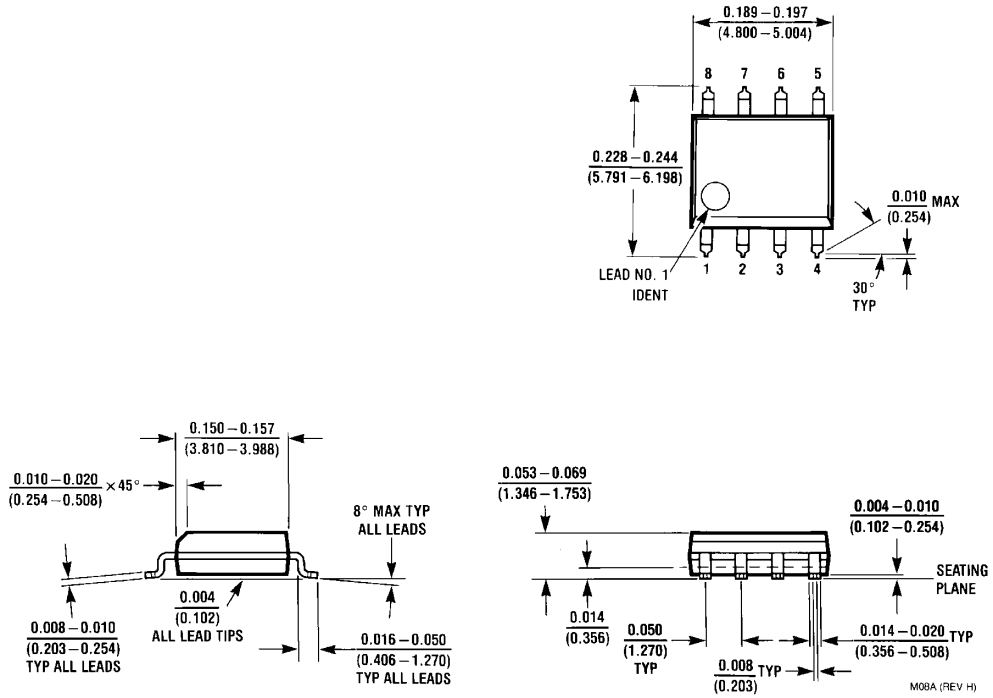


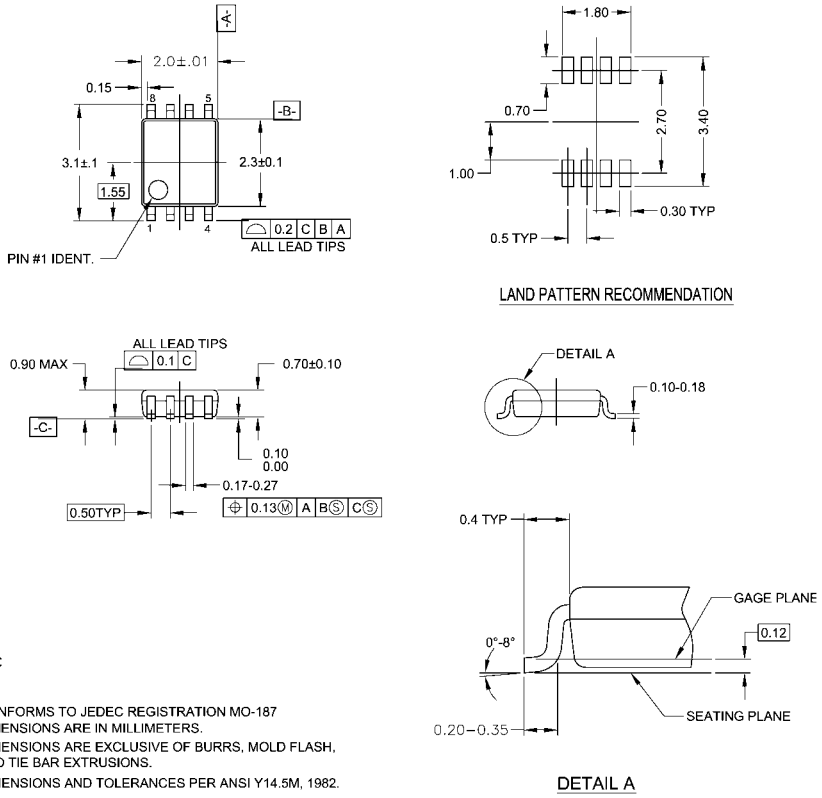
FIGURE 9. Enable and Disable AC Waveforms

Physical Dimensions inches (millimeters) unless otherwise noted



8-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M08A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-187
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MAB08AREVB

8-Lead US8, 0.7mm x 3.1mm x 2.0mm
Package Number MAB08A
(Preliminary)

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